



# AZD141 - IQS9320 KEYBOARD DESIGN GUIDE

Design guide for an inductive sensing keyboard using Azoteq's ProxFusion® IQS9320 sensor IC.  
Design guidance and production specifications to consider.

## Contents

<b>1</b>	<b>Introduction</b>	<b>3</b>
<b>2</b>	<b>Design Specification / Product Requirements</b>	<b>4</b>
2.1	Keyboard Layout and Number of Keys . . . . .	4
2.2	Key Switch Characteristics . . . . .	4
2.3	Key Switch Configuration . . . . .	4
2.4	Channel sampling and polling period . . . . .	4
2.5	Ingress Protection Rating - Liquid . . . . .	5
2.6	Inductive Proximity Interference . . . . .	5
2.7	Operational Environment . . . . .	5
2.8	EMC Pre-Compliance . . . . .	5
2.9	Current Consumption . . . . .	6
2.10	Mechanical specification . . . . .	6
2.11	Software features . . . . .	7
<b>3</b>	<b>Proposed Solution</b>	<b>8</b>
3.1	System Description . . . . .	8
3.2	Azoteq Device Selection Guide . . . . .	9
3.3	Selected Azoteq Device . . . . .	9
<b>4</b>	<b>Design Resources</b>	<b>11</b>
4.1	Documents . . . . .	11
4.2	Software tools and example code . . . . .	11
<b>5</b>	<b>Design Implementation</b>	<b>12</b>
5.1	Sensor Design . . . . .	12
5.2	Circuit Design . . . . .	12
5.3	PCB Layout Design . . . . .	17
5.3.1	Device placements in the key grid . . . . .	17
5.3.2	Power ( <i>VDD</i> ) and regulated ( <i>VREG</i> ) supply decoupling . . . . .	17
5.3.3	Sensor trace routing . . . . .	18
5.3.4	Digital interface routing . . . . .	20
5.3.5	Coil design . . . . .	20
5.3.6	Coil termination . . . . .	23
5.3.7	PCB-material, -layer stack up and -finishing . . . . .	23
5.4	Mechanical Design . . . . .	25
5.4.1	Assembly . . . . .	25
5.4.2	Housing / casing . . . . .	26
5.4.3	Mechanical movement and its effects . . . . .	27
5.4.4	Key frame (overlay) design . . . . .	27
5.4.5	Stand-off supports and spacers . . . . .	27
5.4.6	Metal bracket key braces . . . . .	28
5.4.7	Connectors and cables . . . . .	28



5.5	Manufacturing . . . . .	29
5.6	IC Setup . . . . .	29
<b>6</b>	<b>Design Verification</b>	<b>30</b>
6.1	Keyboard layout and number of keys . . . . .	30
6.2	Key Switch Characteristics . . . . .	30
6.3	Key Switch Configuration . . . . .	32
6.4	Channel sampling and polling rate . . . . .	34
6.5	Ingress Protection Rating - Liquid . . . . .	36
6.6	Inductive Proximity Interference . . . . .	37
6.7	EMC Pre-Compliance . . . . .	38
6.7.1	Radiated Emissions . . . . .	38
6.7.2	Conducted Emissions . . . . .	39
6.7.3	Radiated Immunity . . . . .	40
6.7.4	Conducted Immunity . . . . .	41
6.7.5	ESD Immunity . . . . .	42
6.8	Current Consumption . . . . .	43
<b>7</b>	<b>Interface Description</b>	<b>45</b>
7.1	I <sup>2</sup> C interface mode . . . . .	45
7.2	Key scan interface mode . . . . .	45
7.3	MCU driver, keyboard interface and interaction reference code . . . . .	45
7.4	Software flow . . . . .	47
7.5	Additional status indication . . . . .	48
7.6	PC interface . . . . .	48
<b>8</b>	<b>Revision History</b>	<b>49</b>
<b>A</b>	<b>Bill of Materials</b>	<b>50</b>
<b>B</b>	<b>Schematic and Layout</b>	<b>51</b>
B.1	Schematic design . . . . .	52
B.2	PCB design: Gerbers . . . . .	58
B.3	PCB design: Top and bottom assembly . . . . .	62
B.4	PCB design: 3D bodies . . . . .	63
<b>C</b>	<b>Mechanical Design</b>	<b>64</b>
C.1	PCB design . . . . .	64
C.2	Key design . . . . .	66
C.3	Coil design . . . . .	67
C.4	Full keyboard assembly . . . . .	68
<b>D</b>	<b>Glossary</b>	<b>71</b>



## 1 Introduction

The aim of this document is to provide a step-by-step guide on how to design an inductive sensing keyboard for multipoint actuation for any use case or user customisability. The Azoteq technology used for this application is the [ProxFusion® IQS9320](#) sensor IC.

A summary of the design process is shown below:



*Figure 1.1: Design Process Summary*

The result of this process is to meet the specification of keyboard designers and manufacturers. Construction and performance considerations are discussed and procedures of verification are explained for the featured technology.



## 2 Design Specification / Product Requirements

This section outlines key design specifications that need to be considered when designing a contactless inductive sensing keyboard.

### 2.1 Keyboard Layout and Number of Keys

A 65% ANSI keyboard layout with a total of 68 key switches. With a single IQS9320 device supporting up to 20 key switches at least 4 IQS9320 devices are required.

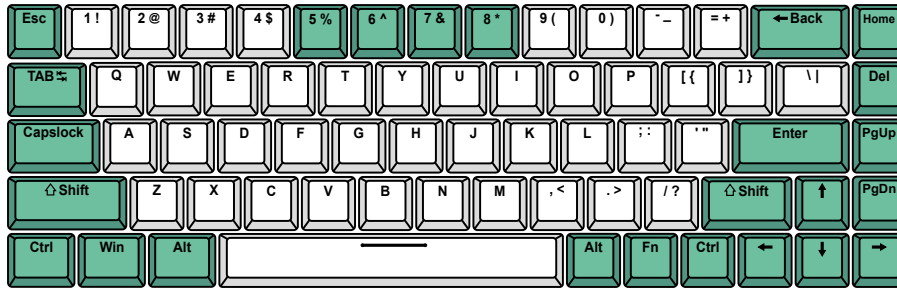


Figure 2.1: ANSI 65% keyboard layout

### 2.2 Key Switch Characteristics

The key switch characteristics should meet the following requirements:

- > Selectable actuation points should approximate a linear response over the entire travel range of the key.
- > Minimum selectable actuation point at a displacement of 0.30mm.
- > Actuation point accuracy of  $\pm 0.10\text{mm}$ .

### 2.3 Key Switch Configuration

Individual keys can be configured independently as follows:

- > Discrete switch with a single adjustable actuation and release point.
- > Discrete switch with a single adjustable actuation point and quick release, TriggerMax™.
- > Analogue switch with up to 255 levels.

### 2.4 Channel sampling and polling period

The time required by the IQS9320 device to update the activation state/output level of a given channel is the channel sampling period. The time required to required by the MCU to read the activation state/output level registers via I2C is the polling period.

Table 2.1: Channel sampling and polling period

Design Specification	Requirement
Channel sampling period	< 1ms <sup>1</sup>
Channel polling period	< 1ms <sup>1</sup>

<sup>1</sup>This applies for the discrete digital and analogue key modes





## 2.5 Ingress Protection Rating - Liquid

The ingress protection rating of the PCBA and key switch assembly should conform to the IPx2 rating as specified by the IEC 60529.

*Table 2.2: IEC 60529 IPxy rating second digit: Liquids*

Level	Object size protected against	Effective against
0	Not protected	
1	Vertically falling water drops	Vertically falling drops shall have no harmful effects
2	Vertically falling water drops when enclosure tilted up to 15°	Vertically falling drops shall have no harmful effect when the enclosure is tilted at an angle up to 15° from its normal position
3	Spraying water	Water sprayed at an angle up to 60° on either side of the vertical shall have no harmful effect
4	Splashing water	Water splashing against the enclosure from any direction shall have no harmful effect
5	Water jets	Water projected in jets against the enclosure from any direction shall have no harmful effects
6	Powerful water jets	Water projected in powerful jets against the enclosure from any direction shall have no harmful effects
7	Temporary immersion in water	Ingress of water in quantities causing harmful effects shall not be possible when the enclosure is continuously immersed in water under conditions specified by the manufacturer and user but which are more severe than 7
8	Continuous immersion in water	The equipment is suitable for continuous immersion in water under conditions which shall be specified by the manufacturer. Normally, this will mean that the equipment is hermetically sealed. However, with certain types of equipment, it can mean that water can enter but only in such a manner that it produces no harmful effects
9	High pressure and temperature water jets	Water projected at high pressure and high temperature against the enclosure from any direction shall not have any harmful effects

## 2.6 Inductive Proximity Interference

Inductive sensing false activation can occur when conductive metal and or highly permeable materials are moved within the vicinity of the sensor coils at distances of  $\frac{D_{out}}{2}$ . System design should be immune to the following:

- > Permanent magnets with magnetic flux densities up to 400mT or 4000G.
- > Highly permeable material such as ferrites with relative permeability values up to 150.
- > Conductive metal objects made from materials like Aluminium, Copper and Stainless Steel.

## 2.7 Operational Environment

*Table 2.3: Operational Environment Specification*

Environment	Specification
Temperature	-10°C to +60°C
Humidity	30% to 70% Relative Humidity

## 2.8 EMC Pre-Compliance

Device should conform with the following EMC pre-compliance specifications:



Table 2.4: EMC Specification

EMC Specification	Compliance Standard	Level
Radiated Emissions (30MHz - 300MHz)	CISRP22	Emissions must be below limit line according to specification on Q-Peak and average measurements
Conducted Emissions (150kHz - 30MHz)	CISPR11 and CISPR15	
Radiated Immunity (400MHz - 4GHz)	IEC 61000-4-3	Field Strength 1V/m
		Field Strength 3V/m
		Field Strength 10V/m
		Field Strength 30V/m
Conducted Immunity (150kHz - 80Mhz)	IEC 61000-4-6	Noise Amplitude 1V
		Noise Amplitude 3V
		Noise Amplitude 10V
ESD Immunity	IEC 61000-4-2	2KV-Contact Discharge and 2KV-Air Discharge
		4KV-Contact Discharge and 4KV-Air Discharge
		6KV-Contact Discharge and 8KV-Air Discharge
		8KV-Contact Discharge and 15KV-Air Discharge

Table 2.5: Immunity Test Pass/Fail Classification

Class	Description
A	Device is fully functional during test. Normal performance within limits specified by the manufacturer, requestor, or purchaser.
B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention.
C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention.
D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

## 2.9 Current Consumption

Table 2.6: Keyboard Current Consumption

Report Rate	Test Condition	Current
0.75ms	Event Mode; LED's Disabled	27mA
5ms		7.2mA
20ms		2.4mA
50ms		1.0mA
100ms		0.5mA

## 2.10 Mechanical specification

- > Relative distance between key-frame and PCB should remain fixed during operation.
- > Any conductive metals and/or highly permeable materials in the housing that do not form part of the PCBA and switch case assembly should have a fixed distance to the PCBA during operation.
- > Distance of PCBA to the bottom case should be at least  $\frac{D_{out}}{2}$ .
- > Distance of PCBA to top of keycap should be at least  $\frac{D_{out}}{2}$ .
- > If the bottom casing is made of metal and the distance of the PCBA to the bottom casing is less than  $\frac{D_{out}}{2}$ , then this distance should remain fixed during operation.



## 2.11 Software features

- > NKRO and 100% anti ghosting.
- > TriggerMax™ for quick lift-off release.
- > Individual key adjustable actuation point.
- > Analogue keys with up to 255 output levels.



### 3 Proposed Solution

This section provides a high level description of Azoteq’s inductive keyboard solution, motivation for a specific IQS sensor IC application and suitability thereof for a key sensing solution. Trade-off considerations will be discussed in context to feature offerings.

#### 3.1 System Description

The proposed design’s system description / high-level overview includes three basic parts:

- > Computer (PC or laptop)
- > Master controller (embedded MCU)
- > Keyboard with,
  - IQS ICs (inductive sensing controllers),
  - PCB coils,
  - mechanical keys (patented design for inductive usage),
  - and discrete key RGB LEDs / distributed back-lighting (optional)

The focus of this design guide is on the keyboard layout and PCB design. Key and coil complementary design and interaction within the intended mechanical structural components of the case and key frame are crucial in this regard. Risks will be highlighted in the mechanical and electrical design of the system. Sensor ICs will operate as slave devices and effective service routines and recommended control procedures will be showcased as executed by any generic embedded micro-controller.

Figure 3.1 below shows a typical system diagram layout for an Inductive Keyboard implementation.

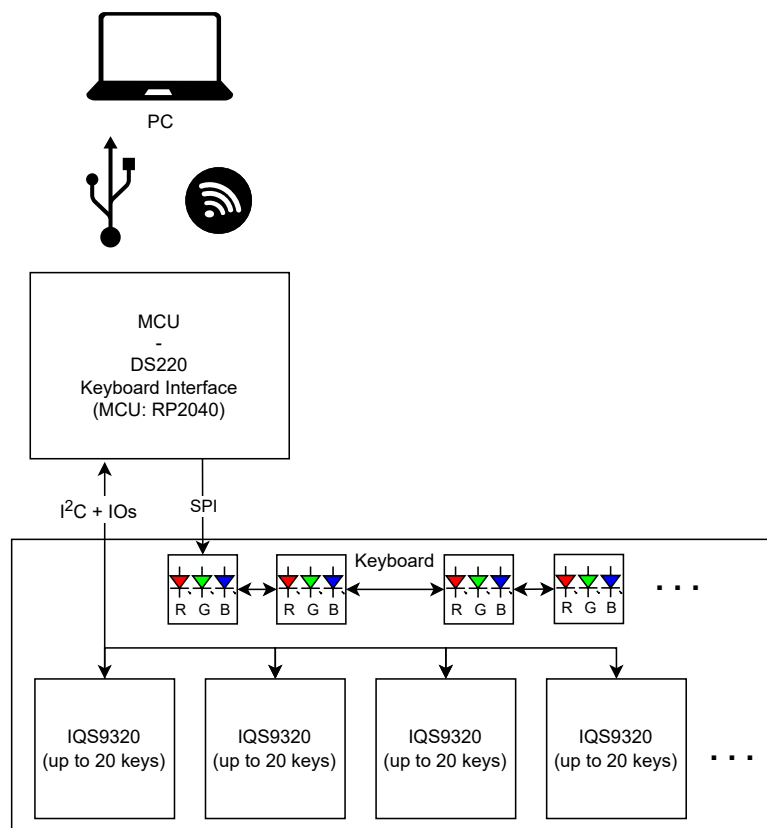


Figure 3.1: Inductive Keyboard System Diagram



### 3.2 Azoteq Device Selection Guide

Azoteq’s Inductive sensor IC solutions for keyboards offerings are:

> IQS7320A

> IQS9320

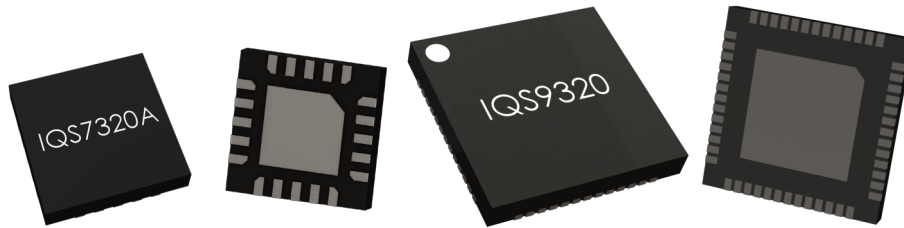


Table 3.1: ProxFusion® Inductive Sensors For Keyboards

IQS part	Max. keys	Package	Communication interface	Report rate	TriggerMax™
<b>IQS7320A</b>	4	QFN20	Key-scanning	1kHz	Yes
<b>IQS9320</b>	20	QFN52	I <sup>2</sup> C Key-scanning	4kHz 2kHz	Yes

Considering the need for typical gaming keyboards with high response rate and to implement inductive sensing on all keys for a 65% (68 keys) or full keyboard (108+ keys) the **IQS9320** is better suited for such a solution. The design will still require a minimum of 4 discrete IQS9320 sensor ICs to serve all 68 keys. Allocation of the number of keys per device can be done equally (17 keys per IC) or in another fashion to optimise for either layout and/or sampling and processing. In our example design featured in this guide we have assigned 4 subsystems each with 17 keys (U1 to U4; even number for 9 sensors in cycle 0 and 8 sensors in cycle 1). Key groups associated/sampled per device was coloured coded as shown in Figure 3.2 below.

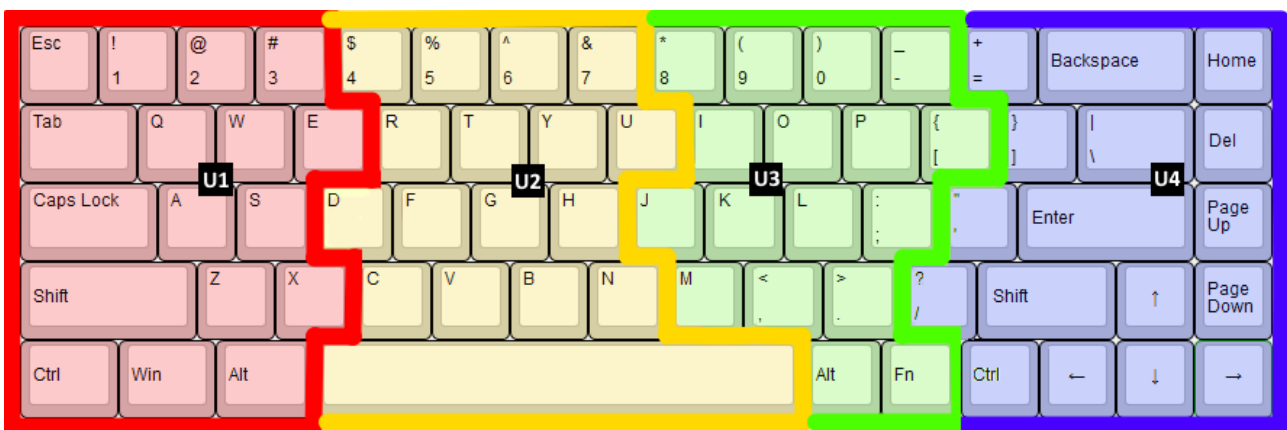


Figure 3.2: 65% - 68 key inductive keyboard layout with IQS9320 device placement and key assignment

### 3.3 Selected Azoteq Device

The IQS9320 was selected because of the higher number of channels/keys that can be sensed by a single device. The IQS9320 device has 13 independent ProxFusion® sensor engines, each with two receiver inputs, which can be sampled within two consecutive cycles. Some engines have an



additional pin and together with the unused GPIOs these pins are purposed as sensor driver/transmitters and can be assigned irrespectively to any sensor engine input. Due to the requirement of assigning inductive sensing pairs (1 Rx receiver + 1 Tx transmitter) for each sensor coil/key, the maximum number of pairs that can be realised are 20 per device (utilising all pins). The achievable report rate is dependent on the number of keys that need to be sampled on each device and the specific mode of reporting information (I<sup>2</sup>C or key scanning). Slightly higher rates can be achieved using the *Fast-mode-plus* capable I<sup>2</sup>C protocol at the maximum clock speed of 1MHz as desired in professional gaming use.

For detailed technical description and comparison data tables on the IQS9320 (or IQS7320A), please refer to *section 4* for a link to the device's datasheet.



## 4 Design Resources

### 4.1 Documents

- > [IQS9320 Datasheet](#)
- > [IQS9320 65% Demo KB User Guide](#)
- > [IQS9320 keyboard Interface Guide](#)
- > [Unionwell Plunger Keys Datasheet](#)
- > [AZD115-Inductive Sensing Application Note](#)
- > [IQS9320 20 Key Demo User Guide](#)
- > [IQS9320 Calibration and Test Jig Guide](#)

### 4.2 Software tools and example code

- > [IQS9320 GUI](#)
- > [IQS9320 example code](#)
- > [Keyboard Interface Python module](#)
- > [Keyboard Interface MCU example code](#)
- > [IQS9320 Keyboard Calibration Example Code](#)



## 5 Design Implementation

This chapter describes the design of the inductive keyboard product (65% keyboard layout with 68 keys in total) using four IQS9320 devices.

### 5.1 Sensor Design

Each key design differ in minor detail and the PCB coil layout can be tailored specifically to the intended key part. The design showcased in this document was prepared specifically to a key manufactured by Unionwell. This key consists of a metal stud with a tapered shaped head referred to as the plunger. The plunger piece is retracted when the key is in the relaxed state and will protrude at the bottom of the casing when the key stem is pressed or deflected downward. The amount of conductive material introduced into the PCB coil by means of this moving plunger piece effects the inductive property and changes the impedance response of the LC tank circuit resonated and sensed by the IQS9320. The IQS can accurately sense this impedance change as a change in then number of charge converted in units of Counts.

Refer to application note [AZD115 - Inductive sensing](#) and the relevant [IQS9320 Datasheet](#) for technical guidance.

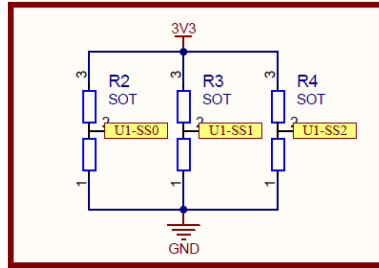
### 5.2 Circuit Design

The complete circuit design schematic is featured in *Appendix B*, but some representative circuit sub-sections will be shown as discussed for clarity. Care should be taken to follow the featured reference schematic from the IQS9320 datasheet as required for either key scanning or I<sup>2</sup>C streaming (the latter showcased by this design guide).

Power supply design and protection should be considered for general commercial PC usage and supported USB standards for power delivery. Voltage regulation for the IQS devices should be implemented using an LDO regulator capable to deliver the total amount of peak power consumption from all devices and reject/reduce supply noise. It is advised to supply back lighting LEDs from a different regulator or be appropriately isolated from the incoming 5V USB supply rail as to not affect the IQS sensor's supply by causing a voltage drop or switching ripple noise. A poly-switch / PPTC can be used to protect USB ports against harmful over current surges in fault conditions. Ferrite beads can be used to filter noise on supply lines and high current carrying traces.

Each IQS9320 device on the shared bus can be assigned an unique I<sup>2</sup>C address based on the state of the address select input pin's logic at start-up.





Address Select 2	Address Select 1	Address Select 0	7-bit Device Address	8-bit Read Address	8-bit Write Address
LOW	LOW	LOW	0x30	0x61	0x60
LOW	LOW	HIGH	0x32	0x65	0x64
LOW	HIGH	LOW	0x34	0x69	0x68
LOW	HIGH	HIGH	0x36	0x6D	0x6C
HIGH	LOW	LOW	0x38	0x71	0x70
HIGH	LOW	HIGH	0x3A	0x75	0x74
HIGH	HIGH	LOW	0x3C	0x79	0x78
HIGH	HIGH	HIGH	0x3E	0x7D	0x7C

Figure 5.1: IQS9320 Device Address Selection

Focusing on a single key’s schematic design refer to the circuit showed in Figure 5.2 (collage of snippets for 'Esc' key sections)

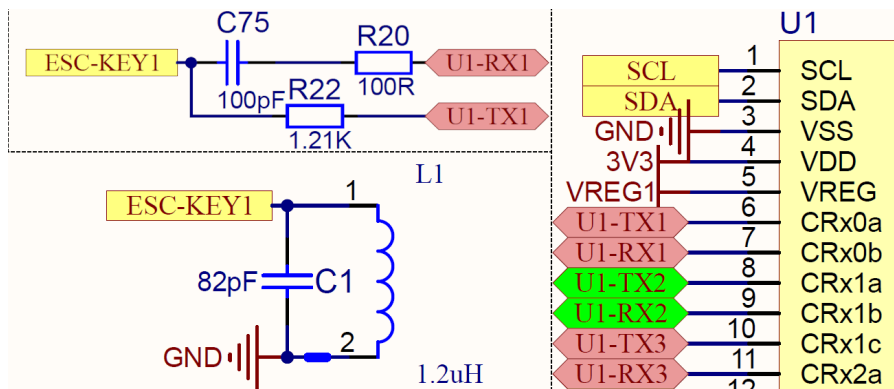


Figure 5.2: Inductive Circuit Schematic Layout for a Single Key

In Figure 5.2 the components R20 = 100 Ω and C75 = 100 pF (C0G/NP0 recommended) are standard use on all receivers (Rx). The resistor size on the transmitter (Tx) needs to be chosen according to the type of Tx (CRx or CTx pin) and will also determine the Q value of the LC tank response. This is directly related to the sensitivity of the sensor. The capacitor C1 = 82 pF (C0G/NP0 mandatory) determines the resonant peak response in parallel conjunction with the coil inductance. The resonant frequency should be chosen with the required amount of tolerance and compensation advised. Once this desired peak frequency is determined the value for the resonating capacitor can be calculated by acquiring the inductance (with the key and any metal frame/supports assembled in position). The frequency at which this peak is located always needs to be higher than the Tx frequency at which the LC tank circuit will be excited. A closest available capacitor size should rather be made lower than the calculated C to ensure the peak is shifted upwards which is the desired response that will be achieved with any key press. This will ensure that the impedance will always decrease (with decrease in inductance) as measured at the fixed excitation frequency.

Engine-cycle allocation determines which Rx (receiver) input will be utilised. Any CRx receiver pin (a or b or c) can be used as Rx's (receivers) with the latest IQS9320 firmware device. The only restriction





Table 5.1 below shows the cycle allocation and channel mapping.

Table 5.1: Channel Rx-Tx And Cycle Allocation

Engine	Channel	Cycle 0		Channel	Cycle 1	
		Rx	Tx		Rx	Tx
Engine 0	CH0	CRx0b	CRx0a			
Engine 1				CH9	CRx1b	CRx1a
Engine 2	CH1	CRx2a	CRx1c	CH10	CRx2c	CRx2b
Engine 3	CH2	CRx3b	CRx3a			
Engine 4				CH11	CRx4b	CRx4a
Engine 5	CH3	CRx5a	CRx4c			
Engine 6	CH4	CRx6c	CRx6b	CH12	CRx6a	CRx5b
Engine 7				CH13	CRx7b	CRx7a
Engine 8	CH5	CRx8b	CRx8a			
Engine 9				CH14	CRx9a	CRx8c
Engine 10	CH6	CRx10a	CRx9b	CH15	CRx10c	CRx10b
Engine 11	CH7	CRx11b	CTx11a			
Engine 12	CH8	CRx12b	CTx6	CH16	CRx12a	CTx7

From the cycle allocation and channel mapping tabulated in table 5.1 above, one will notice that not all sensor engines were utilised in each cycle as receivers. These engine's pins were instead assigned to function as Tx's due to their physical pin location alongside other engines on the QFN52 package making it possible to have close neighbouring Rx and Tx pairs for each coil/key. Figure 5.4 below shows these pairings of Rx and Tx pins to form channels. This alternating cycles and Rx-Tx pins assignment is preferred for sensing analogue considerations, although numerous other combinations are possible depending on the number of keys and application layout thereof.

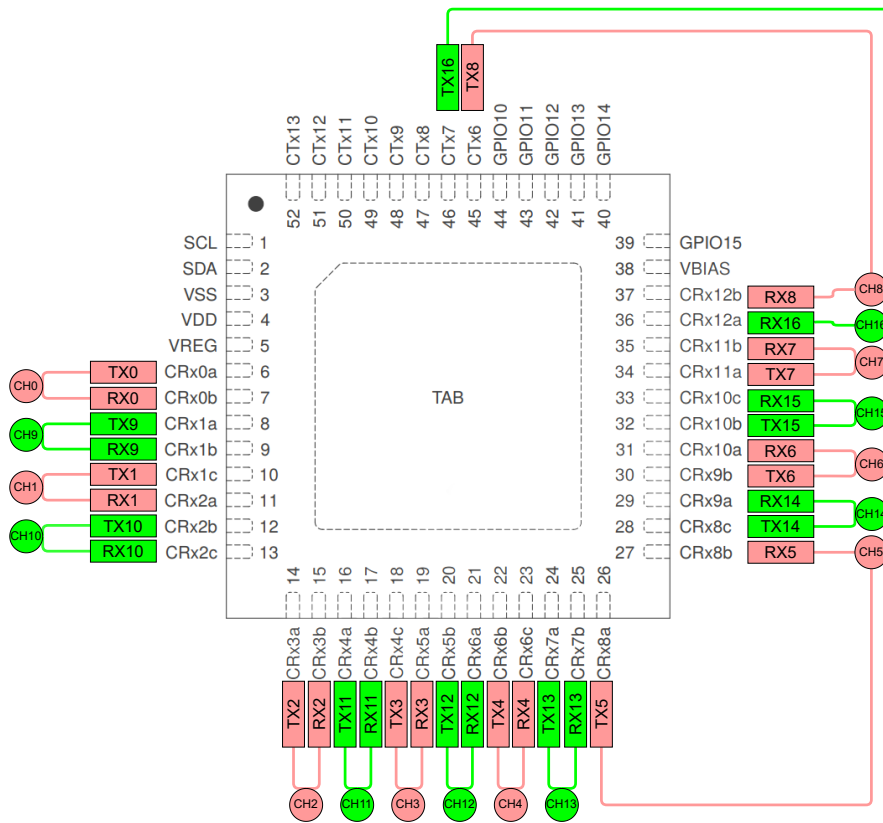


Figure 5.4: IQS9320 QFN52 Pinout and Channel mapping (Passives Omitted)



For the large decoupling capacitors on *VREG* (22  $\mu$ F) and *VDD* (47  $\mu$ F) power supply nets, 0805 component sizes were used. This is to limit the de-rated capacitance characteristic of such large rated ceramic capacitors realised in small SMD package footprints. For the smaller capacitors, 100 nF and below, 0603 or 0402 packages are suitable. Resistors in any package size is possible and accuracy rating of 1% is preferred. Considering the size of a keyboard, PCB space is usually not a concern except near the IC footprint where optimised component layout and proper fanout routing is required on all sensor lines.

### 5.3 PCB Layout Design

The reader is referred to fundamental layout guidelines discussed in [AZD004](#) and [AZD115](#). Supplementary guidance is provided in this section relevant to this application and product design example.

#### 5.3.1 Device placements in the key grid

The placement of each IQS9320 (and its related passives) are of the utmost importance. The key allocation mentioned in *section 3.2* should be considered again:

Each device was allocated a group of keys to sense (as coloured accordingly into four groups related to U1 to U4). All of the electronic components (except for LEDs) are placed on the bottom layer to allow a clean and unobstructed top layer available for key assembly to be flush with the PCB top surface. From the package pinout to allocation of a desired channel (sensor pair) assignment (as illustrated in Figure 5.4), the channels were assigned to keys in a clockwise order (anti-clockwise from the bottom layer / IC pinout perspective). For example starting with 'Esc' key-CH0, then key '1'-CH9, key '2'-CH1, key '3'-CH10 and so forth. This prevents unnecessary trace crossing and jumping with the need for additional vias to other layers causing suboptimal routing and loss of space in constrained areas. Figure 5.5 shows the complete channel assignment of all devices.

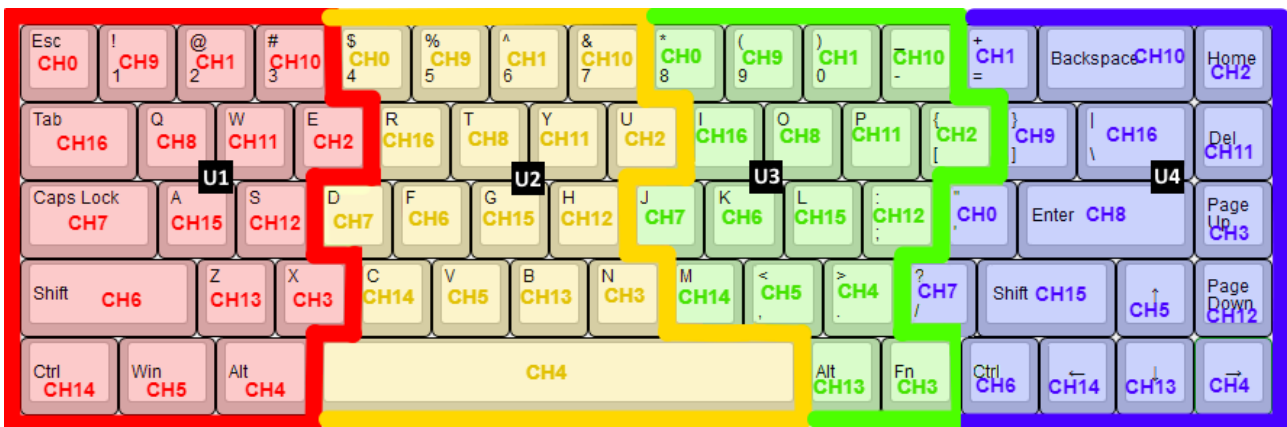


Figure 5.5: 65% - 68 Keys Inductive Keyboard Layout - IQS9320 Placement And Channel Assignments

The device of each group is placed central in position to all of the keys assigned to it. The devices U1, U2 and U3 was placed between the second and third rows because the bottom row has less keys and thus less density of routing. Each device occupies the space between four adjacent keys as this limits the available PCB area due to the cut-outs needed for each key. Device U4 is different with only 14 keys and can occupy the space underneath the 'Enter' key towards the right, alongside the 'Page Up' key, ensuring an equal distribution of its key's positions. The placement of devices should be considered carefully and various alterations of key and channel assignment schemes are possible, thus alternatives to the example showcased can be considered based on keyboard key amount, number of sensor devices and key-grid layout specifications.

#### 5.3.2 Power (VDD) and regulated (VREG) supply decoupling

As mentioned in the previous section the decoupling capacitors are crucial and need to be placed as close as possible to the IQS9320 package and routed optimally. Highlighted in Figure 5.6 below, the smaller (high frequency) decoupling 100 pF and then the 100 nF capacitors are placed closer before the larger 0805 capacitors for VDD (3V3) and VREG respectively. Each are terminated to the closest



common ground pour connection with a trace and in most instances an immediate via connection leading back to the VSS pin or tab/saddle underneath the IC.

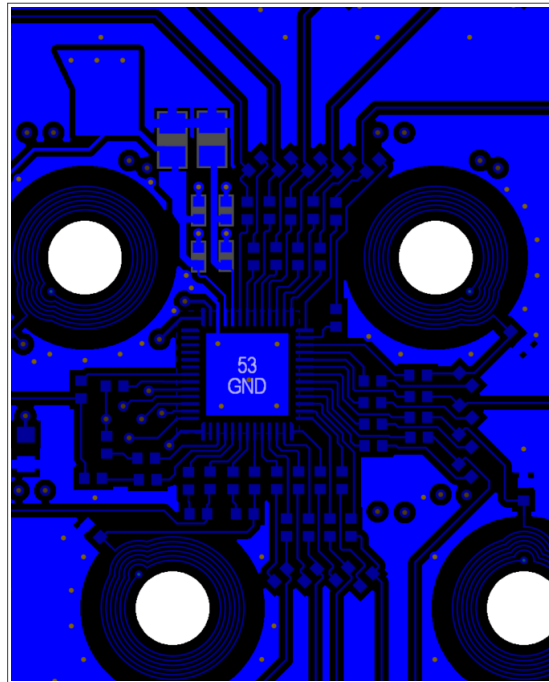


Figure 5.6: Bottom Layer Decoupling Component Placement And Routing

### 5.3.3 Sensor trace routing

Receiver (Rx) series resistors should be prioritised and placed closest to the IC package. Rx routing can enjoy preference before Tx traces however keeping them both short and pairs close to one another from their respective pins to their series passive components are an advised rule of thumb. The common connected sensor net trace (where ports were assigned for each key) should then extend to the key position following the shortest path possible to where the resonant LC tank (coil and parallel resonance capacitor) is located in the key grid. It is recommended to shield these lines by ensuring ground copper separation flowed-in between adjacent sensor traces fanning out from passives and using solid ground copper in layers above (and beneath if inner layers are used). Although this can add a minuscule amount of parasitic capacitance, this lumped capacitance will merely be added (in parallel) to the resonance capacitor for each coil. To simplify routing and restrict the resonance capacitor component size to the similar value for all coils, it is advised to start optimisation from the coil furthest away with the longest trace length. Rotation of each coil can ensure that the via connection point is located closest to where the trace leads back to the sensor IC to simplify routing and minimise trace lengths.

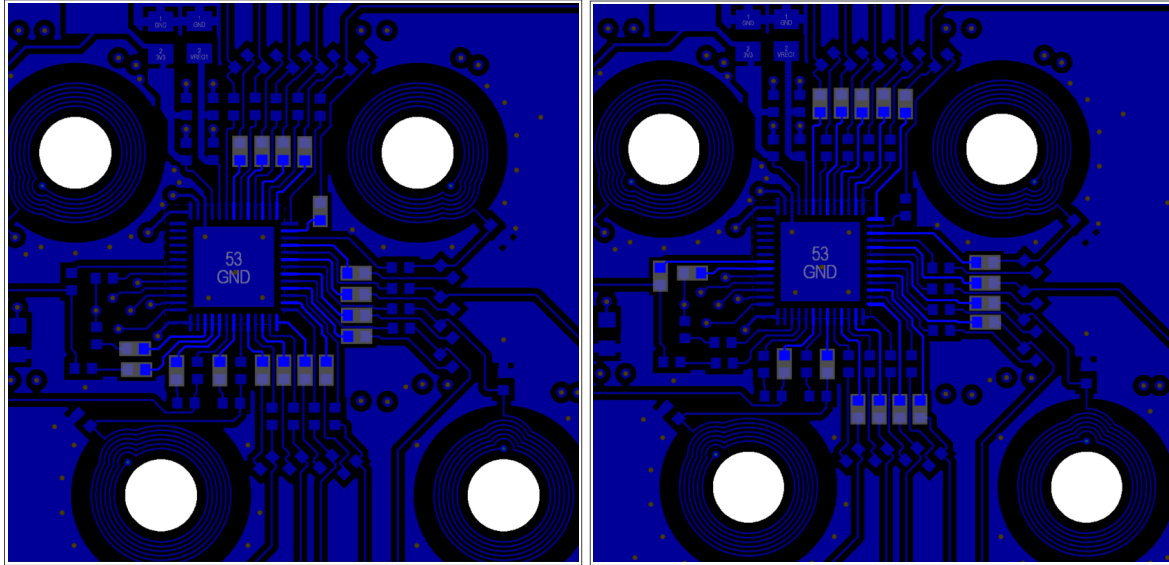


Figure 5.7: Bottom Layer Sensor Receiver (Rx) and Transmit (Tx) Trace Routing and Passives

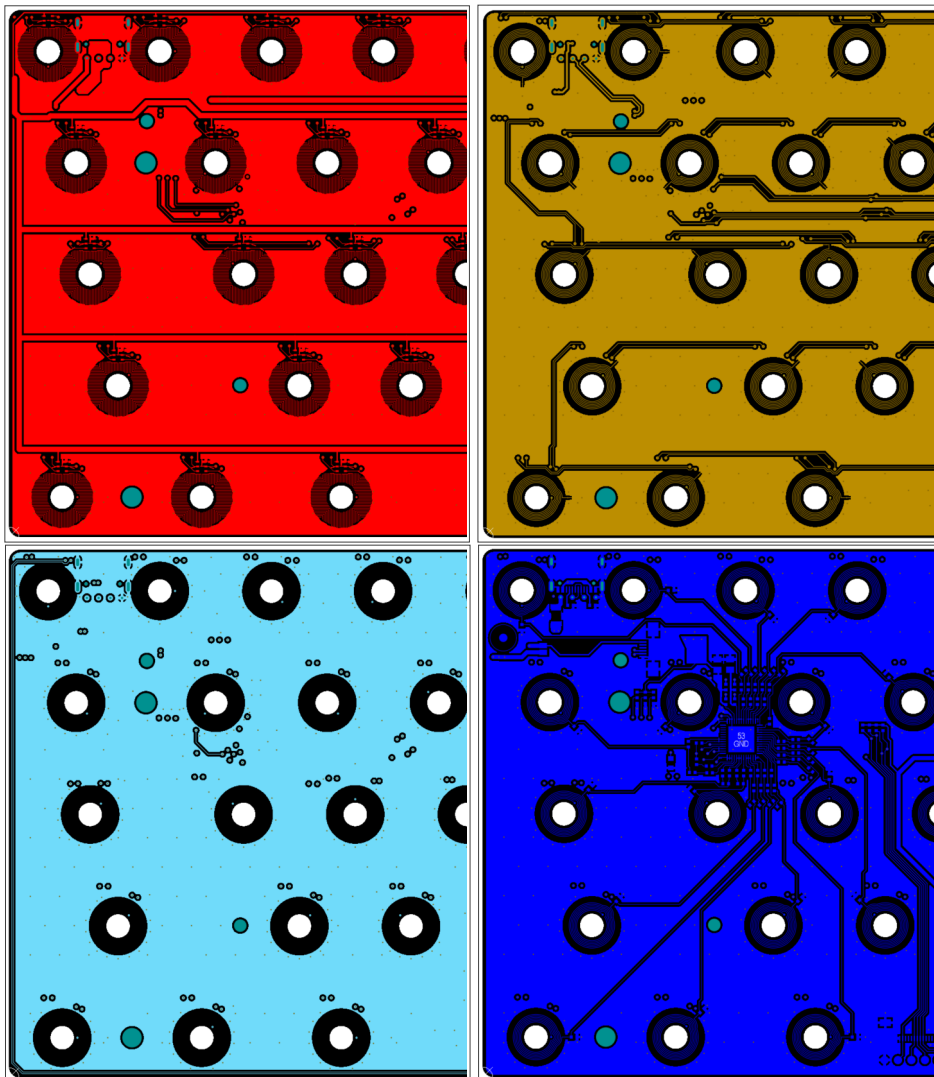


Figure 5.8: Top, In1, In2 And Bottom Layer Routing To Key-Coil Location Related To U1





### 5.3.4 Digital interface routing

Each sensor device has of a number of digital IO and communication (I<sup>2</sup>C) lines that needs to be connected to single FFC/FPC connector that is shared between devices. Best practise is to group these digital traces together and route alongside one another from each device. The top layer snippet on the left hand side, in Figure 5.8 above, shows and example of such a routing layout. This occupies minimal amount of space, doesn't interfere/cross over the coils and can be shielded by inner layers not to impact bottom layer sensor traces.

### 5.3.5 Coil design

The coil design can be simulated and optimised with the use of EM-/finite element analysis software packages. Application note [AZD115](#) provides first principle formulas to calculate the inductance of multi-layer coils and other characteristic properties of significance. Some graphical representation and tools/calculators are available online as freeware or free-to-use while some PCB design software offer such features or as tool extensions. The aim of using such simulation is to design a coil that fulfils the electrical and mechanical specifications to suit the IQS9320 sensor and the specific key design that will be used optimally. The inductance change can be simulated and the finer details related to loading and parasitic can be envisioned prior to prototype manufacturing and testing.

The design showcased in this example layout adheres to the PCB manufacturer's minimum trace width and -clearance constraints (0.127mm for both). The routed PCB copper-to-edge clearance needs to be more than 0.35mm while the targeted key's metal plunger/stud requires a hole of 4mm in diameter. Ultimately these dimensions constrains the coil inner diameter. A coil with an outer diameter of 7.87mm and an inner diameter of 5mm, featuring six windings on both IN1 and Bottom layers (1.2mm layer separation), results in a theoretical inductance of 0.903 μH. The table 5.2 below provides the featured multi-layer coil design attributes and resultant theoretical electrical characteristics that can be expected.

*Table 5.2: Coil Design Specifications And Resultant Characteristics*

Input specifications		Calculation output	
Coil design aspects	Specification	Coil properties	Characteristic
Coil shape	Circular	Inductance	0.903 μH
Turns per layer ( <i>n</i> )	6	Parasitic capacitance	2.591 pF
Outer diameter of coil ( <i>D<sub>out</sub></i> )	7.87mm	Parallel capacitance	82 pF
Inner diameter of coil ( <i>D<sub>in</sub></i> )	5.08mm	Resonating frequency	18.210 MHz
Layers ( <i>k</i> )	2	Excitation frequency	16 MHz
PCB (FR4) relative dielectric constant ( <i>ε<sub>rs</sub></i> )	4.4	Self inductance per layer	0.336 μH
Trace width ( <i>W</i> )	0.127mm	DC resistance	0.992 Ω
Spacing between traces ( <i>S</i> )	0.127mm	AC resistance (skin effect alone)	2.353 Ω
Copper plating thickness ( <i>t</i> )	35 μm	Skin depth	16 μm
Layer separation ( <i>x</i> )	1.2mm	Coil length ( <i>l<sub>g</sub></i> ) per layer	119.619mm

The ground pour around the coil was chosen to have a clearance of 1.5mm all around on all the layers except for a specific shielding pattern on the top layer. A single via is required for the multilayer coil, to feed the signal from the inner winding on bottom layer to the start of inner winding on the inner1 layer. This via should be of minimum dimensions with a small hole size of 0.2mm and 0.45mm angular ring diameter. This minimises the bulge of traces needed to encompass the via, in order to fulfil the design- and manufacturing rules and constraints. Ultimately this allows a smaller inner coil diameter





while reducing the coil coverage and optimising the fill ratio of plunger metal inside the coil core under similar inductances.

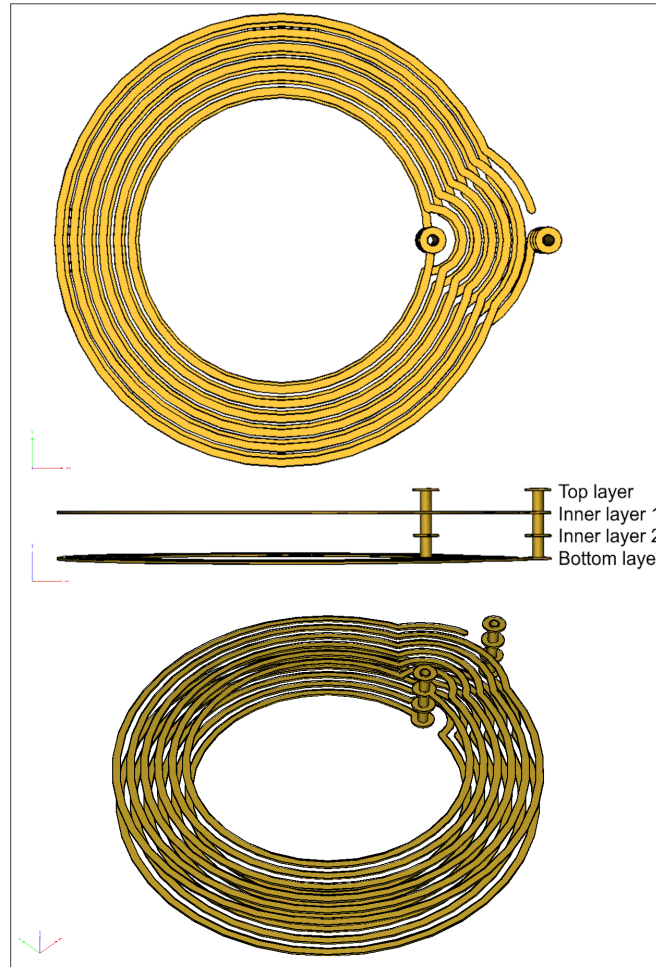


Figure 5.9: Computer-Aided Coil Design

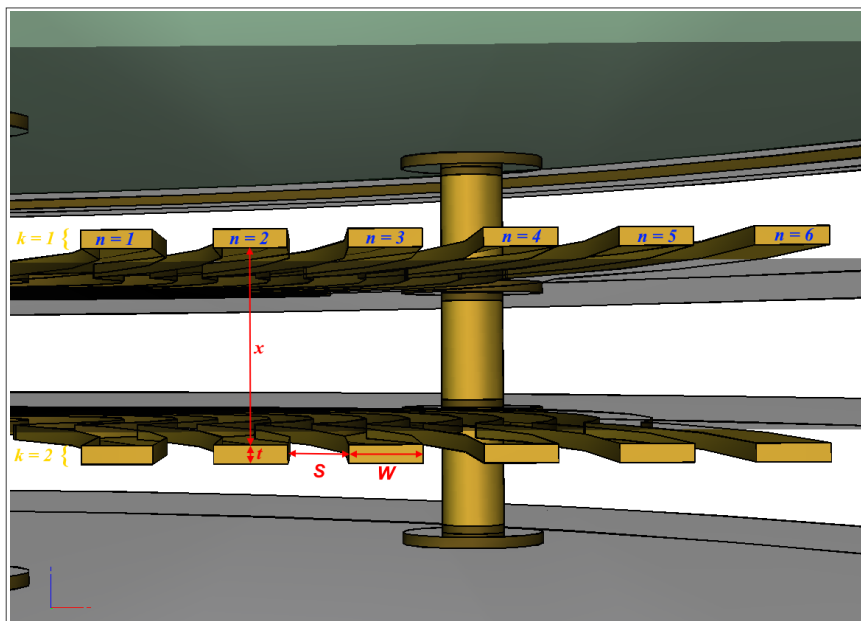


Figure 5.10: Sectional View Of Coil Trace And Dimensioning

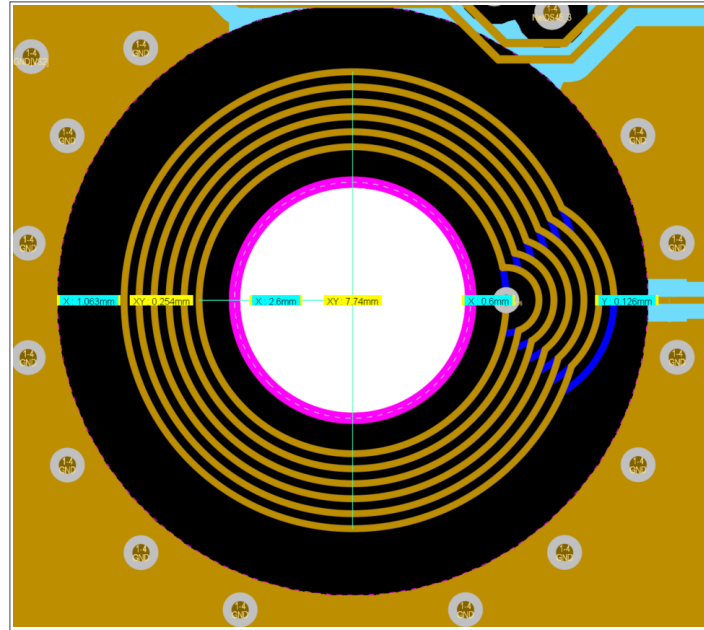


Figure 5.11: Inner Layer View Of PCB Coil Design with Dimensions

Figure 5.12 below shows the total layer stack-up for a specific coil. Here the shielding pattern on the top layer (in red) can be seen. Ground stubs with single connections are used to cover the coil, this is to prevent loops from forming while still shielding from the top layer. These shielding stubs are also of minimum trace width and clearance from one another or the signal vias and covers the entire coil plus some border. The ground pour is via stitched every ~2.5mm along the edge closest to the coil and evenly throughout the areas between adjacent keys.

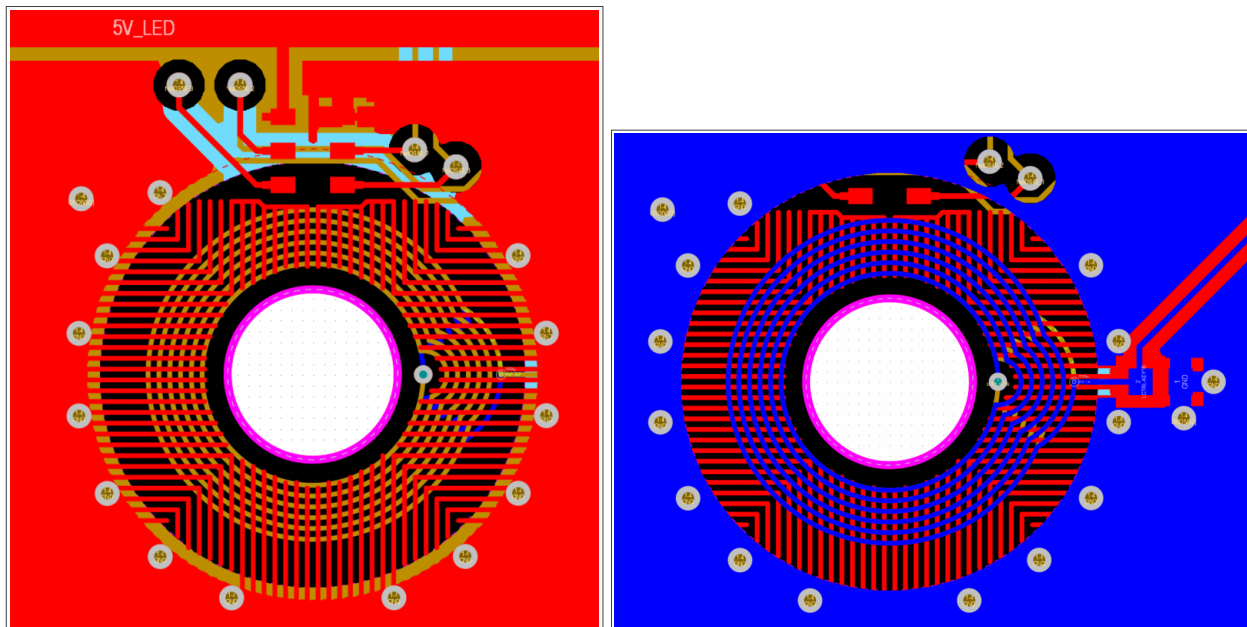


Figure 5.12: Top And Bottom Views Showing Coil Ground Shielding, -Pours, LED and Resonant Capacitor

### 5.3.6 Coil termination

Termination of the coil and resonance capacitor to ground is of importance. Each sensor has a unique (shortest) ground path leading back to the sensor device’s VSS pin or IC tab/saddle (where ground is common to sensor and IQS9320 power supply and both should be the same electrical connection). Ideally the path should be short, simple and direct using the minimum amount of vias and not required to circle around other coils or follow loops that may be effected from other high frequency EM noise or currents flowing irregularly through the same path. Doing this improves performance of sensors and prevents cross coupling noise between adjacent keys.

### 5.3.7 PCB-material, -layer stack up and -finishing

An FR-4 PCB (refer to Appendix B and C for design detail) which consists of four signal layers were used for the IQS9320, passive components, sensor coil and RGB LED routing. The complete layer stack-up results in a standard 1.6mm thick board which is structurally sound and stiff enough for general keyboard purposes.

#	Name	Type	Thickness	#	Thru 1:4
	Top Overlay	Overlay			
	Top Solder	Solder Mask	0.01mm		
1	Top Layer	Signal	0.035mm	1	
	Dielectric1	Core	0.2104mm		
2	IN1	Signal	0.0152mm	2	
	Dielectric 3	Prepreg	1.065mm		
3	IN2	Signal	0.0152mm	3	
	Dielectric 2	Core	0.2104mm		
4	Bottom Layer	Signal	0.035mm	4	
	Bottom Solder	Solder Mask	0.01mm		
	Bottom Overlay	Overlay			

*Figure 5.13: PCB Layer Stack-up And Through Hole Via Usage*

The first two (L1 to L2) and the last two layers (L3 to L4) are equally spaced but the core (dielectric 3 between L2 and L3) is five times thicker at roughly ~1 mm. Each copper layer is predominantly flooded with a common ground copper pour to prevent bow and twist. Provided holes and routed cut-outs on the PCB edge was designed to fit plastic support pillars and screw fastening locations with threaded holes once placed inside the plastic casing.

To save cost and manufacturing lead time all vias used on this 4-layer PCB was through hole (TH; as indicated above 'Thru1:4'). No blind or buried vias were needed and this simplifies the manufacturing process and reduces costs. A further reduction in cost can be acquired by using a plating finish such as HASL or OSP, albeit considering the trade-off for each to still meet production specifications and certifications as stipulated.

It is important to add fiducial (FID) markers at the appropriate location on the PCB. This round copper marker acts as a reference point for pick and place assembly machines. The FID markers are normally placed on the same layer as components and ideally as far as possible in opposite corners on the rectangular PCB to increase accuracy of automated placement.

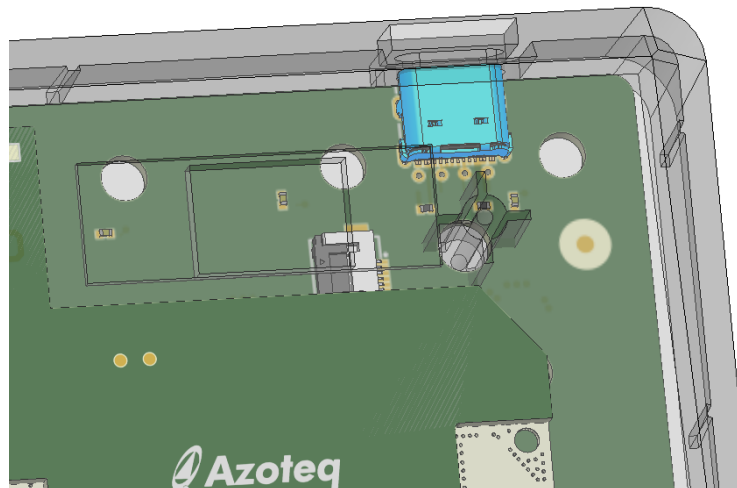


Figure 5.14: CAD Assembly Of PCBA Fitted Inside Case To Confirm Connector And Support Feature Alignment

The feasibility of designing a 2-layer PCB should consider the following implications and points of concern:

- > The coil shielding on the top-layer will not be possible.
  - Ingress protection tests against liquids would likely fail with level 0 rating (not protected).
  - Key frame, support brackets or other conductors would have more severe impact.
- > Generally routing will become more difficult, with more vias required and likely less than ideal EM compatibility and performance.
- > There might not be enough space to route the LED backlighting optimally, or the backlighting could potentially couple noise into the inductive sensors.
- > The coil inductance will change with a new layer separation distance ( $x$  = PCB core thickness).



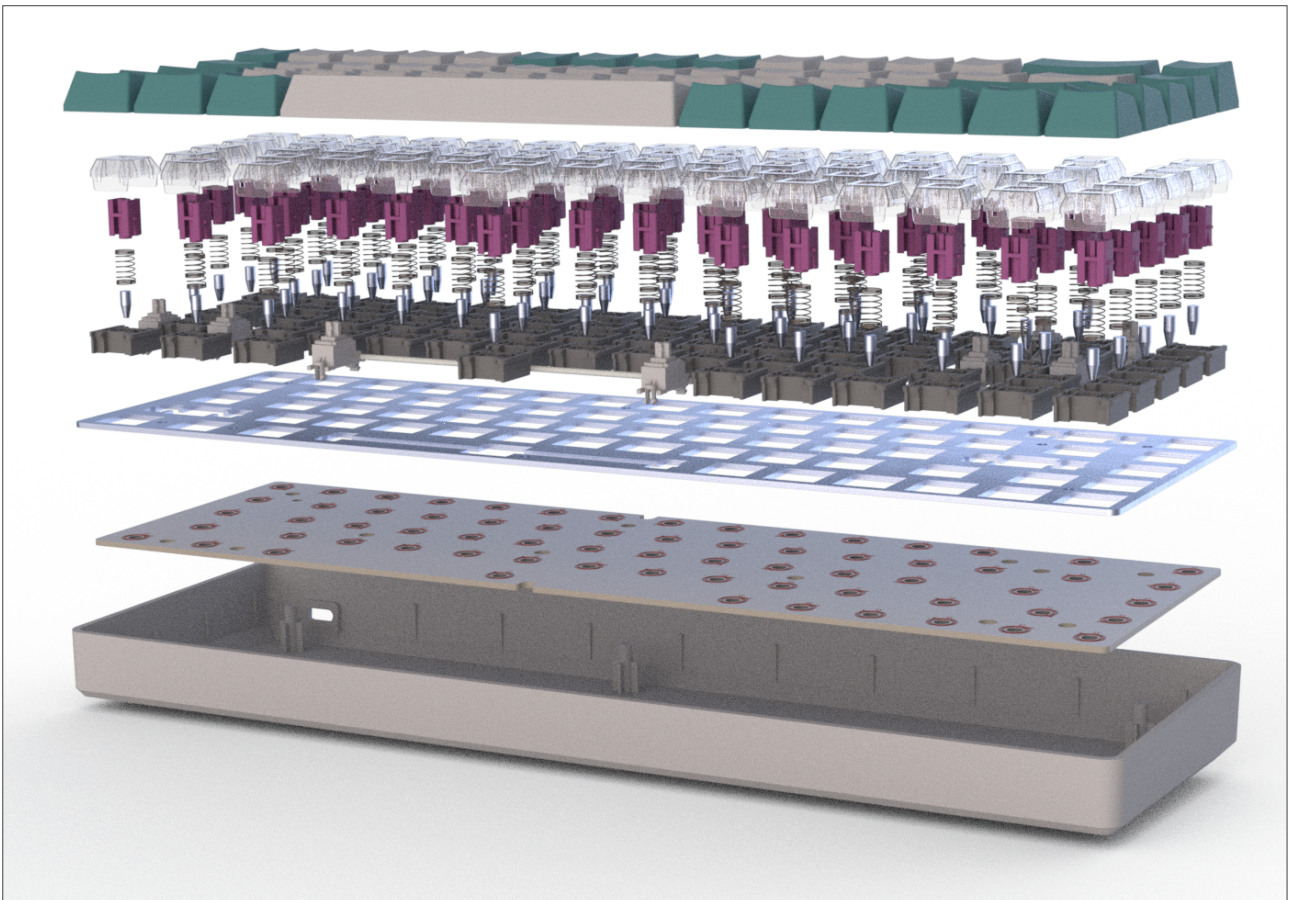
## 5.4 Mechanical Design

This section discusses topics regarding product mechanics and assembly.

### 5.4.1 Assembly

A keyboard assembly entails stacking/integrating the various components. These components include at least the following parts (in order from top to bottom):

- > Key caps
- > Keys, as a sub-assembly consisting of:
  - transparent top enclosure
  - stem
  - spring
  - metal plunger
  - bottom enclosure
- > Key frame (screw fastened)
  - Optional stand-off support / spacer inserts
- > Keyboard PCBA (IQS devices and key grid of sensors; also screw fastened)
  - FFC ribbon cable connection (if needed) to interface to a sub-assembled host PCBA
- > Host / Controller PCBA (can also be integrated onto the keyboard PCBA)
- > Bottom casing / enclosure



*Figure 5.15: Exploded Keyboard View: Full Stack-up Assembly*

Additional parts for more elaborate keyboard designs with added features/capabilities might expand





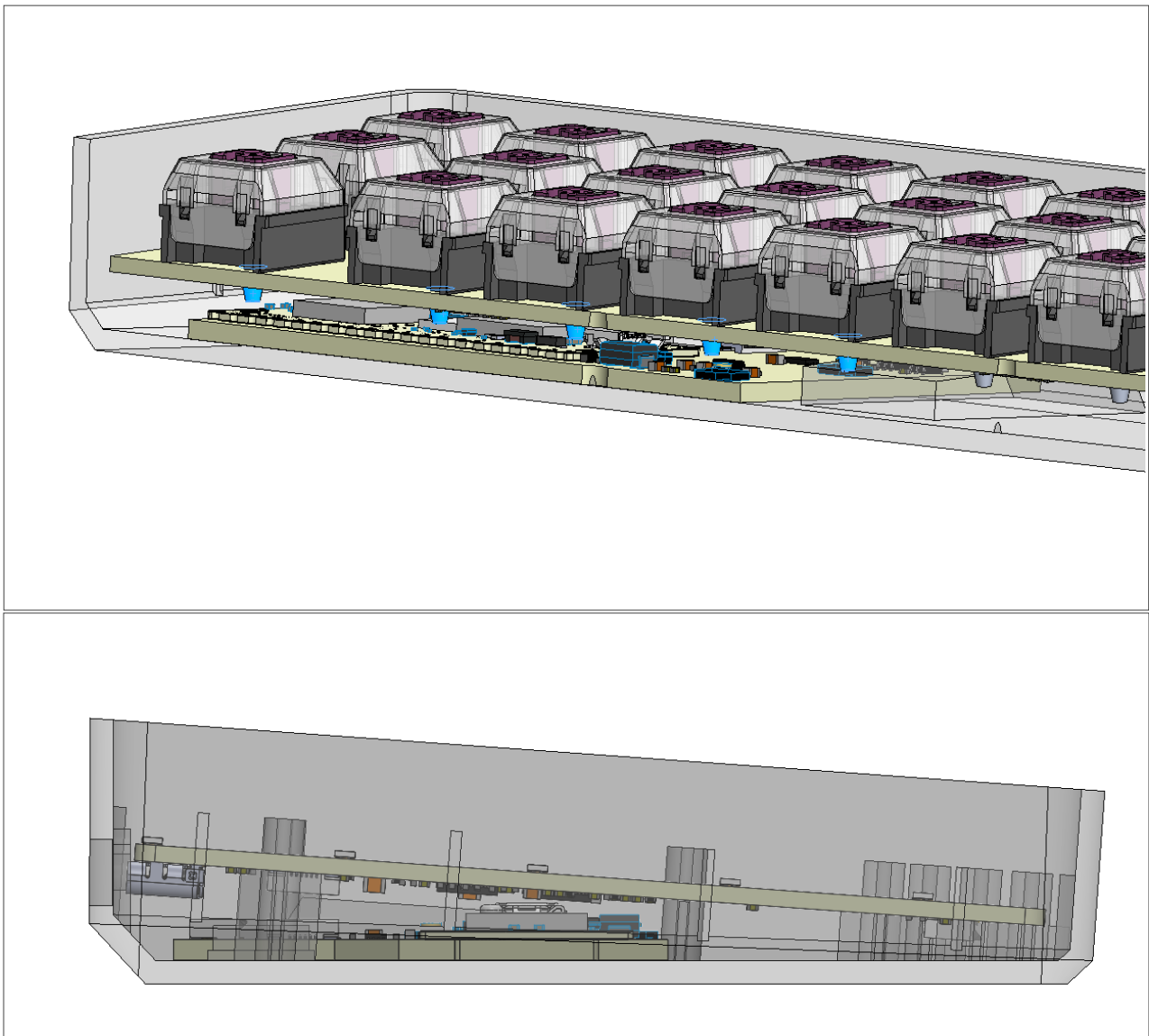
on the rudimentary list given above.

The assembly process should sensibly take place in the reverse order as listed i.e. from bottom (starting with the enclosure) to top (assembling key caps last).

#### 5.4.2 Housing / casing

The housing or external case design of keyboards may vary depending on the specific make and model. Keyboard manufacturers alter this based on aesthetics, customisability, user preference and ergonomic design goals.

The example design showcased was based on an existing keyboard enclosure that consists of a single plastic bottom case with walls on all sides. Integrated in the ABS moulded design of this enclosure are the necessary support pillars, holes and features to support the keyboard PCBA and key frame in place. The sectional view of CAD images illustrated in Figure 5.16 below shows some detail of this and its functionality to host the assembled parts. The enclosure should allow plungers to move freely and unobstructed.



*Figure 5.16: Sectional And Transparent Views Of PCBAs Within Keyboard Housing*

### 5.4.3 Mechanical movement and its effects

Keys should be properly seated and installed to conformity. Mechanical movement of the key part itself (in respect to the PCB or dedicated sensor coil) will directly result in a deviation from typical plunger actuation path and depth and result in deviation of signal and desired configured actuation point. Key stem wobble under an applied force is also non-ideal and should be prevented. The springs used inside keys should not show any disturbance (irregular jumps/offset) in signal when compressed and making contact from one winding to the next on itself. Key manufacturers can opt to use springs which are coated with a thin non-conductive isolation anodised or coated onto spring surfaces.

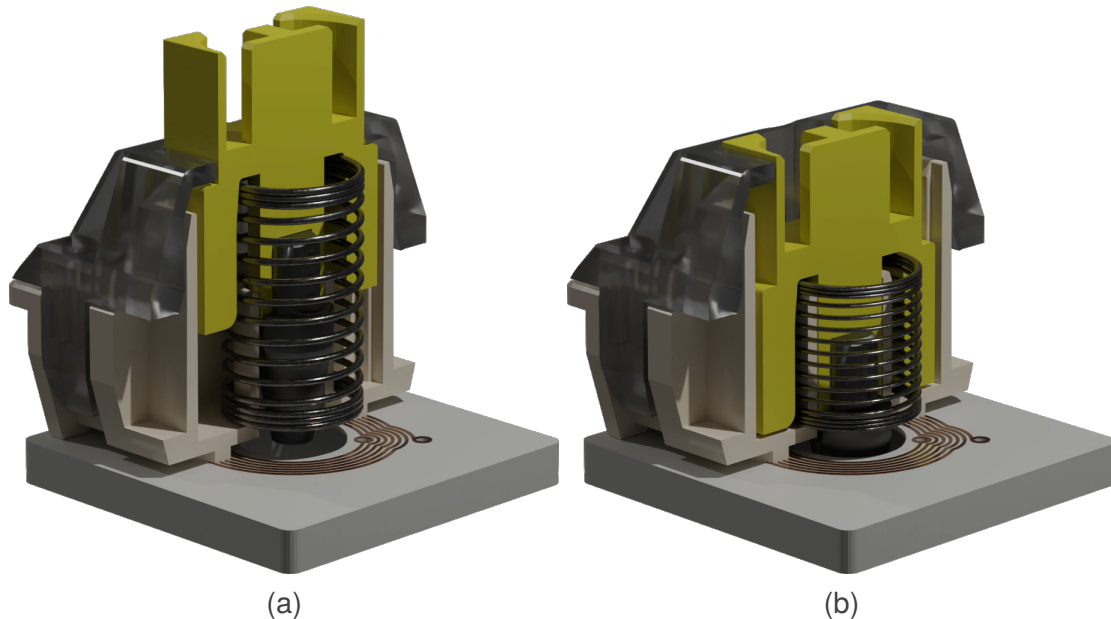


Figure 5.17: Sectional View Of Key Mechanic Positions For (a) Relaxed And (b) Pressed Actuation

### 5.4.4 Key frame (overlay) design

Conductive materials like metals (or any alloys) near coils reduces their inductance, and resultantly changes the impedance response of the sensor (at a fixed operating frequency). During sensor design and evaluation such conductive elements (like key frames, overlays, inlays etc.) should be installed and accounted for by having the hardware state as close as possible to a final product assembly.

If a metal key frame will be used, it is crucial to design ample structural support. A metal key frame moving slightly towards the PCB will show a small but similar change in inductive measured counts likewise to a key press. The top layer shielding of coils helps to minimise this effect, but cannot entirely prevent this. Although this problem can be solved by using a key frame from non-conductive material, durability and the appealing preference of a metallic look and feel finish on premium products should be possible with proper mechanical design practises.

### 5.4.5 Stand-off supports and spacers

To limit mechanical movement between the metal key-frame and the PCB (hosting the coils in inner layers), plastic stand-off support inserts were used as indicated in Figure 5.18. The four stand-off supports were distributed in the areas where force exerted on the keys and transferred to the key frame may result in bending of the metal frame at areas further away from the screw fastened pillar supports from the casing.

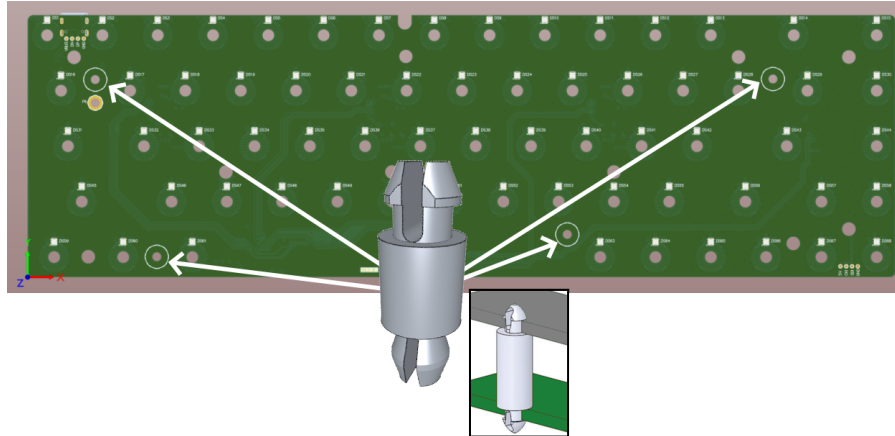


Figure 5.18: PCB And Key-frame Stand-off Support (M3/3mm dia.) To Minimize Deflection

#### 5.4.6 Metal bracket key braces

Metallic bended wire bracket joints usually feature as support braces for the larger keys that are wider such as space bar, caps lock and the enter key. These bracket joints have an influence on the inductive sensor performance due to them passing close by these keys' coils once assembled and this hinders magnetic fields. The contributed affect is usually accounted for internally by the IQS device during calibration, but the operating point is still distinguishable to other keys. In the case of the enter key it was even decided to increase the series Tx resistance (also where CTx1 was utilised) to 1 k $\Omega$  to improve the Q value of this key suffering from both side effects and less sensitivity than the rest.



Figure 5.19: Space Bar Metal Bracket Joint Support

#### 5.4.7 Connectors and cables

It is common practise in keyboard design to use FFC ribbon cables of multiple circuits (e.g. 30 pins in this design) to interface all required power and digital connections to host or sub controller system. Connector placement should be considered for ribbon orientation, connection, insertion and if needed folding.



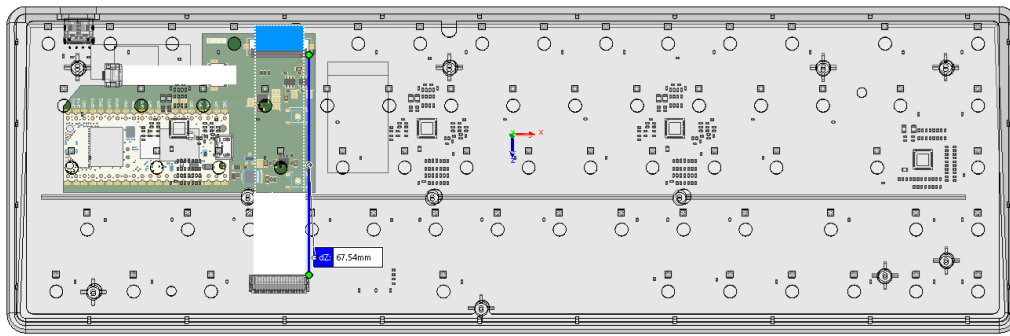


Figure 5.20: FFC Ribbon Cable Connections

It is recommended that IQS sensor devices are always located on the same circuit substrate as the coils that they will sense. Transferring Rx and Tx sensor lines through FFC/FPC/board-to-board connectors or any wired option is not ideal as these traces are extremely sensitive to any electrical and mechanical interference.

## 5.5 Manufacturing

Manufacturing requires a set of finalised manufacturing files which may include the following (or more):

- › BOM - document with part numbers, ratings and tolerances, sourcing and alternative details.
- › CAD - test points for jig, connector placement, adhesive, key frame or casing DXF files.
- › PCB - Gerber files, drill drawings, pdf plots and pick and place files.
- › PCB assembly instructions - Part handling, preparation, SMT and re-flow procedures, hand soldering.
- › Product assembly instructions - Sub- and product assemblies (keys, key frame, casing, battery etc.).

## 5.6 IC Setup

Azoteq provides a USB dongle (DS220) and a GUI to assist designers in finding configuration settings for each IQS9320 and associated hardware. Please refer to the [IQS9320 GUI Setup Guide](#) for a detail description and step-by-step guidance to configure the IQS9320. The result of this procedure is a h-file containing settings for each IC. The settings should be written by the master MCU to the IQS devices after each power cycle.



## 6 Design Verification

### 6.1 Keyboard layout and number of keys

65% ANSI keyboard implemented with 4 IQS9320 on a 4 layer FR4 PCBA, (refer to Appendix B for more info).

### 6.2 Key Switch Characteristics

From Figure 6.1, the response of the key approximates a linear function over the travel distance up to 3.80mm and the earliest activation point can be set at 0.30mm. At this distance, the Normalized Delta value is 2 times the average channel noise level.

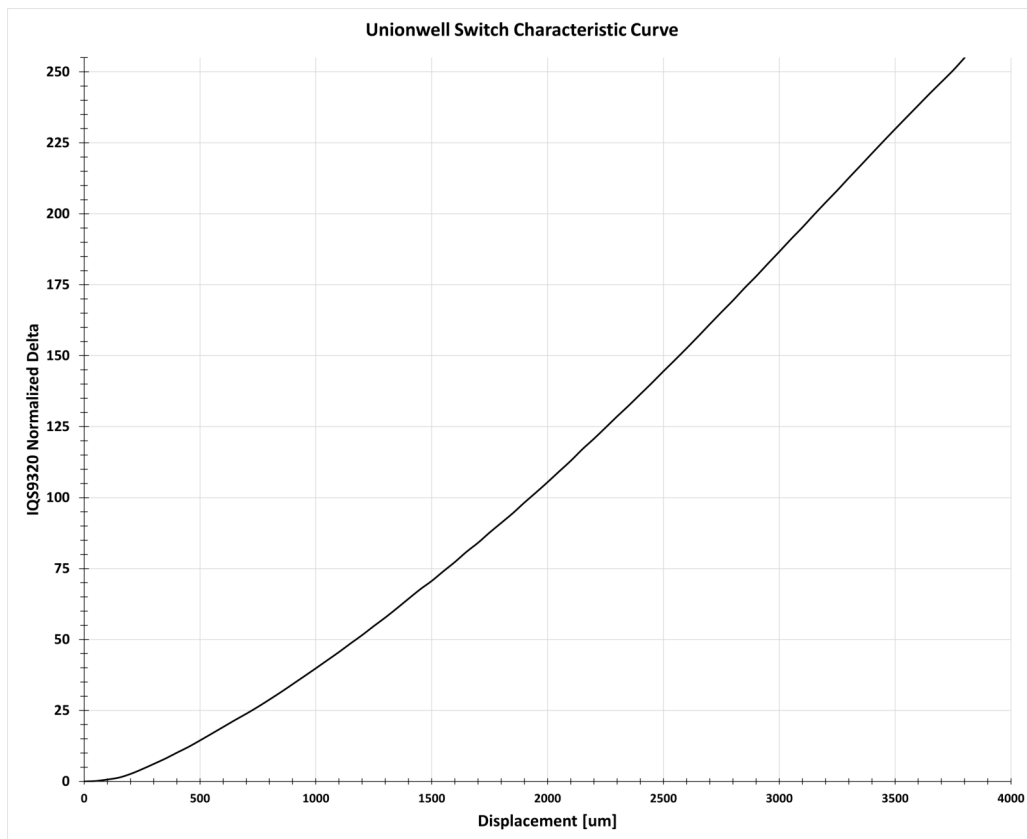


Figure 6.1: Unionwell Key Switch Response

A sample size of 30 Unionwell keys was characterized to provide data on the response variation across multiple keys. Figure 6.2 shows the lower limit, mean and upper limit response curves for the key samples. The mean response is considered to be the expected reference characteristic curve for a given Unionwell key and the lower and upper limit curves show the limits of the deviation from the reference.

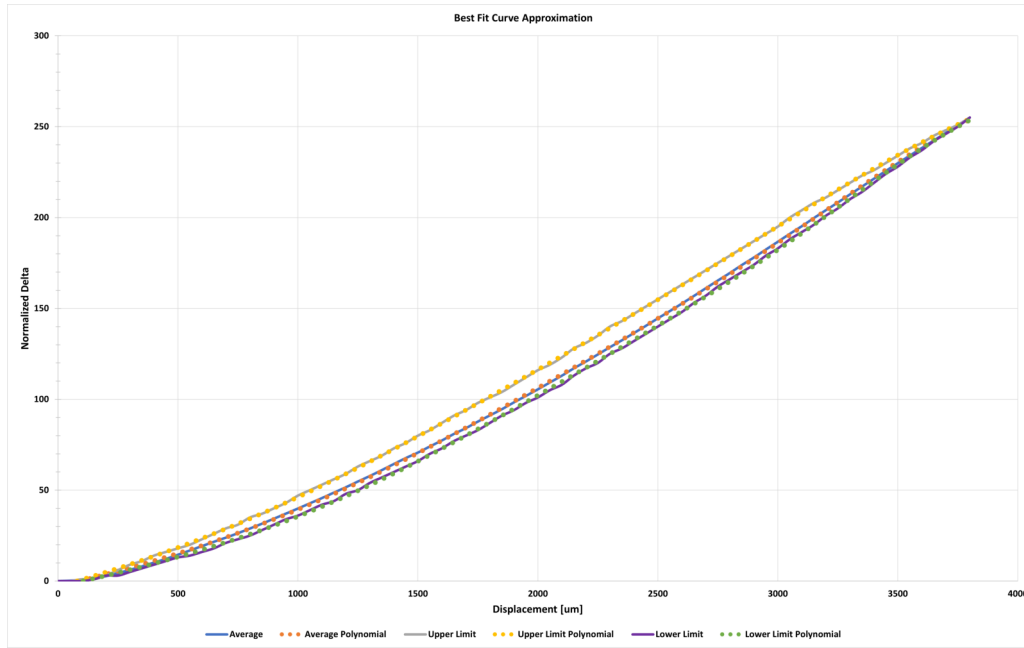


Figure 6.2: Characteristic curve response distribution

The measure response curves can be approximated by 5<sup>th</sup> order polynomials provided in Table 6.1:

Curve	$x^5$	$x^4$	$x^3$	$x^2$	$x^1$	$x^0$
Upper Limit	$6.496 \times 10^{-9}$	$-4 \times 10^{-6}$	$1.19 \times 10^{-3}$	-0.166	25.455	80.329
Average	$8.719 \times 10^{-9}$	$-6 \times 10^{-6}$	$1.68 \times 10^{-3}$	-0.232	29.935	93.708
Lower Limit	$11.831 \times 10^{-9}$	$-8 \times 10^{-6}$	$2.27 \times 10^{-3}$	-0.303	33.451	104.75

Table 6.1: 5<sup>th</sup> order polynomial curve approximation

The accuracy of the key is computed from the difference between the upper/lower limits curve and the average curve over the travel range of the key. For the sample set of keys, the accuracy is found to be within 140um.

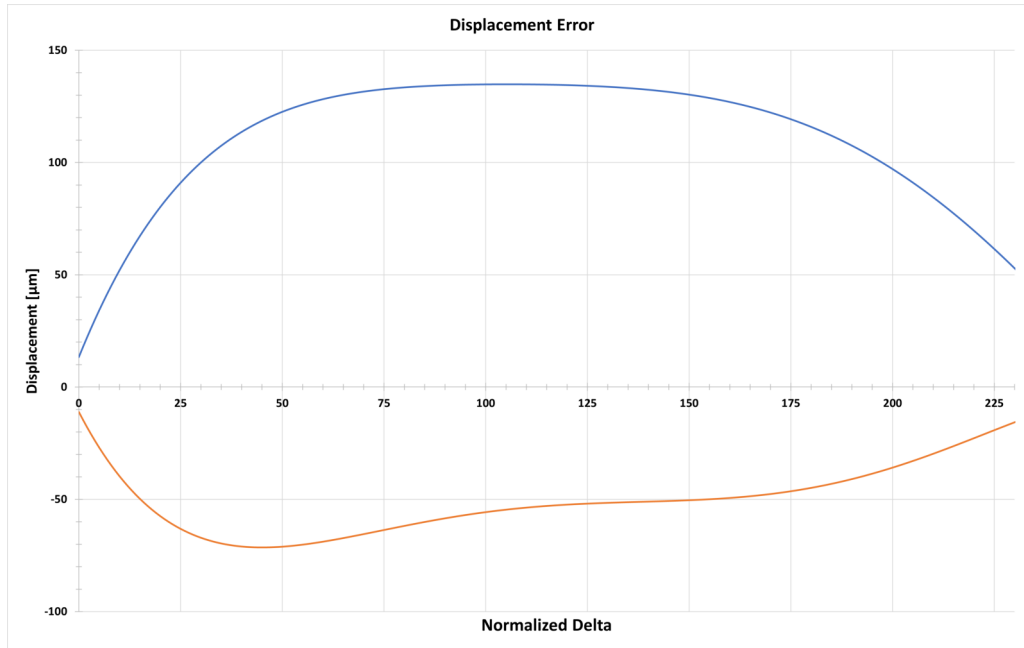


Figure 6.3: Accuracy over key travel distance

### 6.3 Key Switch Configuration

Each channel has an 8-bit register that can be used to configure the key as a discrete switch with a single actuation point or an analog switch with up to 255 levels. Each channel output value (Normalized Delta) can be read from IQS9320 register address `0x100E` to `0x1021`. Register addresses `0x30F0` to `0x3103` (activation thresholds) define the channel output level at which the activation flags in registers `0x100A` to `0x100D` are set.

Figure 6.4 shows Key0 and Key1 with activation thresholds of 50 and 100 respectively. The keys are displaced by the same amount such that the output levels of both keys are just above 50. Only Key0 is activated.

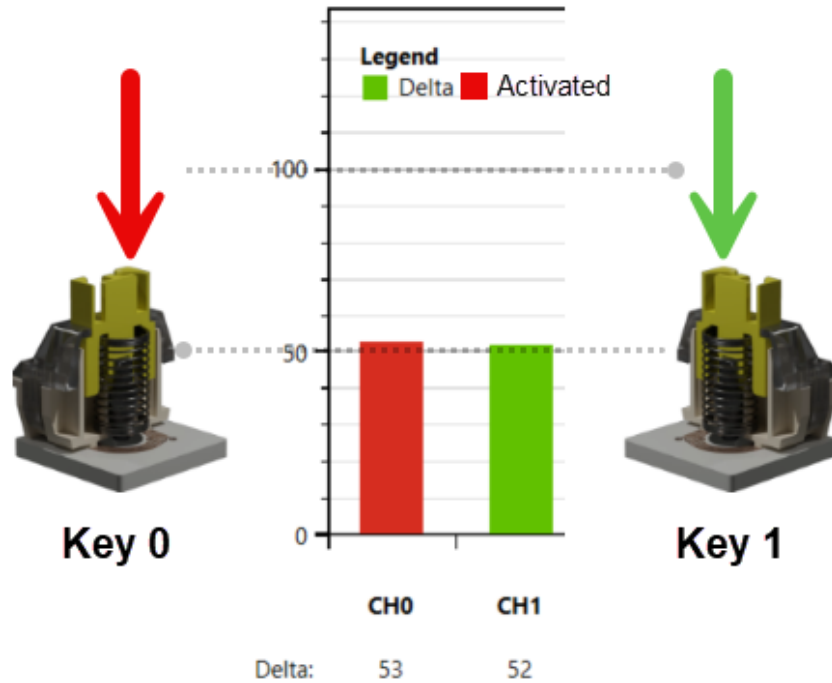


Figure 6.4: Key0 active and Key1 not active

Figure 6.5 shows the keys displaced further such that the output levels of both keys are just above 100. Both Key0 and Key1 are activated in this case.

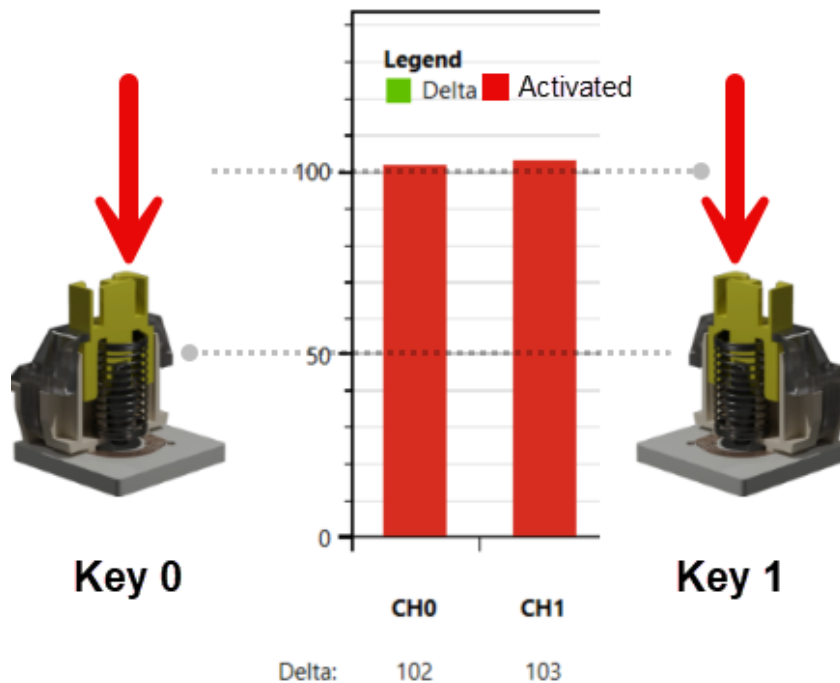


Figure 6.5: Key0 and Key active

Table 6.2 shows the TriggerMax™ functionality, for a key with a normalized actuation level delta of 100. TriggerMax™ allows for multiple key activations without returning to the initial actuation point.



9 Key State	Normalised Delta Value	Key State
Pressed below threshold		Non-Active
Pressed above threshold		Active
Released above threshold	 Delta: 132	Non-Active
Re-pressed above threshold	 Delta: 154	Active

Table 6.2: TriggerMax™ Functionality

## 6.4 Channel sampling and polling rate

Figure 6.6 and Figure 6.7 show the signal at the Tx pin of a given channel when none of the keys are pressed and when all the keys are fully pressed respectively. For both scenarios, the channel



sampling rate is less than 1ms.

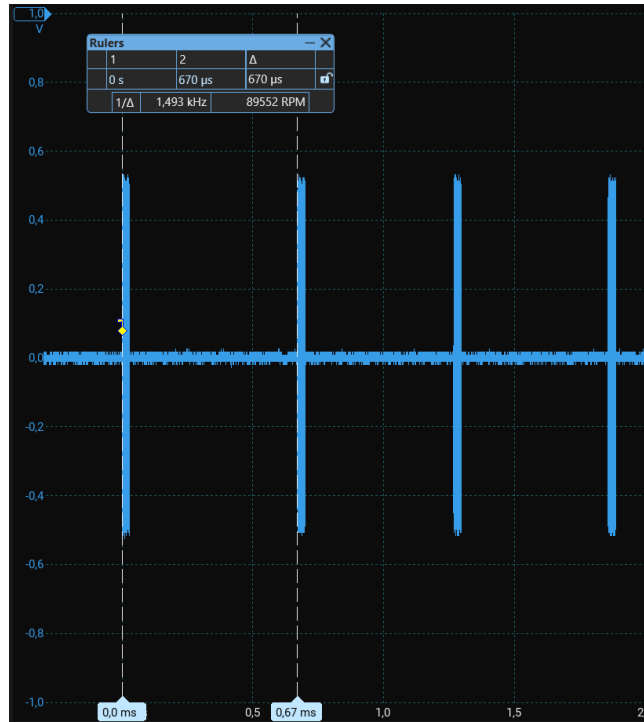


Figure 6.6: 670us Tx pin sampling rate no active channels

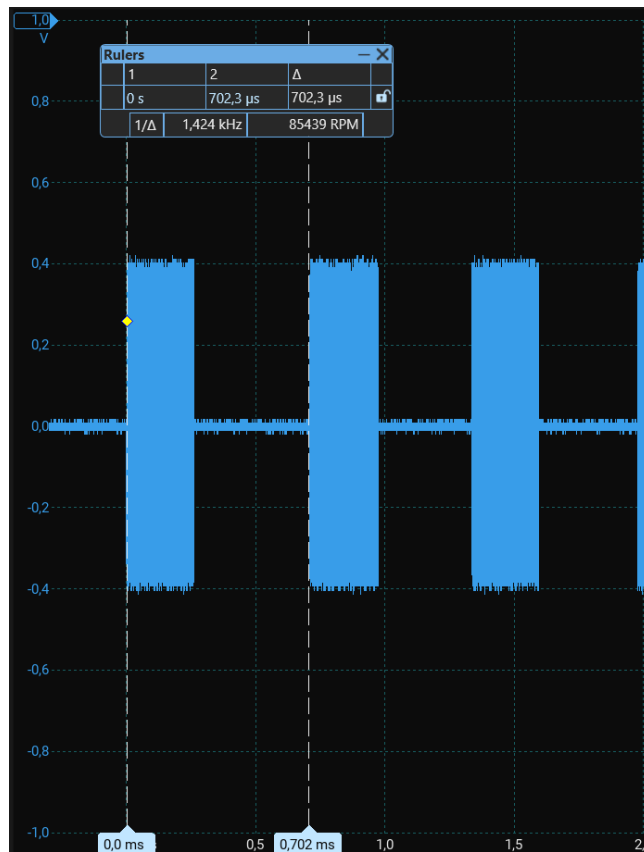


Figure 6.7: 702us Tx pin sampling rate all active channels



The time required to read the activation status flags for a single IQS9320 device is 0.1845ms as shown in Figure 6.8. For all 4 IQS9320 devices, the activation status flags can be read within 1ms as shown in Figure 6.9.



Figure 6.8: I2C activation flag read for single IQS9320 devices

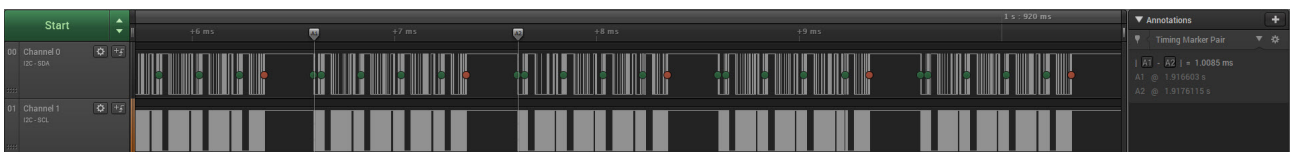


Figure 6.9: I2C activation flag read for all 4 IQS9320 devices

## 6.5 Ingress Protection Rating - Liquid

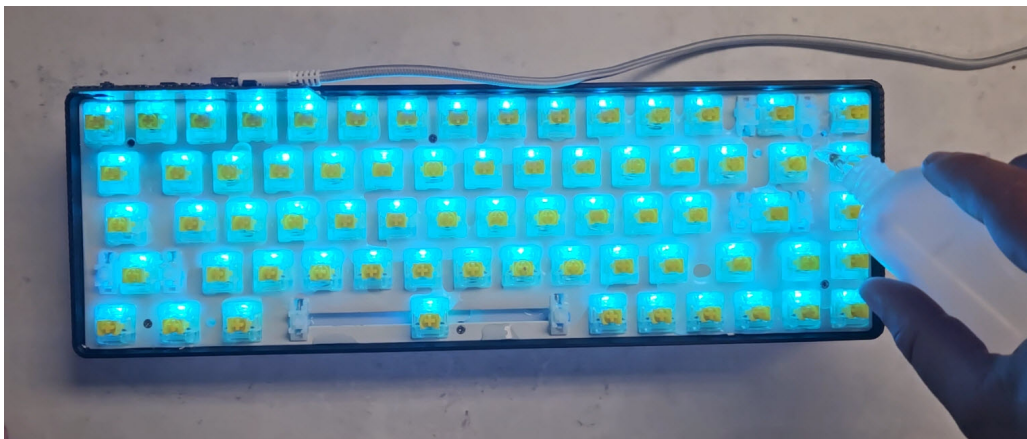


Figure 6.10: Water Ingress Protection Test Setup

The liquid IP rating test procedure is defined as follows:

- Make sure the bottom cover of the keyboard has drain holes to avoid the pooling of water on the bottom layer of the PCB.
- Set the activation level for each key to the lowest level at 0.30mm.
- Pour 100ml of water evenly along the entire length of the keyboard.
- Without pressing any of the keys, tilt the keyboard assembly 60° in the front, back, left and right directions.
- Observe for any false activations of the keys.
- If no false activations are observed, press all the keys and confirm functionality.
- If false activations are observed, power cycle the keyboard and test each key for functionality.
- Power off the device, open the keyboard assembly and air dry for at least 45 minutes.
- Power on the device and press all the keys to confirm functionality.





Table 6.3: Liquid Ingress Protection Test Results

Test Step	False Activation	Key Functionality
Pour 100ml of water and tilt assembly 60° front, back, left and right	No	Full key functionality
Power cycle keyboard while wet and test for functionality	No	Full key functionality
Air dry keyboard assembly and test for functionality	No	Full key functionality

Keyboard assembly passes Class A IPx2 liquid ingress protection as described in Table 6.4.

Table 6.4: Liquid Ingress Protection Classification

Class	Description
A	Keyboard is fully functional for the duration of the test.
B	Keyboard loses functionality when wet and recovers once dry.
C	Keyboard loses functionality when wet and does not recover when dry.

## 6.6 Inductive Proximity Interference

The inductive proximity interference test procedure is defined as follows:

- > Remove the keyboard top and bottom casing to access the PCB and key assembly.
- > Place interfering material and plastic spacer with thickness  $\frac{D_{out}}{2} = 4mm$  on flat surface.
- > Set the activation threshold for each key to the lowest level at 0.30mm.
- > Place PCB and key assembly directly over the interfering material and plastic spacer.
- > Observe the keyboard for any false key activations.
- > Repeat the test for a 2mm spacer.

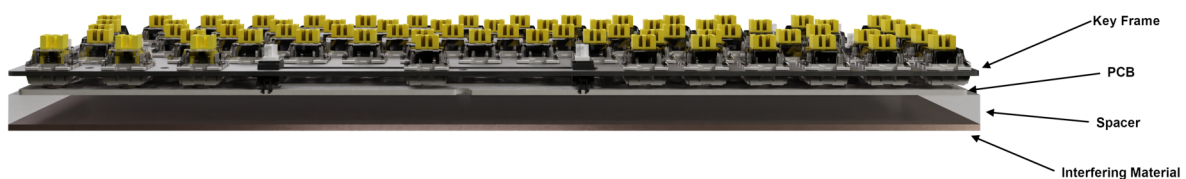


Figure 6.11: Inductive proximity immunity test

*Table 6.5: Inductive Proximity Immunity Test*

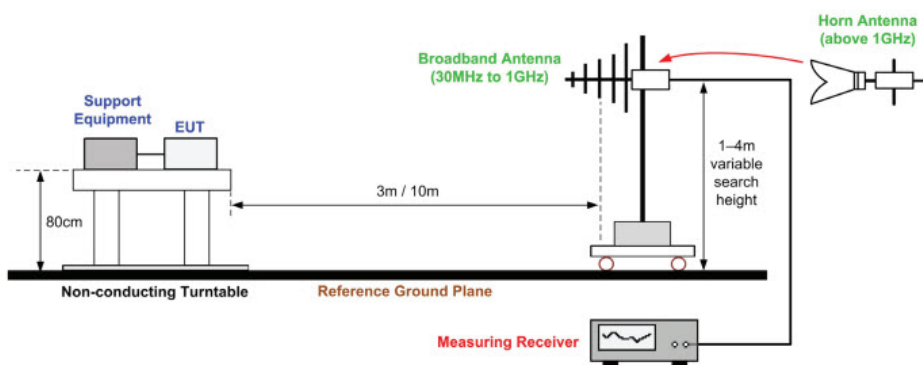
Interfering Material	Spacer Thickness	False Activation
Copper	2mm	Yes
	4mm	No
Stainless Steel	2mm	Yes
	4mm	No
Ferrite Sheet	2mm	Yes
	4mm	No
Permanent Magnet	2mm	Yes
	4mm	No

## 6.7 EMC Pre-Compliance

### 6.7.1 Radiated Emissions

The radiated emissions test procedure as defined in the *CISPR22: SANS 222 (2009) / CISPR22 (2008) 'Information technology equipment - Radio disturbance characteristic - Limits and methods of measurement standards'* is defined as follows:

- > Test is performed in a room without RF absorption material and includes a horizontal reference metallic ground plane.
- > EUT and support equipment are placed on an electrically insulated turn table.
- > Antenna mounted on an adjustable tower is placed 3m away from EUT.
- > A peak detector pre-scan is performed on the spectrum analyzer to find the vertical antenna height with the strongest signal. This is done for both vertical and horizontal antenna polarizations.
- > The EUT is also rotated on the turn table from 0 to 360° to find the strongest signal due to antenna-EUT azimuth.
- > For the specified antenna height and antenna EUT azimuth a peak detection scan is carried out over the specified frequency range from 30MHz to 300MHz.



*Figure 6.12: Radiated emissions test setup*

The EUT passed the radiated emissions test with the emissions levels below the limit line over the frequency range.

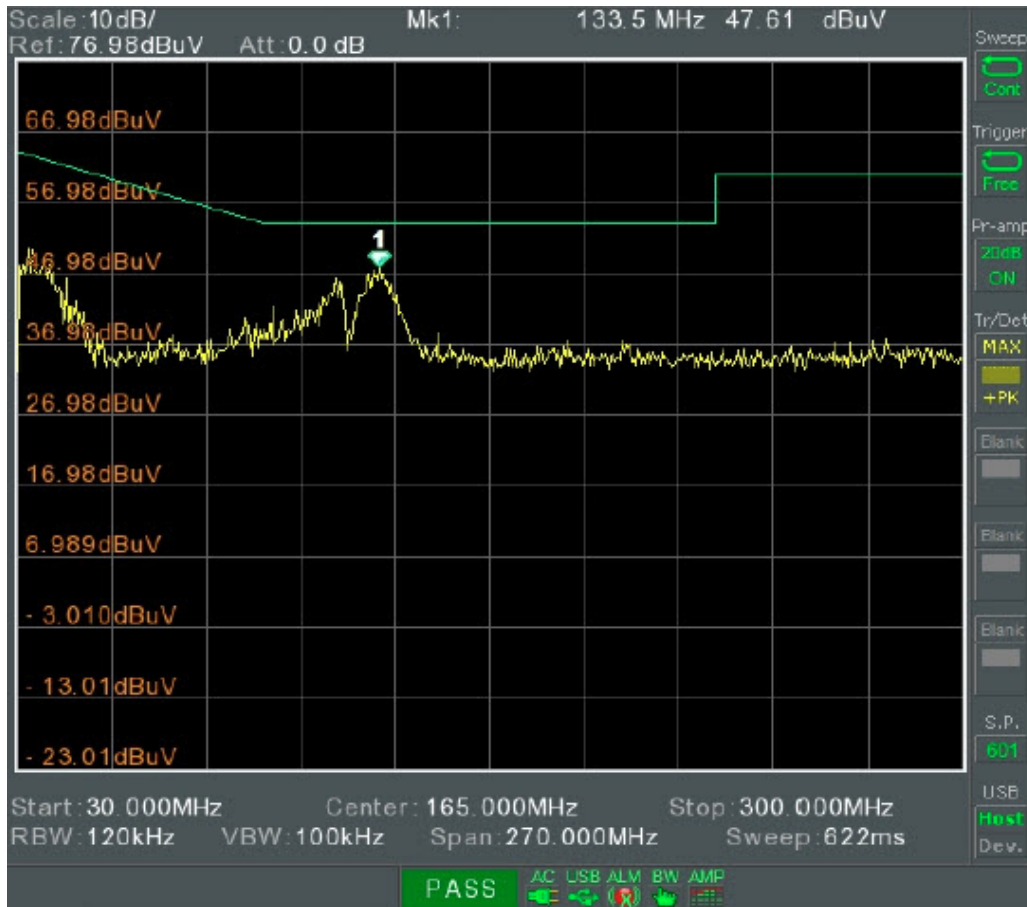


Figure 6.13: Radiated emissions peak detector

## 6.7.2 Conducted Emissions

The conducted emissions test procedure as defined in the *CISPR11* and *CISPR15* standards is defined as follows:

- > EUT and support equipment are placed on an electrically insulated turn table.
- > Place EUT on an electrically insulated table at a height of 80cm.
- > Power EUT via LISN.
- > With no input connections to the analyzer measure the open port noise floor. Ensure levels are low and the trace is smooth.
- > Connect spectrum analyzer to RF port of LISN using coaxial cable. An attenuator and transient limiter are placed in series to protect the spectrum analyzer.
- > Measure the conducted emissions from EUT in the frequency range 150kHz to 30MHz using the CISPR11 QP class B limit line.

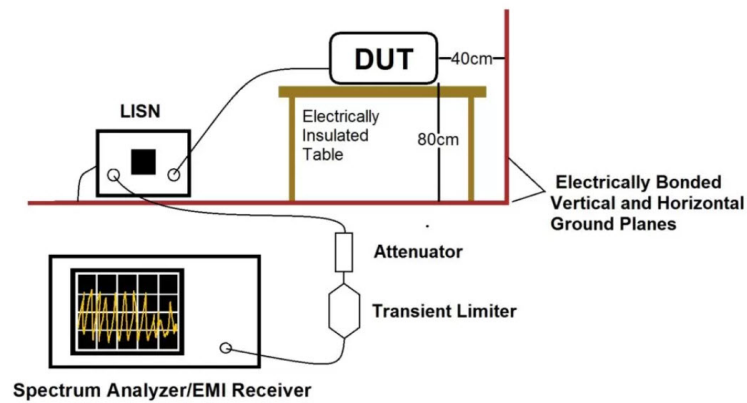


Figure 6.14: Conducted emissions test setup

EUT passed the conducted emissions test with the emissions level below the limit line over the frequency range.

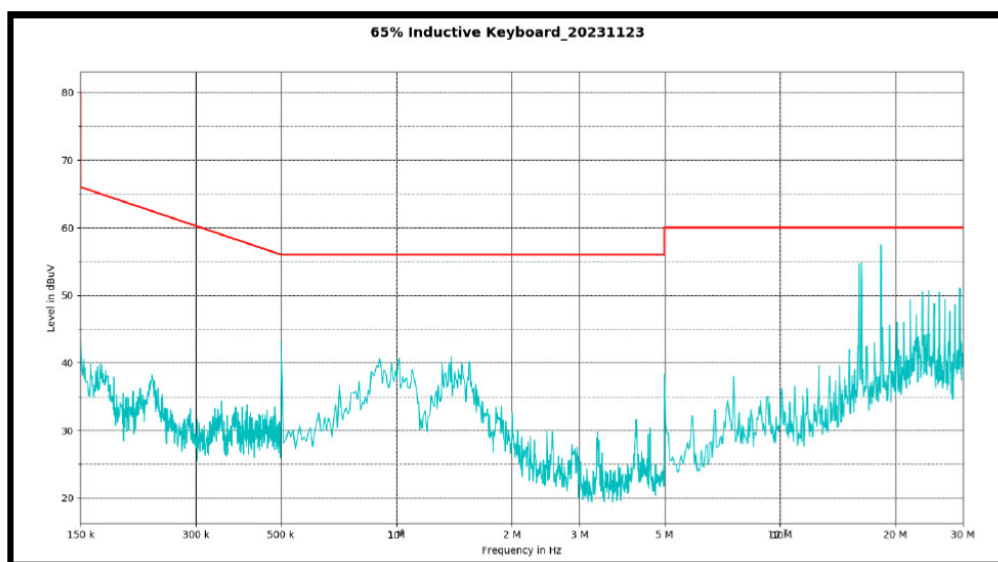


Figure 6.15: Conducted emissions quasi peak detector CSIPR11 class B limit

### 6.7.3 Radiated Immunity

The radiated immunity test procedure as defined in the *IEC 61000-4-3: Electromagnetic compatibility (EMC): Part 4-3: Testing and measurement techniques - Radiated, radiofrequency, electromagnetic field immunity test* standard is defined as follows:

- > Test is performed in a room without RF absorption material, horizontal and vertical reference metallic ground plane.
- > EUT and support equipment are placed on a non-conductive table at a height of 80cm.
- > Electrically insulated polystyrene standoffs with a height of 15cm are placed between EUT and the tabletop.
- > EUT and supporting equipment are powered through a filtered AC power outlet.
- > Using a field generator, EUT is exposed to EM radiation in the range 400MHz to 4GHz and filed strengths 1V/m,3V/m, 10V/m, 30V/m.

- > EM radiation exposure is measured using the isotropic field receiver/sensor.
- > The EUT is tested for normal functionality while exposed to EM radiation.

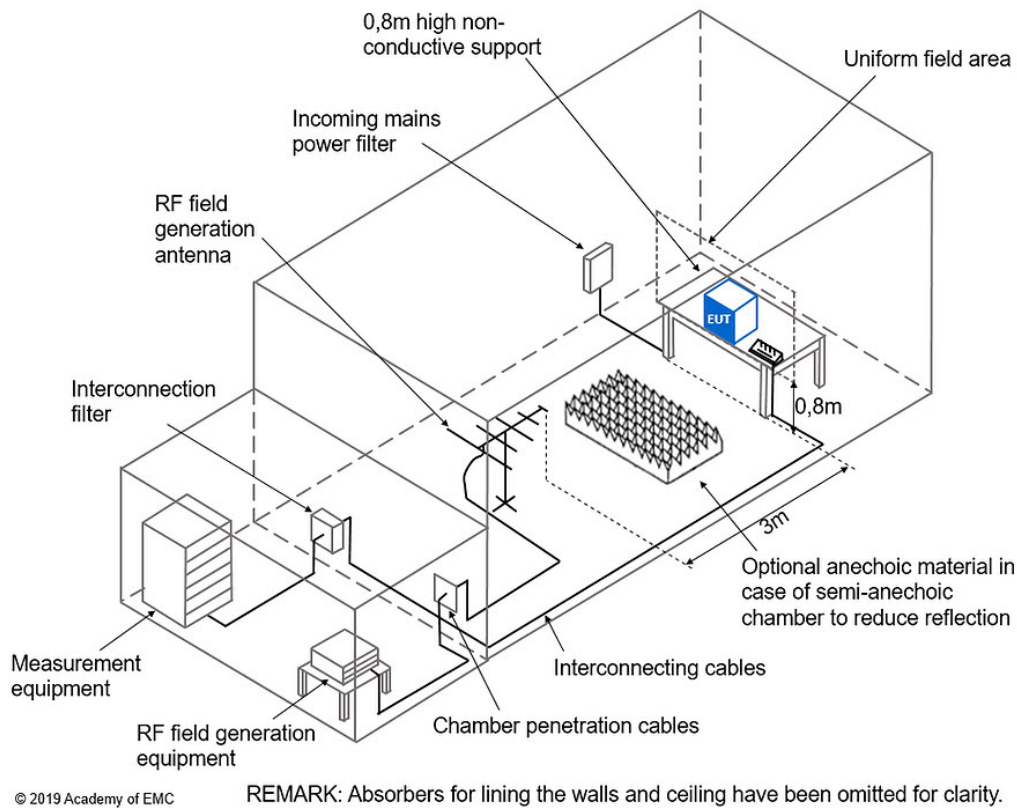


Figure 6.16: Radiated Immunity test setup

EUT passed the radiated immunity test up to test levels of 3V/m. Higher test levels resulted in false triggering on the keyboard.

#### 6.7.4 Conducted Immunity

The conducted immunity test procedure as defined in the *Conducted Immunity testing according to the IEC 61000-4-6 standard: 2008 Edition-3: Electromagnetic compatibility (EMC): Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields* standard is defined as follows:

- > Test is performed with EUT placed over horizontal reference metal ground plane.
- > EUT is placed on a non-conductive table at a height of at least 30cm.
- > Electromagnetic disturbance from the RF signal generator is injected into the EUT power cables via the coupling decoupling network (CDN-M2).
- > The RF disturbance signal is in the frequency range 150kHz to 80MHz with test RMS amplitudes of 1V, 3V, and 10V.
- > Amplitude modulation with 80% and 1Hz sine carrier wave is applied to the RF signal.
- > The EUT is tested for normal functionality while exposed to the conducted disturbance at specified levels.

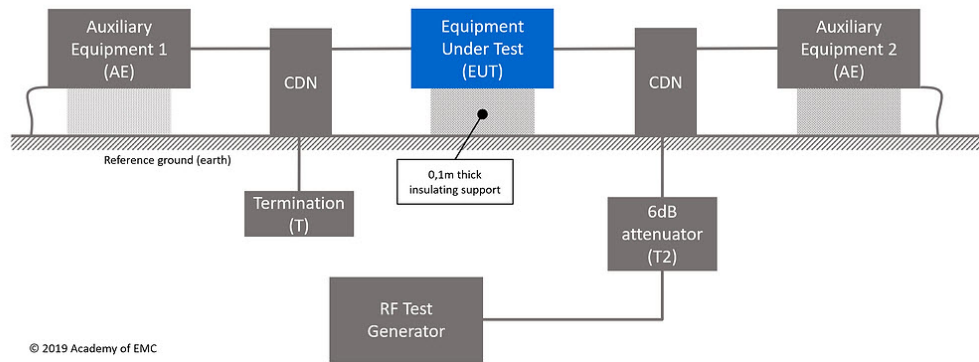


Figure 6.17: Radiated Immunity test setup

Table 6.6: Conducted Immunity Test

Test Level	Frequency Sweep Range	RMS Amplitude	EUT Functionality
1	150kHz - 80MHz, 1% step	1	EUT fully functional, with no false key activations.
2		2	EUT fully functional, with no false key activations.
3		8	EUT fully functional, with no false key activations except in the frequency range 16MHz to 17.5MHz.
4		10	EUT not functional, with false key activations.

### 6.7.5 ESD Immunity

The ESD test procedure as defined in the *Electrostatic Discharge (ESD) immunity tests IEC61000-4-2: SANS 61000-4-2 (2009) / IEC 61000-4-2 (2008): Testing and measurement techniques - Electrostatic discharge immunity test* standard is defined as follows:

- > EUT is placed on an insulated table with a horizontal reference ground plane below the table.
- > An insulating sheet of thickness 0.50mm is placed between the EUT and the tabletop.
- > ESD gun is used to generate the test voltages used in the contact and air discharge tests.
- > For contact discharge, the ESD gun probe is placed in contact with the conductive metal surface of the EUT.
- > For air discharge, the ESD gun probe is placed in contact with the insulated surfaces of the EUT.



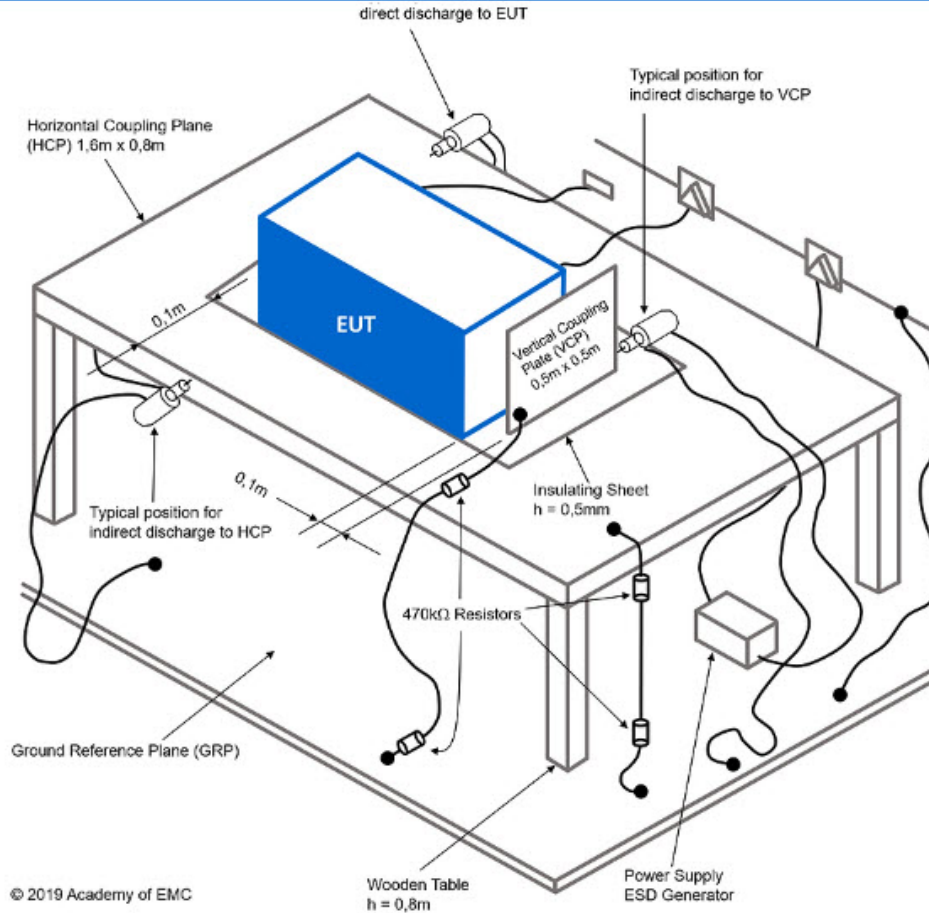


Figure 6.18: ESD Immunity Test Setup

Table 6.7: Contact ESD Immunity Test

Contact Discharge		
Level	Test Voltage (kV)	EUT Functionality
1	2	Pass (Class A)
2	4	Pass (Class A)
3	6	Pass (Class A)
4	8	Pass (Class A)

Table 6.8: Air ESD Immunity Test

Air Discharge		
Level	Test Voltage (kV)	EUT Functionality
1	2	Pass (Class A)
2	4	Pass (Class A)
3	8	Pass (Class A)
4	15	Pass (Class A)

## 6.8 Current Consumption

The keyboard is configured as follows:





- > Number of IQS9320 devices: 4
- > Number of channels device1: 17
- > Number of channels device2: 17
- > Number of channels device3: 17
- > Number of channels device4: 17
- > Tx frequency: 16MHz
- > Conversion frequency: 8MHz
- > ATI Target: 250
- > Communication mode: I2C
- > I2C polling rate: 1ms

The measured current consumption for the different report rates is as follows:

*Table 6.9: Keyboard Current Consumption*

Channel update rate	No key press average current
1ms	29mA (TBC on C1)
5ms	8.50mA (TBC on C1)



## 7 Interface Description

The IQS9320 provides two possible interface methods to communicate with a host controller / MCU.

> I<sup>2</sup>C

> Key scanning

Figure 7.1 below provides a brief diagrammatic representation of each:

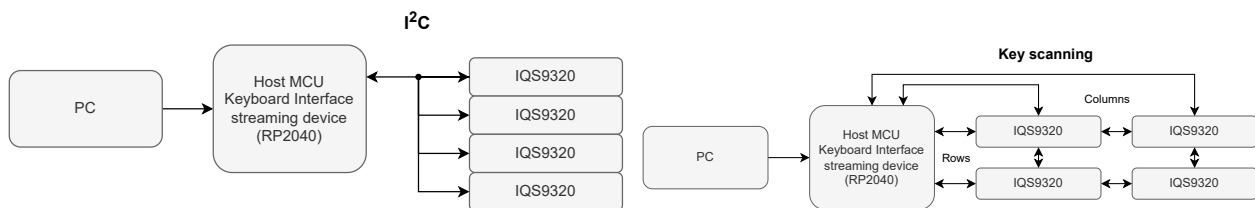


Figure 7.1: Block Diagram Overview Of Interface Methods

### 7.1 I<sup>2</sup>C interface mode

The I<sup>2</sup>C interface is the preferred (and IQS9320 recommended) scheme for a shared bus (single SCL and SDA pair) to communicate with all IQS devices. Three additional and shared IO connections towards the MCU conveys the global device event interrupts and reset indication/control. Separate device address selections should be made by means of hardware configuration (I<sup>2</sup>C address select).

### 7.2 Key scan interface mode

The **Key scan** interface requires IQS devices to be connected in a matrix of shared column and row lines. The amount of GPIO pins required on the MCU increases to 10 (2 columns + 2 rows with 4 lines per device row interface) to service four IQS9320 in a 2x2 matrix as an example. This interface still supports the usability of SCL and SDA lines for device setup and debugging but host control is needed to enter/enable an I<sup>2</sup>C communication session on a single device in the matrix at a time.

Technical detail and specification for both interface schemes are described in detail in the relevant IQS datasheet (subject to part capability).

### 7.3 MCU driver, keyboard interface and interaction reference code

Example code (Arduino based C/C++ for I<sup>2</sup>C interface support) for a host controller / MCU is available on GitHub:



iqs9320examplecode:  
<https://github.com/Azoteq/iqs9320-example-code.git>

Reference code (supporting both for I<sup>2</sup>C and Key scan interfaces) for a host keyboard MCU is interface streamer example (such as the featured DS220) is available on GitHub:



azo\_ki\_arduino:  
[https://github.com/Azoteq/azo\\_ki\\_arduino.git](https://github.com/Azoteq/azo_ki_arduino.git)

The intended MCU (RP2040) hardware platform is commercially available, better known as the [Raspberry Pi Pico](#) which has various IDE and development platform support with a wealth of technical resources.



Azoteq also offers a Python interaction project/module for use with the keyboard interface streamer (DS220):



azo\_ki\_python:  
[https://github.com/Azoteq/azo\\_ki\\_python.git](https://github.com/Azoteq/azo_ki_python.git)



## 7.4 Software flow

Figure 7.2 below shows the software flow diagram for the referenced example code.

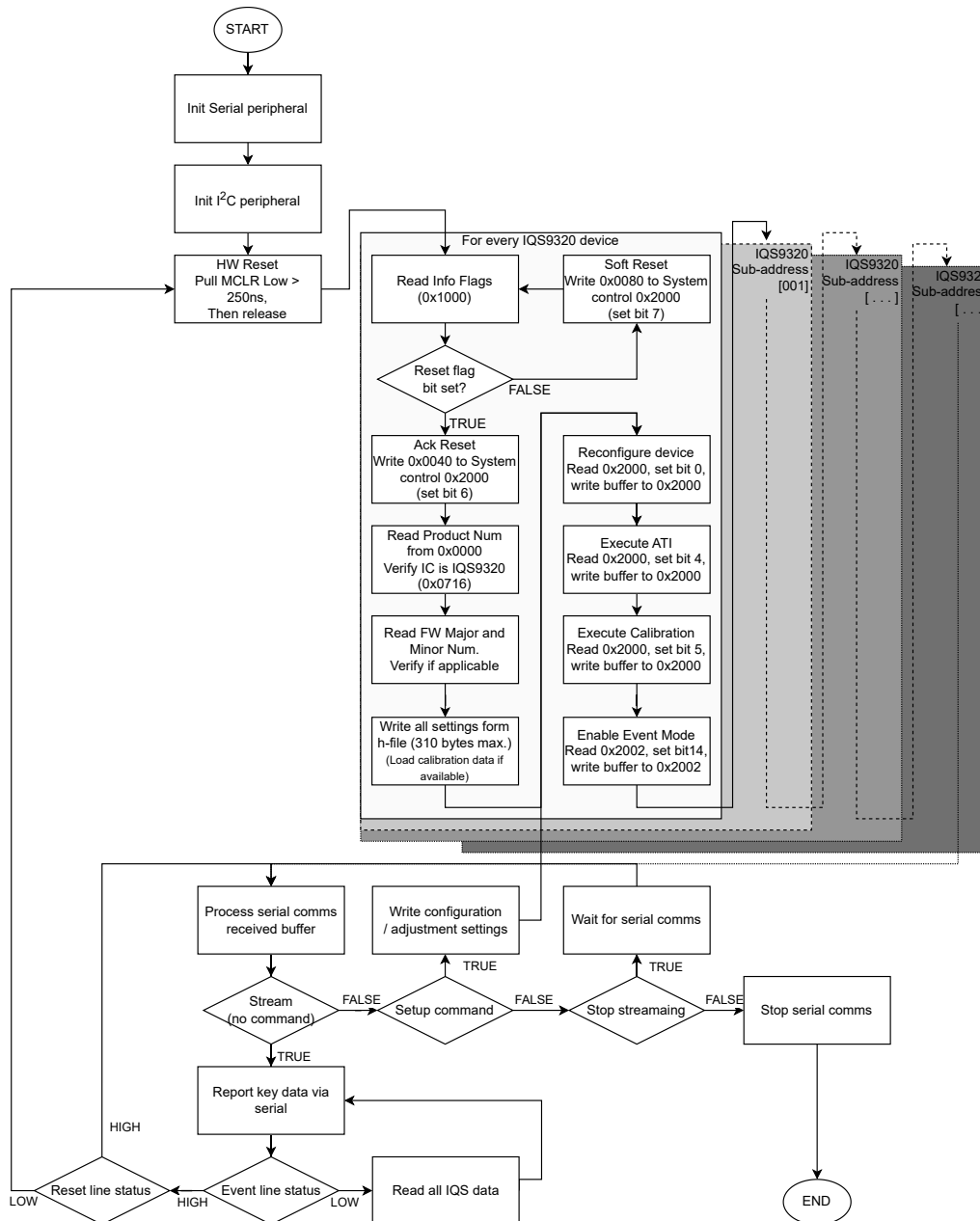


Figure 7.2: Master Software Flow Diagram For Serial And IQS9320 I<sup>2</sup>C Interaction

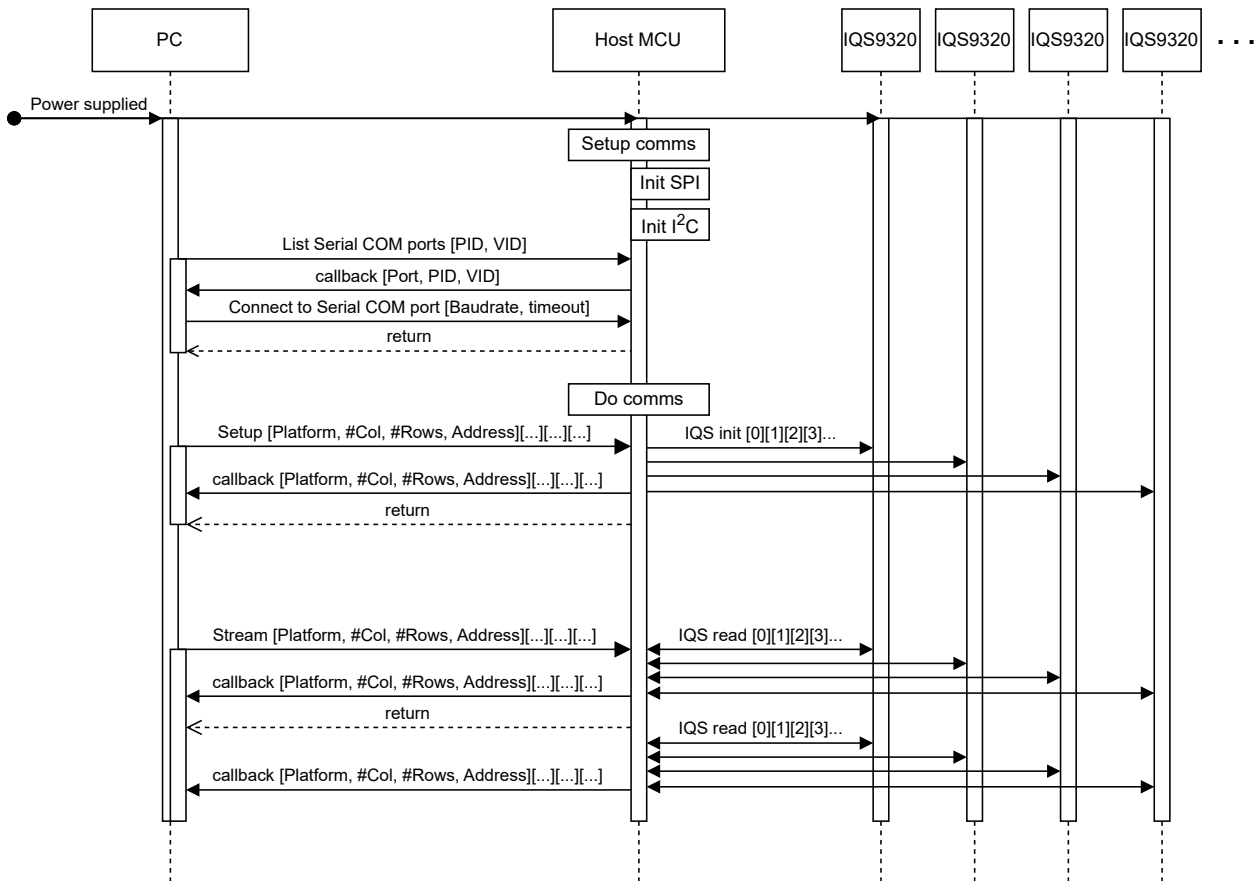


Figure 7.3: Master Software Sequence Diagram

## 7.5 Additional status indication

*EVENT* and *RESET* outputs can be enabled per device. This configures the respective GPIO pins as open-drain active-low outputs to indicate when any key interaction events or device reset related to that device have occurred. This enables hosts to react only when needed with minimal service requirements and reduced power consumption. Multiple IQS device outputs can be connected together to share the same MCU input and handled in a global response fashion (example wake and check all devices via I<sup>2</sup>C and continue at high response service rate).

## 7.6 PC interface

The example showcased in this design document focusses on the IQS interface with an arbitrary MCU acting as host controller. Serial communication is established between the PC and the host MCU (keyboard streamer), although any other protocol can be used (wired or wireless). The critical consideration is to ensure that the highest response rate can be achieved and transmitted data integrity are ensured without error by employment of some parity or redundancy check or method.



## 8 Revision History

Release	Date	Comments
v1.0	2024/02/21	Initial document released
v1.1	2024/04/09	Updated IQS9320 pinout and AZP1331C1 hardware update



## A Bill of Materials

The following Table A.1 provides the bill of material detail for the schematic layout in Appendix B.

Table A.1: Bill Of Materials

Part	Description	Designator	Footprint	Manufacturer (P/N)
IQS9320	IQS9320-QFN-52N	U1, U2, U3, U4	QFN-52N	Azoteq (IQS9320001QFR)
22 μF	Capacitor, ceramic, X5R, 20%	C71, C94, C117, C140	0805	Murata (GRM21BR60J226ME39L)
47 μF	Capacitor, ceramic, X5R, 20%	C74, C97, C120, C143	0805	Samsung (CL21A476MQYNNNG)
100 nF	Capacitor, ceramic, X7R, 10%	C70, C73, C93, C96, C116, C119, C139, C142	0402	Yageo (CC0402KRX7R7BB104)
100 nF	Capacitor, ceramic, X7R, 10%	C161, C162, C163, C164	0603	Yageo (CC0603KRX7R7BB104)
100 pF	Capacitor, ceramic, C0G/NP0, 5%	C69, C72, C75 to C160	0402	Murata (GCM1555C1H101JA16D)
82 pF	Capacitor, ceramic, C0G/NP0, 2%	C1 to C68,	0402	Murata (GRM1555C1H820GA01J)
100R	Resistor, 100 Ω, 1%, 0.05W	R20, R21, R24, R25, R28, R29, R32, R33, R36, R37, R40, R41, R44, R45, R48, R49, R52, R54, R55, R58, R59, R62, R63, R66, R67, R70, R71, R74, R75, R78, R79, R82, R83, R86, R88, R89, R92, R93, R96, R97, R100, R101, R104, R105, R108, R109, R112, R113, R116, R117, R120, R122, R123, R126, R127, R130, R131, R134, R135, R138, R139, R142, R143, R146, R147, R150, R151, R154	0201	
750R	Resistor, 750 Ω, 1%, 0.0625W	R47, R51, R81, R85, R115, R119, R149, R153	0402	
1k	Resistor, 1 kΩ, 1%, 0.0625W	R148	0402	
1.21k	Resistor, 1.21 kΩ, 1%, 0.0625W	R22, R23, R26, R27, R30, R31, R34, R35, R38, R39, R42, R43, R46, R50, R53, R56, R57, R60, R61, R64, R65, R68, R69, R72, R73, R76, R77, R80, R84, R87, R90, R91, R94, R95, R98, R99, R102, R103, R106, R107, R110, R111, R114, R118, R121, R124, R125, R128, R129, R132, R133, R136, R137, R140, R141, R144, R145, R148, R152, R155	0402	
4.7k	Resistor, 4.7 kΩ, 1%	R16, R17, R18, R19	0402	
5.1k	Resistor, 5.1 kΩ, 1%	R14, R15	0402	
0R/SOT	Resistor, 0 Ω	R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13	0402	
Unionwell Inductive coil	8mm 2-layer PCB coil, 4mm TH 1.2 μH	L1 to L68	Special	GT06-A001
USB-C	USB-C connector RCP USB2.0 24P	J1	Special	GCT (USB4105-GF-A))
FP201EH-006M10M	FFC-/FPC 6W connector	P2	0.5mm pitch	JXT (FP201EH-006M10M)
505110-3091	FFC-/FPC 30W connector	P12	0.5mm pitch	MOLEX (5051103091-FPC-30W)
NS107S-RGB	LED, 2.0x2.0x0.78mm, TOP SMD Type, 0.2Watt	DS1 to DS68	6P DIL	Newstar (NS107S-2020-RGB)
0.5A POLY-SWITCH	Polyswitch, nanoSMDC050F, 0.5A, 13.2V	R1	1206	Tyco (nanoSMDC050F/13.2)
PCB	FR4-PCB, ENIG finish, 1.6mm thick, 4-layer	AZP1331C1		PCB manufacturer of choice





## B Schematic and Layout

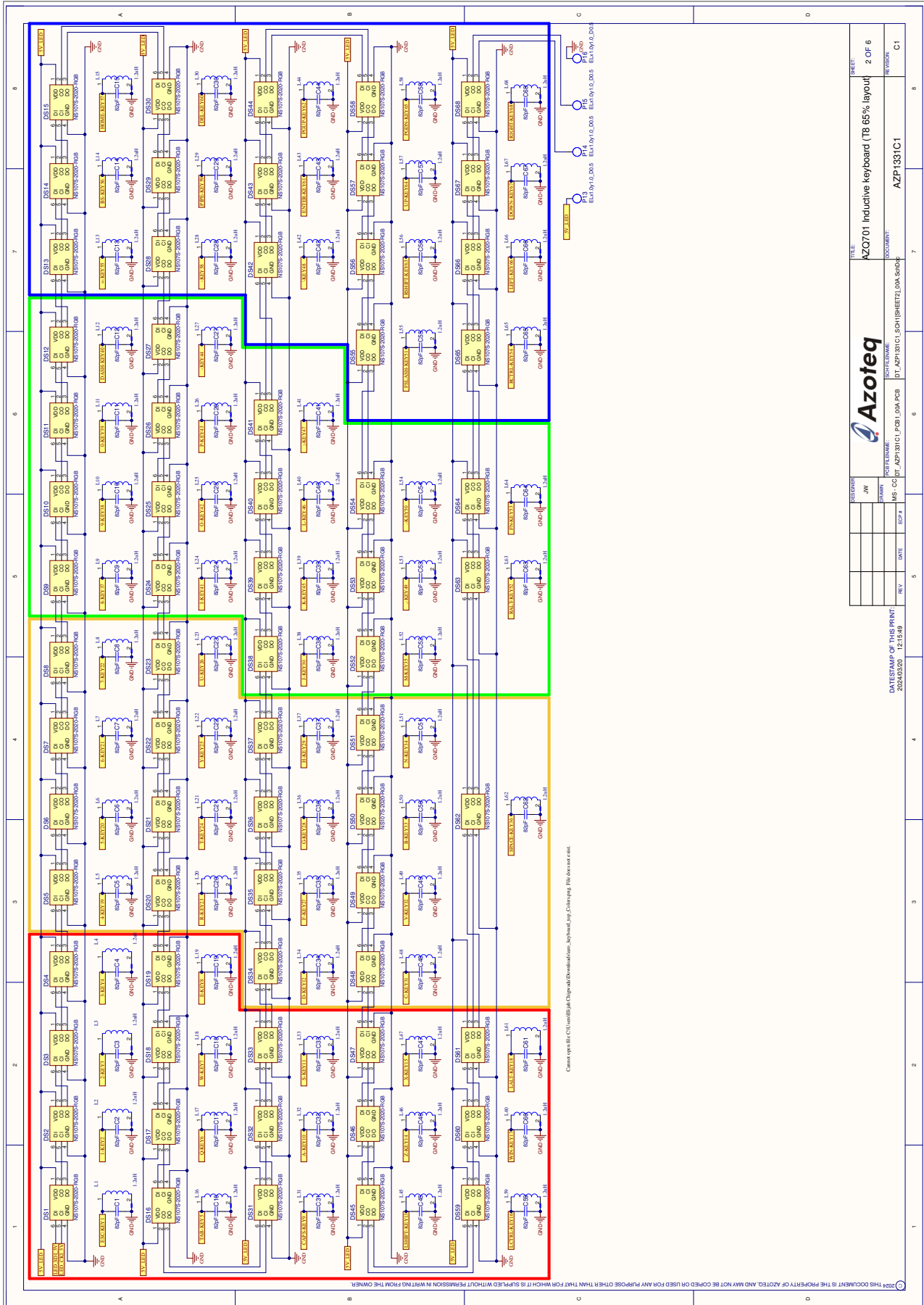


The information published in this document pertaining to the schematic and PCB detail are subject to change and may be amended based on ongoing research, development, qualification and feature improvement of the IQS device and supporting operational hardware circuits and environment. For customers starting new designs, please contact the relevant support channel or write to Azoteq ([info@azoteq.com](mailto:info@azoteq.com)) to obtain the latest revision schematic and PCB layout files.



## B.1 Schematic design

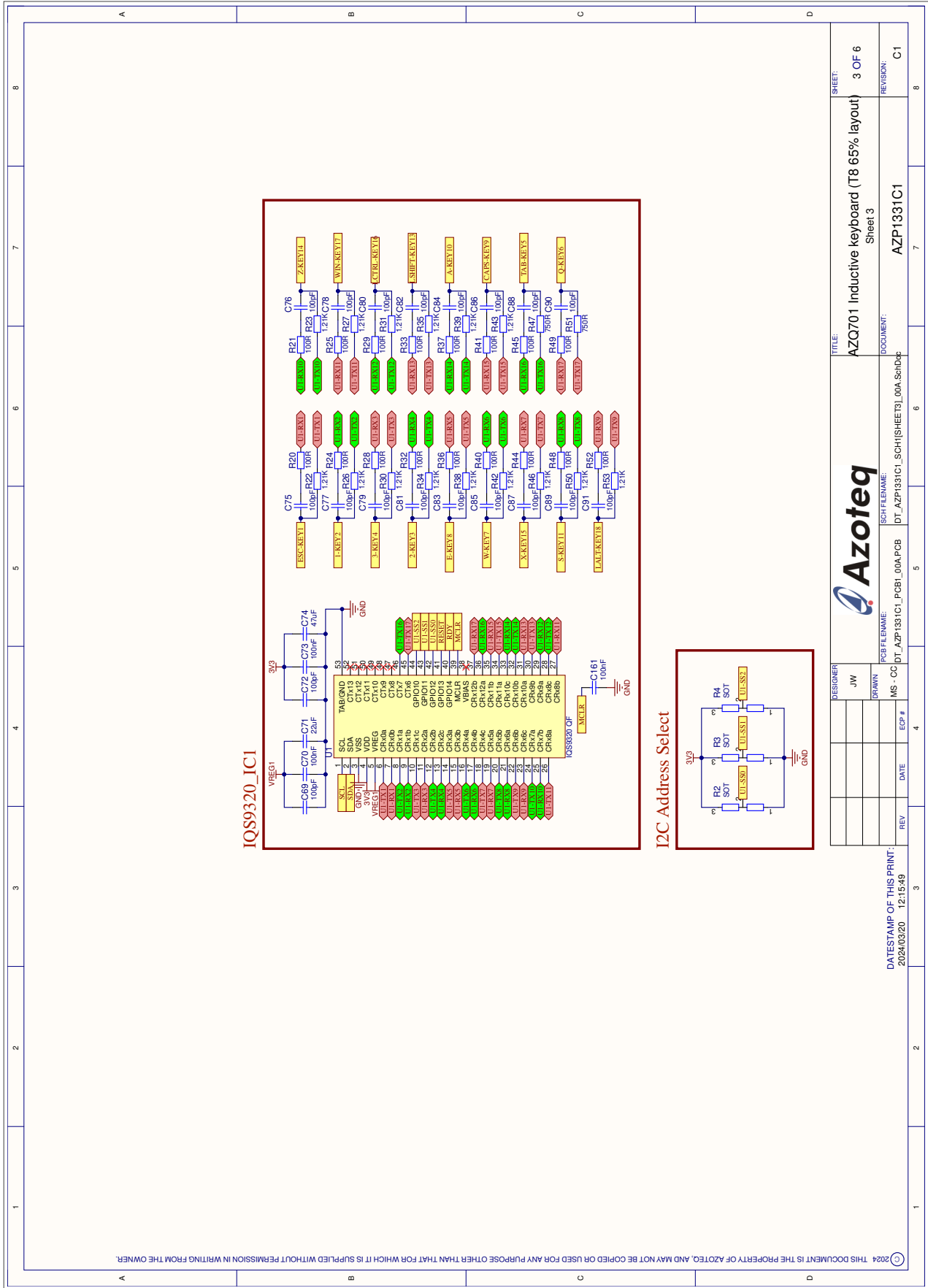
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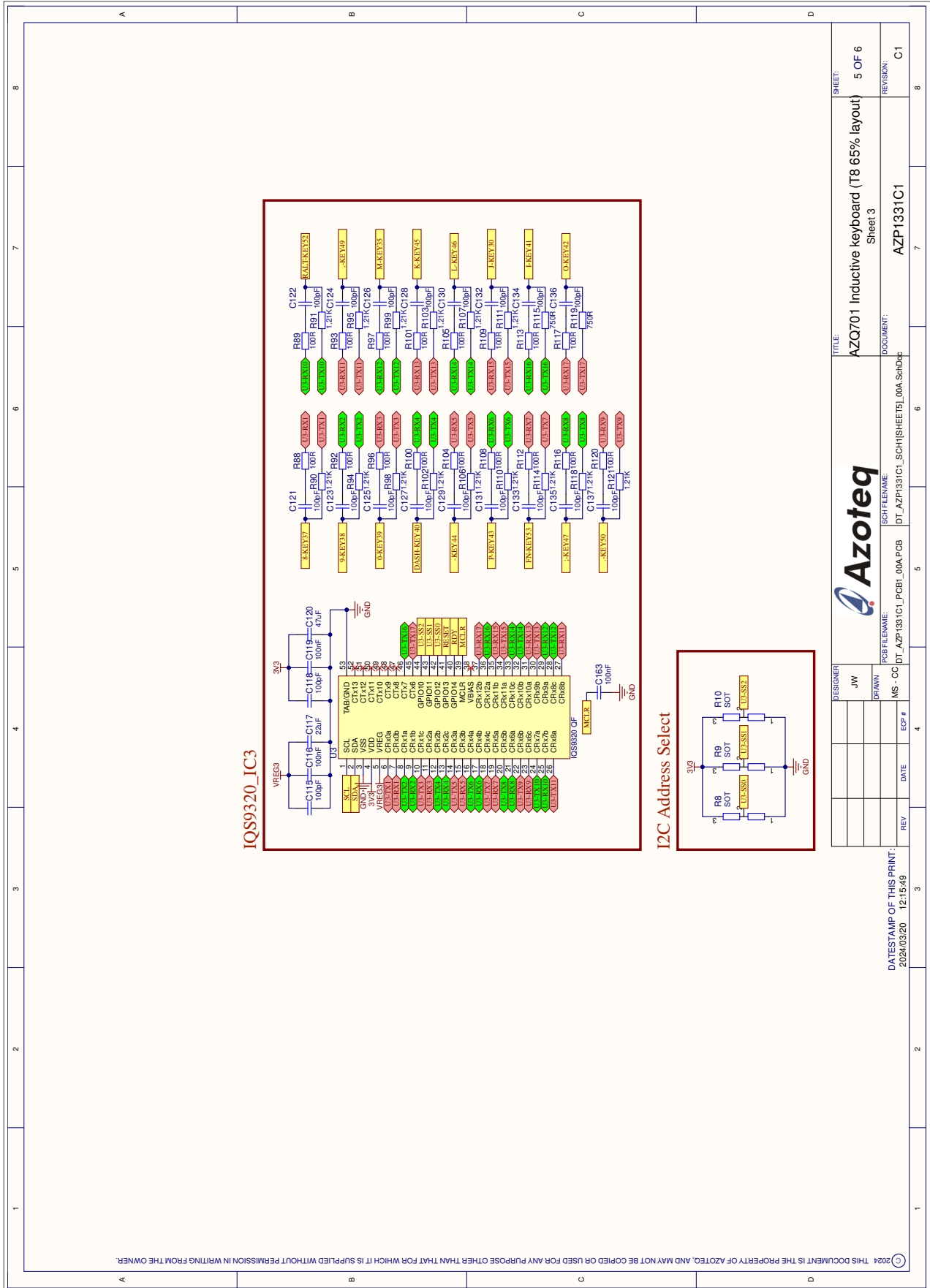
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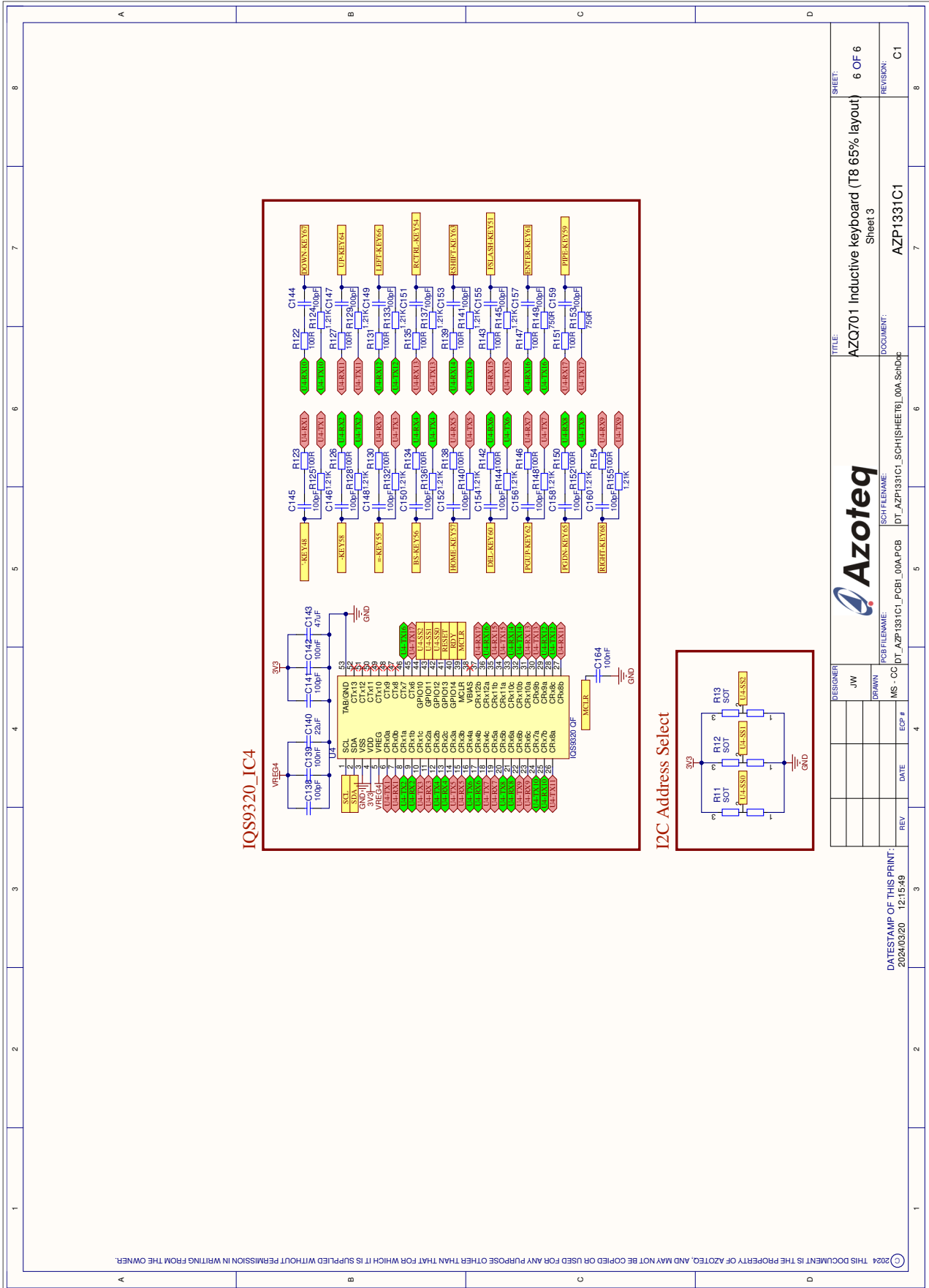


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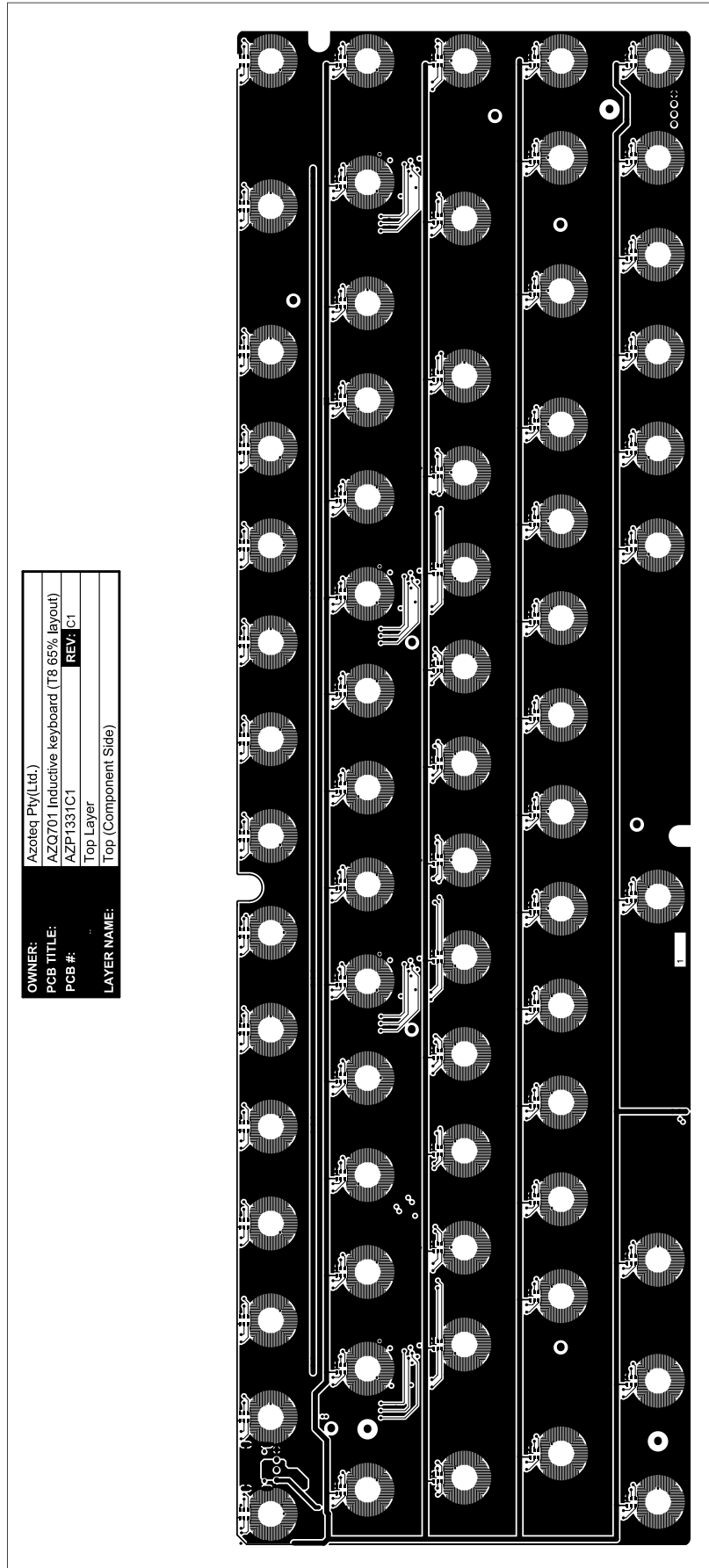


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REV		DATE		DOCUMENT	Sheet 3



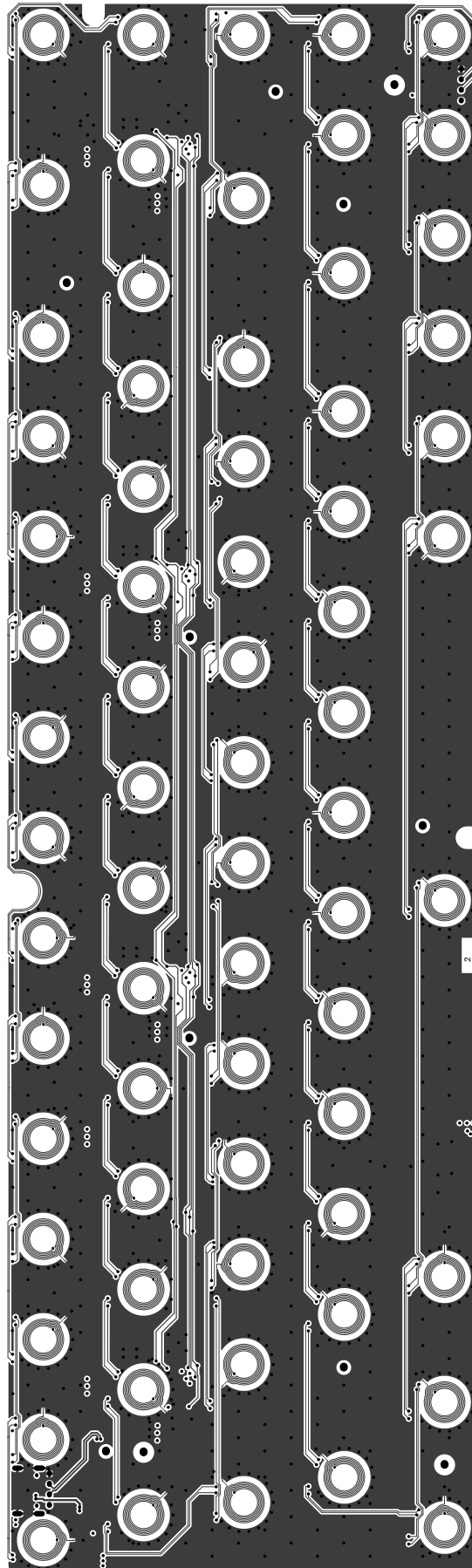


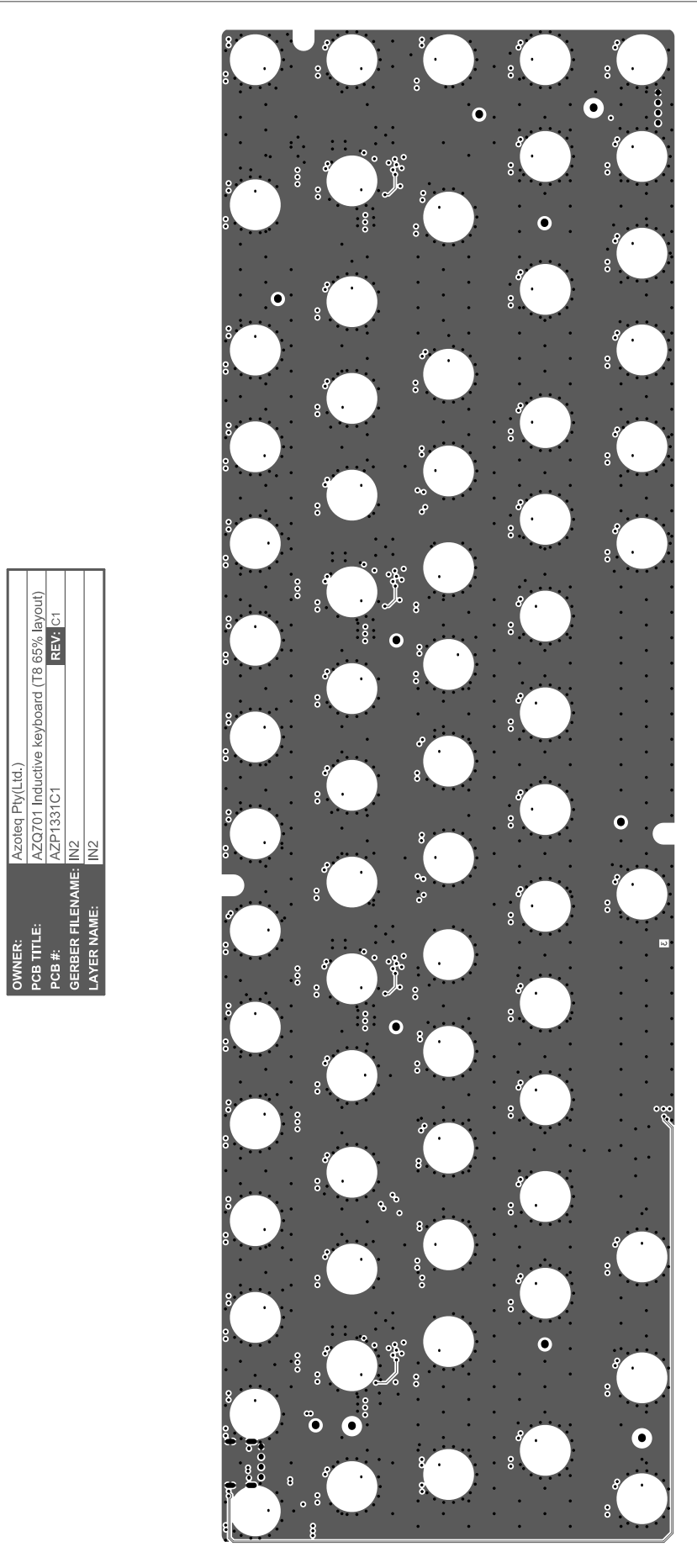
## B.2 PCB design: Gerbers





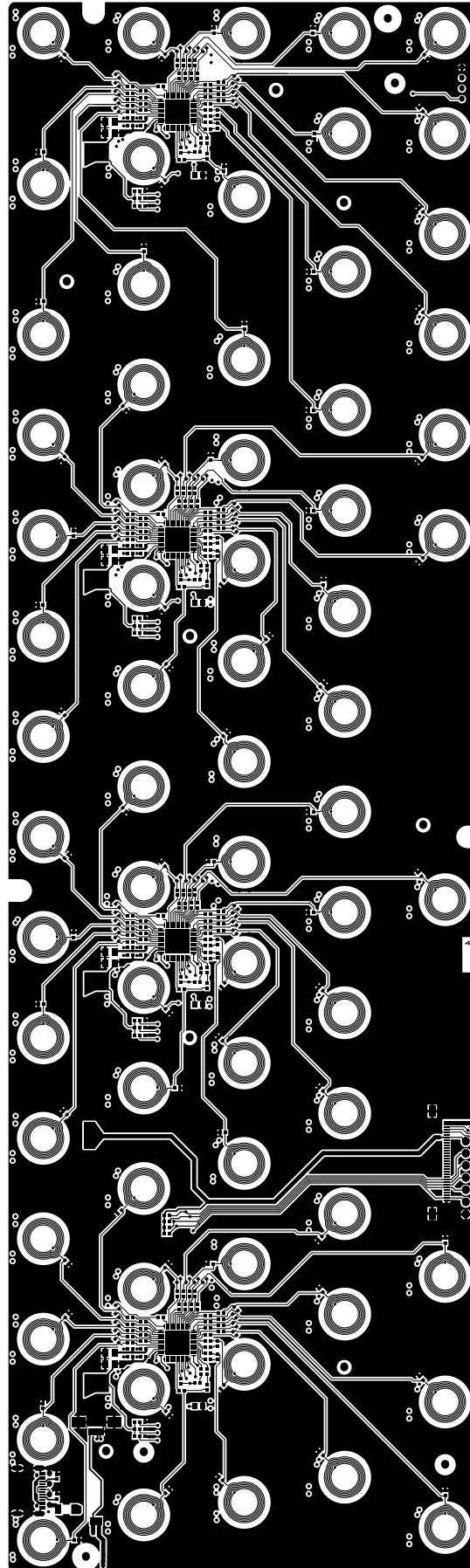
OWNER:	Azoteq Pty(Ltd.)
PCB TITLE:	AZQ701 Inductive keyboard (T8 65% layout)
PCB #:	AZP1331C1 REV. C1
GERBER FILENAME:	IN1
LAYER NAME:	IN1





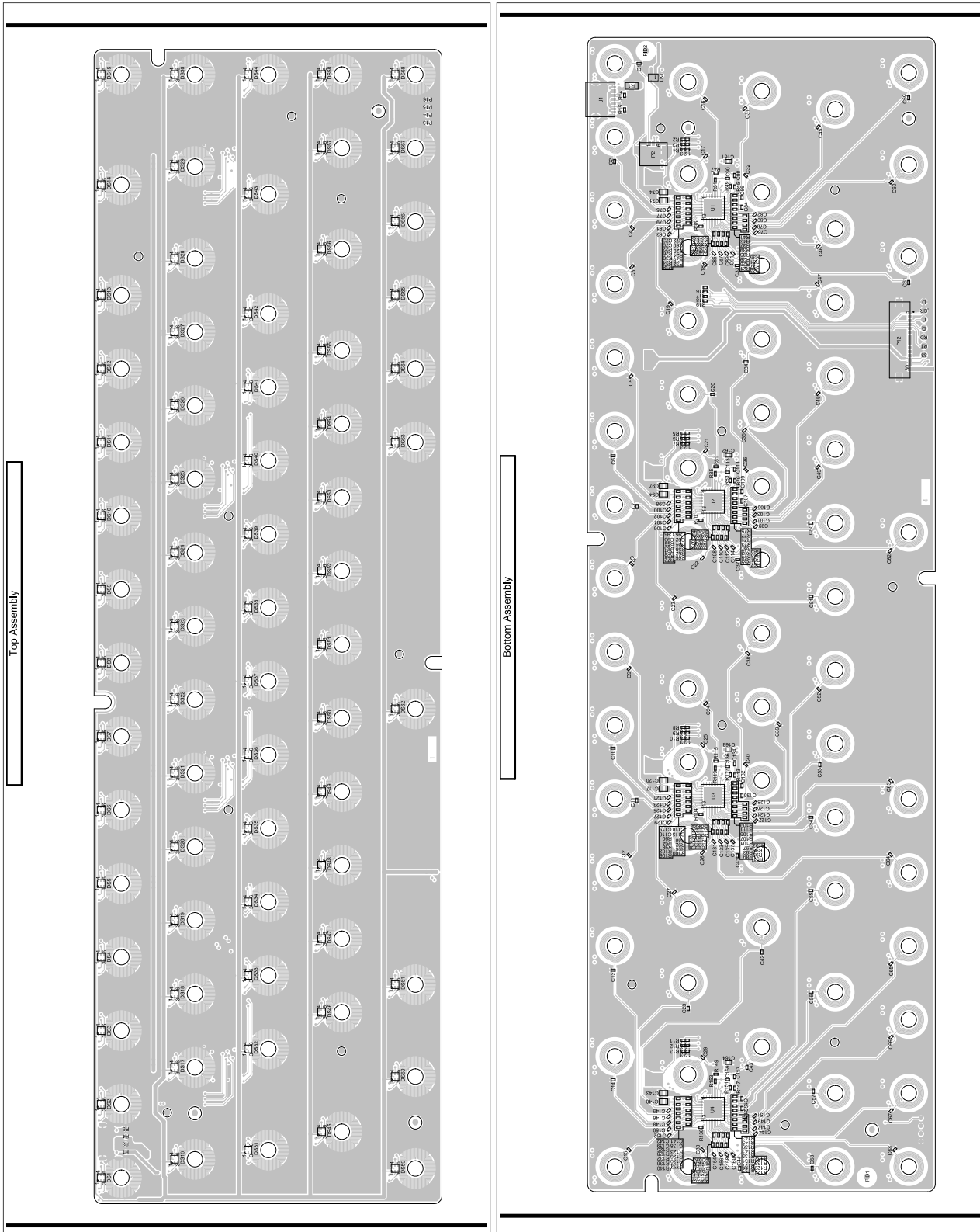


OWNER:	Azoteq Pty(Ltd.)
PCB TITLE:	AZQ701 Inductive keyboard (T8 65% layout)
PCB #:	AZP1331C1 REV. C1
GERBER FILENAME:	Bottom Layer
LAYER NAME:	Bottom (Solder Side)



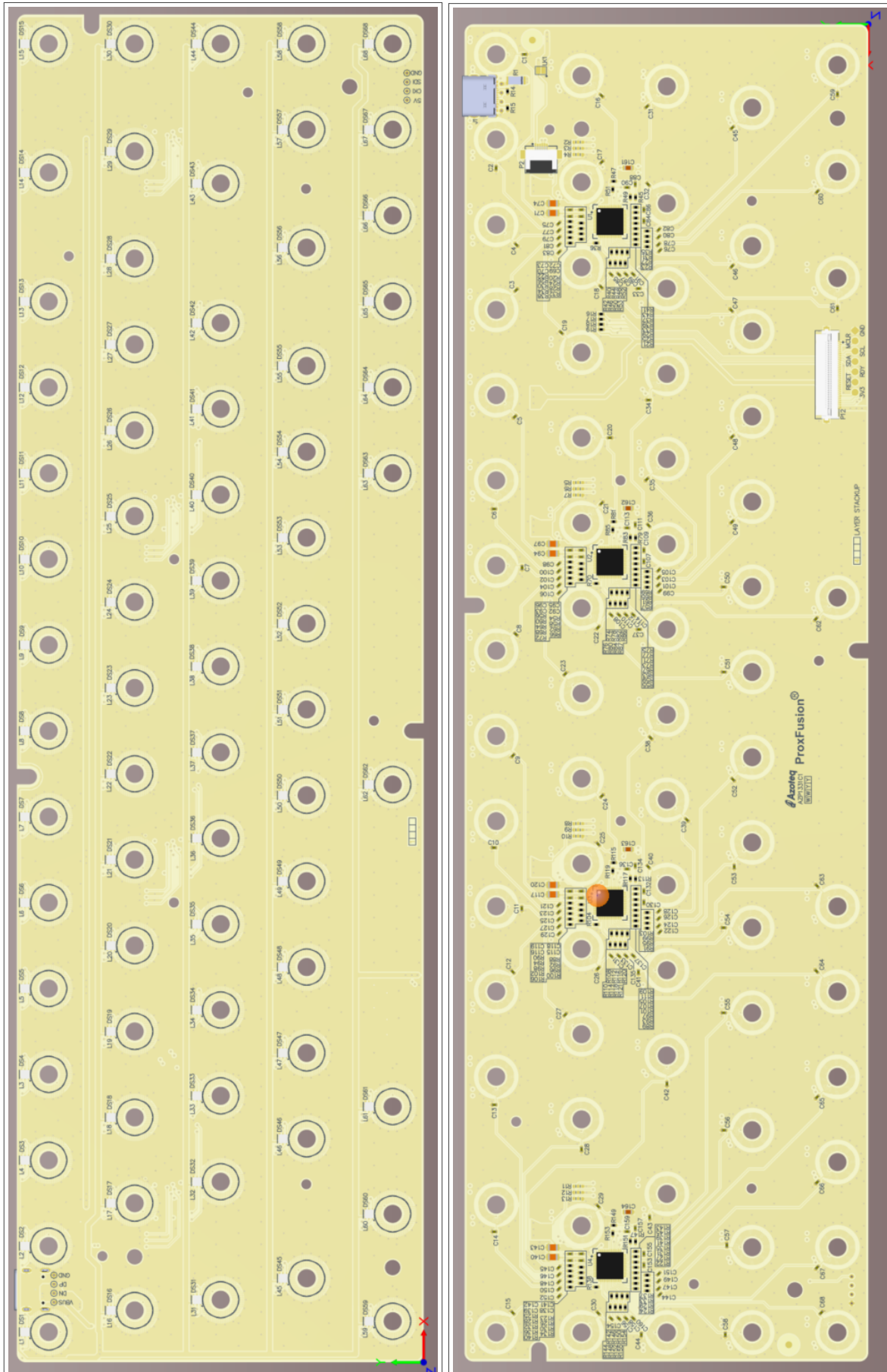


### B.3 PCB design: Top and bottom assembly





## B.4 PCB design: 3D bodies







## C Mechanical Design

### C.1 PCB design

#	Name	Type	Thickness	#	Thru 1:4
	Top Overlay	Overlay			
	Top Solder	Solder Mask	0.01mm		
1	Top Layer	Signal	0.035mm	1	
	Dielectric1	Core	0.2104mm		
2	IN1	Signal	0.0152mm	2	
	Dielectric 3	Prepreg	1.065mm		
3	IN2	Signal	0.0152mm	3	
	Dielectric 2	Core	0.2104mm		
4	Bottom Layer	Signal	0.035mm	4	
	Bottom Solder	Solder Mask	0.01mm		
	Bottom Overlay	Overlay			

Figure C.1: PCB Layer Stack-up And Via Detail







## C.2 Key design



Figure C.3: Exploded View Of Key Part Housing, Spring, Stem And Metal Plunger Assembly

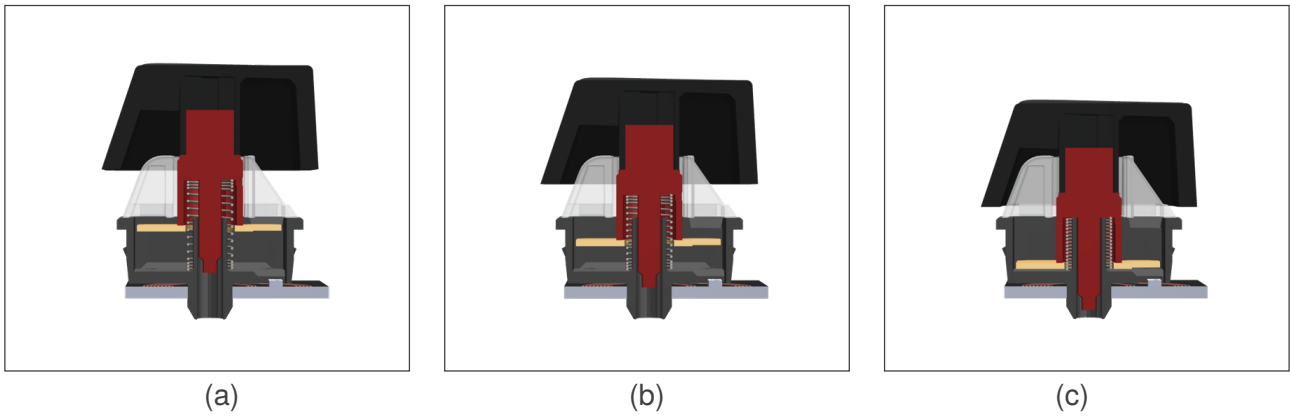


Figure C.4: Key mechanic positions for (a) relaxed, (b) halfway pressed and (c) fully pressed actuation



### C.3 Coil design

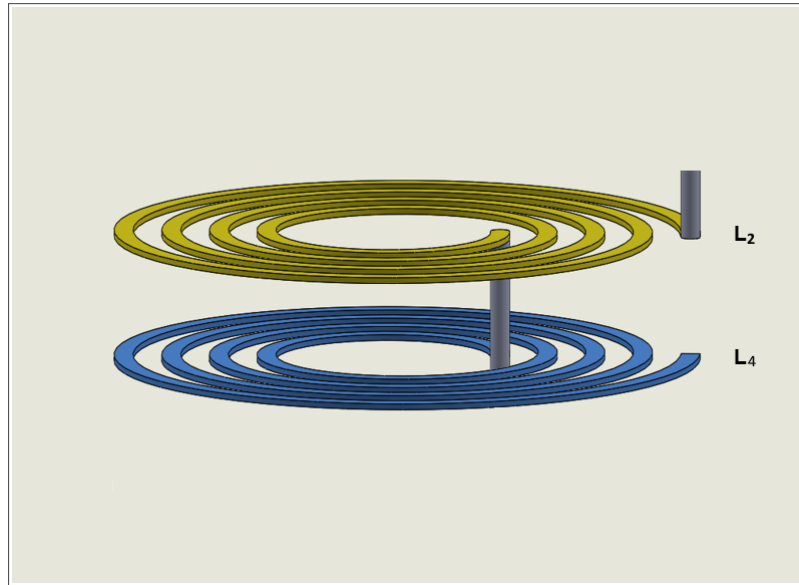


Figure C.5: Inner Layer PCB Coil Design With Via Transfer Connections

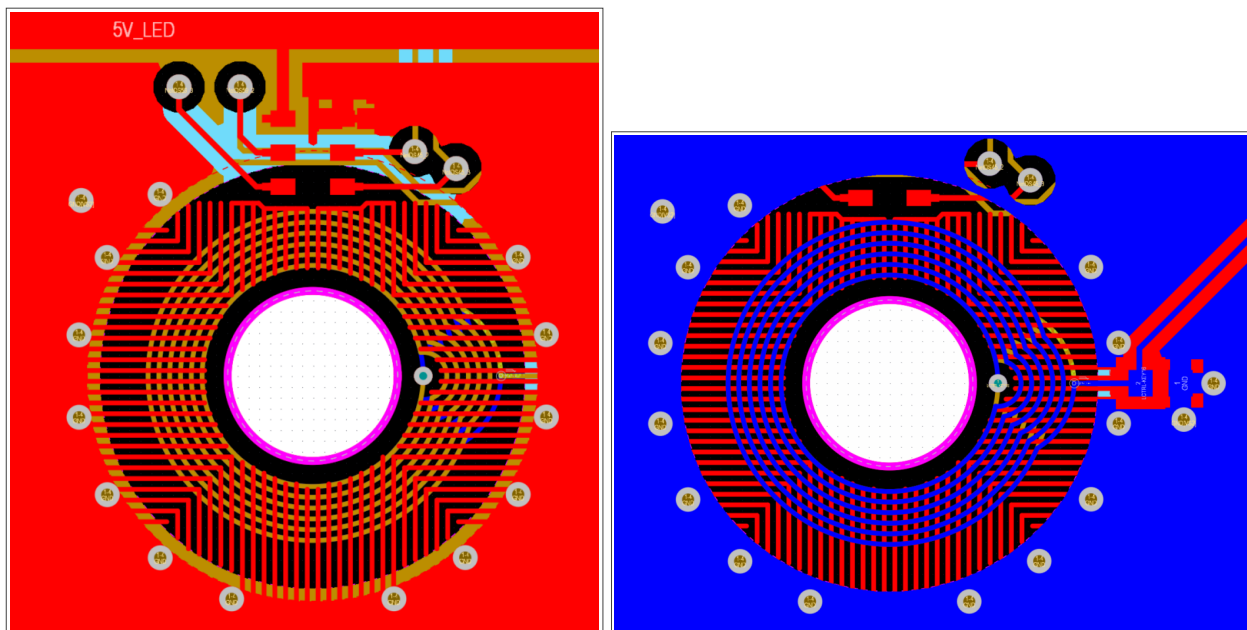
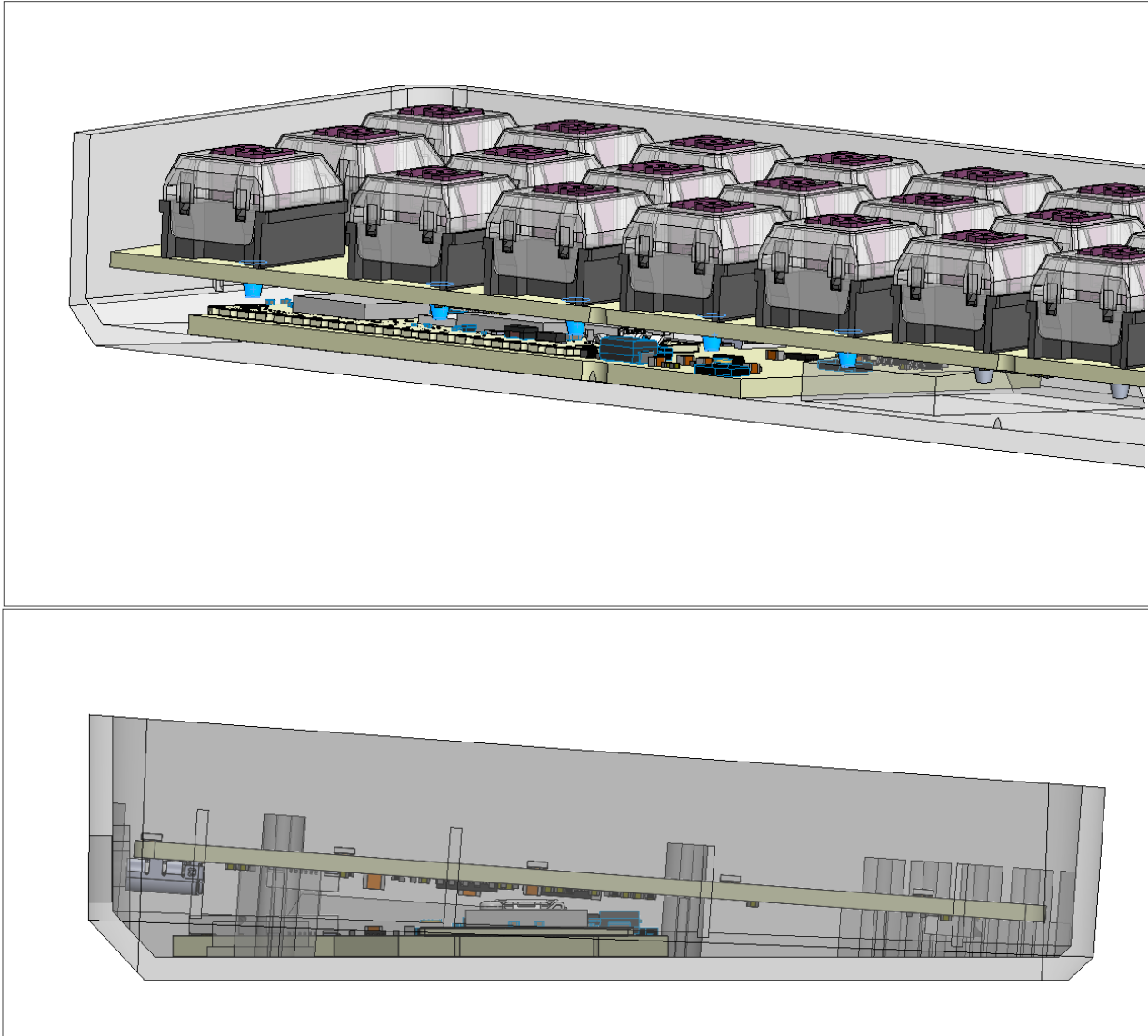


Figure C.6: Top And Bottom Layer Ground Shielding And -Pours



## C.4 Full keyboard assembly



*Figure C.7: Sectional And Transparent Views Of PCBAs Within Keyboard Housing*

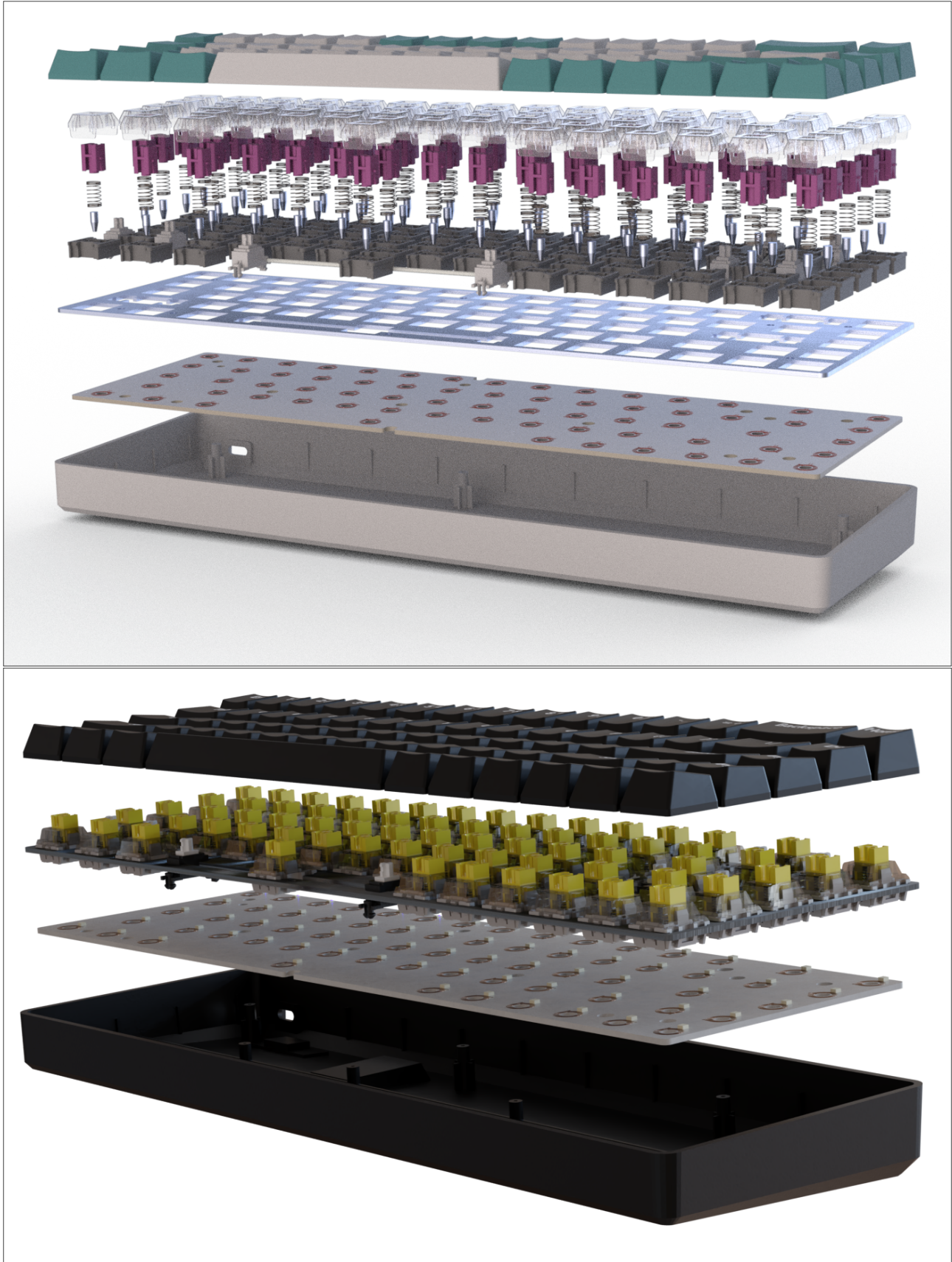
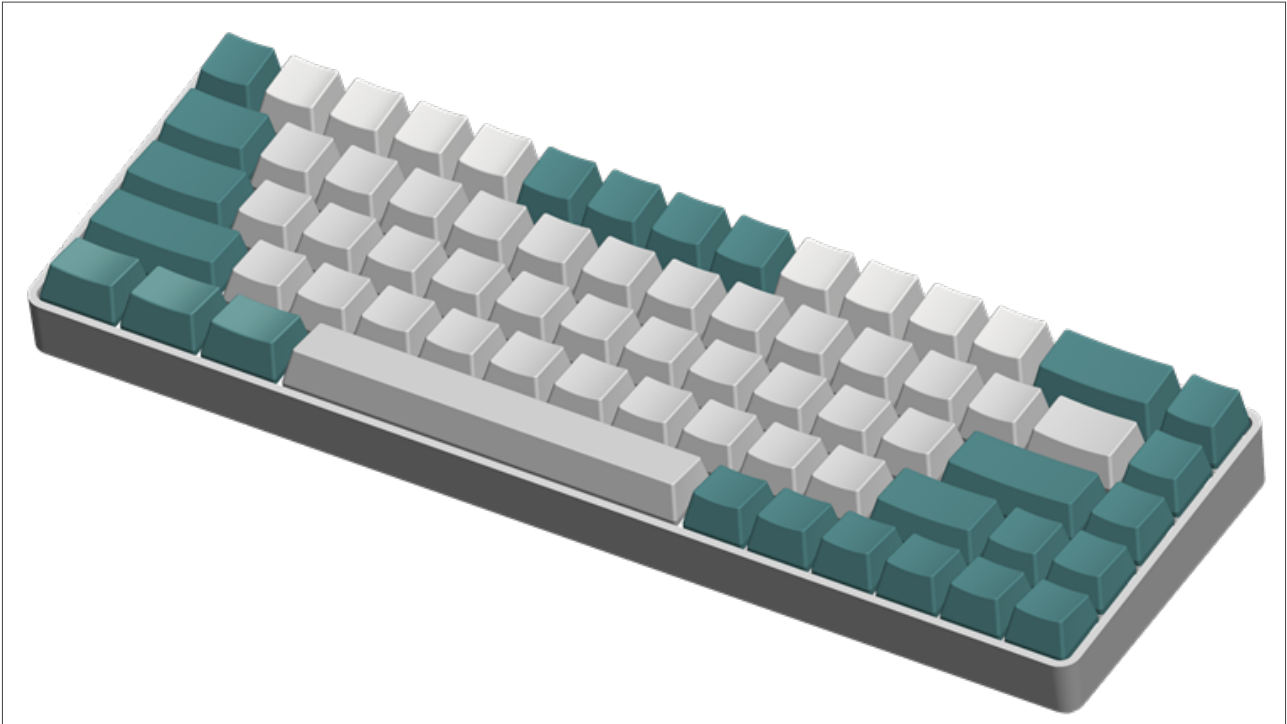


Figure C.8: Exploded Keyboard View: Full Stack-up Assembly



*Figure C.9: Fully Assembled Keyboard*





## D Glossary

Acronymm	Term	Definition
ABS	Acrylonitrile butadiene styrene	A common thermo plastic polymer typically used in electronic housing material.
ANSI	American National Standards Institute	An organization supporting the development of technology standards in the USA.
AOI	Automated Optical Inspection	An automated visual inspection of printed circuit board manufacture (or assembly) where a camera autonomously scans the device under test for both catastrophic failure (e.g. missing component) and quality defects (e.g. fillet size, shape or component skew).
ASIC	Application-specific Integrated Circuit	Integrated circuit for a particular use.
BLE	Bluetooth Low Energy	A wireless personal area network technology standard for mobile electronics.
CAD	Computer Aided Design	Use of computer-based software to aid in design processes.
CH	Channel	A software defined instance of a single sensor with related settings, measurement values and UI processing.
CPU	Central Processing Unit	Main processing circuitry for arithmetic, logic, control and input / output operations.
CS	Count(s)	A single unit / quantity of an arbitrary amount of charge or current measured by the ProxFusion sensor engine.
	Cycle	A period during which selected sensors are sampled. One measurement is taken per ProxFusion measurement circuit.
ENIG	Electro-less nickel immersion gold	A metal plating process used in the manufacture of printed circuit boards, to avoid oxidation and improve the solderability of copper contacts and plated through-holes.
HASL	Hot Air Solder Levelling	A type of PCB finish where the board is dipped into a bath of molten solder so that all exposed copper surfaces are covered by solder and the excess is removed by passing through hot air knives.
IC	Integrated Circuit	A set of electronic circuits on one small flat piece (or "chip") of semiconductor material, usually silicon.
IEC	International Electrotechnical Commission	An organization that prepares and publishes international standards for all electrical, electronic and related technologies.
I <sup>2</sup> C	Inter-Integrated Circuit	A synchronous, multi-controller/multi-target (master/slave), packet switched, single-ended, serial communication bus.
IP	Ingress Protection	Ratings which grade the resistance of an enclosure against the intrusion of dust or liquids to protect electrical and electronic products.
IRQ	Interrupt Request	A hardware signal sent to the processor that temporarily stops a running program and allows a special program, an interrupt handler or -service routine, to run instead.
ISR	Interrupt Service Routine	A special block of code associated with a specific interrupt condition.
LDO	Low Dropout	A type of linear regulator with a low input-output voltage differential.
LED	Light-Emitting Diode	A semiconductor device that emits light when current flows through it.
LTA	Long Term Average	A slow filtered response or averaged value evaluated over a long period and used as a baseline or reference to differentiate instantaneous or sudden changes in new measurement data.
MCU	Microcontroller Unit	A small computing device with processor core(s), memory, peripherals and basic input / output functionalities.
NKRO	N-key Rollover	Ability to correctly detect input from each key on the keyboard at the same time, regardless of how many other keys are also being pressed.
OSP	Organic Solderability Preservative	A method for coating of printed circuit boards that uses a water-based organic compound that selectively bonds to copper and protects the copper until soldering.
PCB	Printed Circuit Board	A non-conductive material with conductive lines printed or etched. Electronic components are mounted on the board and the traces connect the components together to form a working circuit or assembly.
PMU	Power Management Unit	A microcontroller that governs power functions of digital platforms.
PPTC	Polymeric Positive Temperature Coefficient (Poly-switch)	Device that help protect against harmful over-current surges and over-temperature similar to traditional fuses but without permanent sustained damage when exceeding operational limits thus does not need to be replaced.
RGB	Red, Green and Blue	A colour model that represents colours as mixtures of three underlying components, namely: red, green, and blue. Particularly associated in peripherals with backlighting hardware utilising LEDs of these three discrete colours for varied combinational use and appearance customisability at user discretion.
RX	Receiver	Dedicated ProxFusion® inputs which can convert analogue sensor data into Counts.
SMT/SMD	Surface Mount Technology / Surface Mount Device	A method in which the electrical components are mounted directly onto the surface of a printed circuit board. An electrical component mounted in this manner is referred to as a surface-mount device.
	TriggerMax™	A dynamic actuation UI that tracks changes in the Normalised Delta value of channels for which the Normalised Delta exceeds the Activation Threshold.
TX	Transmitter	A pin (any ProxFusion® or specific GPIO) assigned with the capability to output a specific waveform pattern and frequency for excitation of external circuitry.
UI	User Interface	The space where interactions between humans and machines occur.
USB	Universal Serial Bus	An industry standard that establishes specifications for cables, connectors and protocols for connection, communication and power supply (interfacing) between computers, peripherals and other computers.
UX	User Experience	A person's behaviour, attitude, and emotion about using a product, system, or service.
QFN	Quad Flat No-lead	An IC package consisting of a lead frame, single or multiple dies, wire bonds, and moulding compounds.



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