IQS7223C DATASHEET

4 Channel Mutual/Self-capacitive Touch, Proximity and Wear Controller with I²C communications interface, configurable GPIOs and low power options

1 Device Overview

The IQS7223C ProxFusion® IC is a sensor fusion device for various long-term activation or presence detection applications. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in its lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 4 external sensor pad connections
- Dedicated Wear UI for long-term wear or presence detection.
- Advanced environmental tracking for robust detection.
- Power-On detection/sensor activation.
- Off-chip absolute capacitance measurement[i].
- Built-in basic functions:
  - Intelligent wear state output
  - Automatic tuning
  - Noise filtering
  - Debounce and hysteresis
  - Automated system power modes for optimal consumption[ii]
  - I²C communication interface with IRQ/RDY(up to fast plus -1 MHz)
  - Event and streaming modes
- Design simplicity:
  - PC Software for debugging and obtaining optimal settings and performance
- Supply voltage 1.71 V to 3.5 V
- Small packages:
  - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4 mm x 0.6 mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4 mm pitch

QFN20

WLCSP18

1.2 Applications

- Fitness band & smartwatch wear detection
- Headphone wear detection
- TWS earbud wear detection

[i] Absolute capacitance calculations performed by MCU based on data from IQS7223C

[ii] Please refer to product information notice PIN-230172 for more details

1.3 Block Diagram

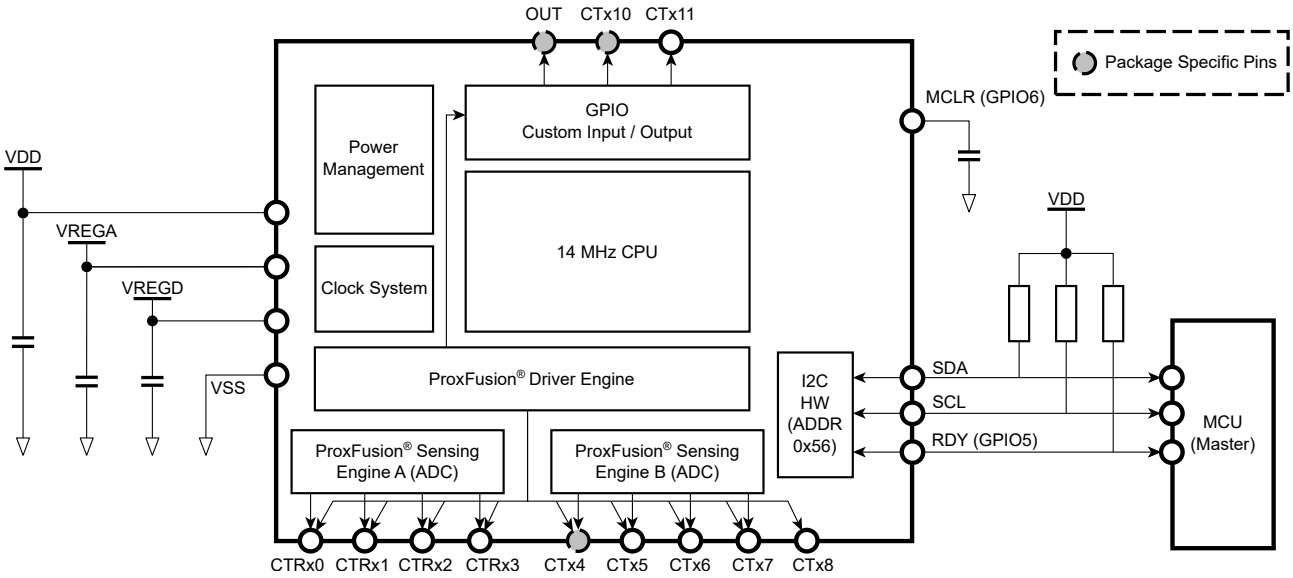


Figure 1.3: Functional Block Diagram[iii]

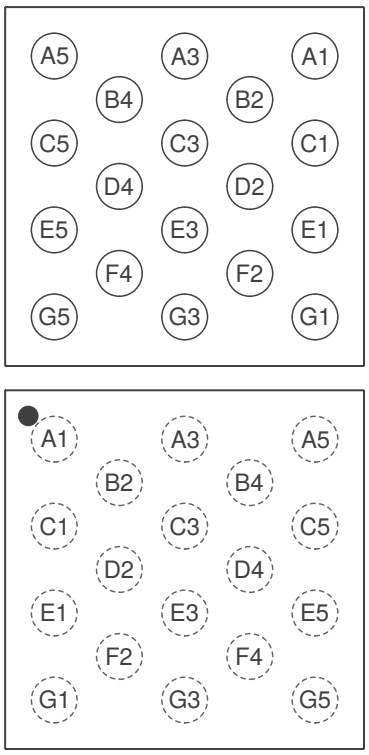
[iii] WLCSP18 packages do not have a CTx4 and combines OUT and CTx10

Contents

2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

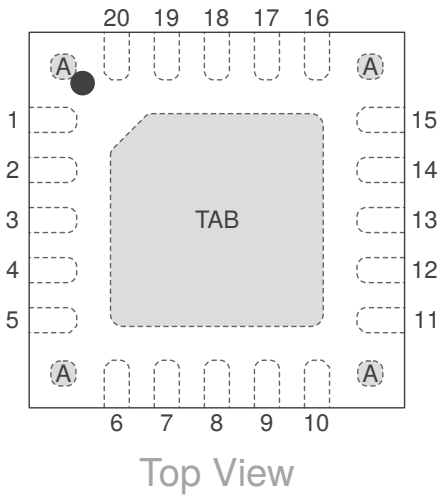
Table 2.1: 18-pin WLCSP18 Package



Pin no.	Signal
A1	OUT/CTx10[i]
A3	SCL
A5	MCLR
B2	CTx11
B4	SDA
C1	CTx8
C3	RDY
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CTx5
F4	CRx0/CTx0
G1	CTx7
G3	CRx3/CTx3
G5	VREGA

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CTx6
2	VREGD	12	CTx7
3	VSS	13	CTx8
4	VREGA	14	OUT
5	CRx0/CTx0	15	CTx10
6	CRx1/CTx1	16	CTx11
7	CRx2/CTx2	17	RDY
8	CRx3/CTx3	18	SCL
9	CTx4	19	SDA
10	CTx5	20	MCLR

Area name	Signal name
TAB[ii]	Thermal pad (floating)
A[iii]	Thermal pad (floating)

[i] Please note that OUT and CTx10 are connected together in the WLCSP18 package.
[ii] It is recommended to connect the thermal pad (TAB) to VSS.
[iii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CTx4	Analog		VREGA
F2	10	CTx5	Analog		VREGA
E1	11	CTx6	Analog		VREGA
G1	12	CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
A1	14	OUT	Digital		VDD
B4	19	SDA	Digital		VDD
A3	18	SCL	Digital		VDD
A1	15	CTx10	Analog		VREGA
B2	16	CTx11	Analog		VREGA
C3	17	RDY	Digital		VDD
A5	20	MCLR	Digital		VDD

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iv]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CTx4	-	9	O	
	CTx5	F2	10	O	
	CTx6	E1	11	O	
	CTx7	G1	12	O	
	CTx8	C1	13	O	CTx8 pad
GPIO	OUT	A1	14	O	OUT pad
	CTx10	A1	15	O	CTx10 pad
	CTx11	B2	16	O	CTx11 pad
	RDY	C3	17	O	RDY pad
	MCLR	A5	20	I	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA	B4	19	IO	I^2C data
	SCL	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[iv] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.5 Hardware Layouts

This section details the supporting passive components required and antenna combinations that may be used.

2.5.1 Reference Schematic

Below is the basic schematic layout for the IQS7223C. Note that the term "antenna" and "electrode" are used interchangeably throughout the document.

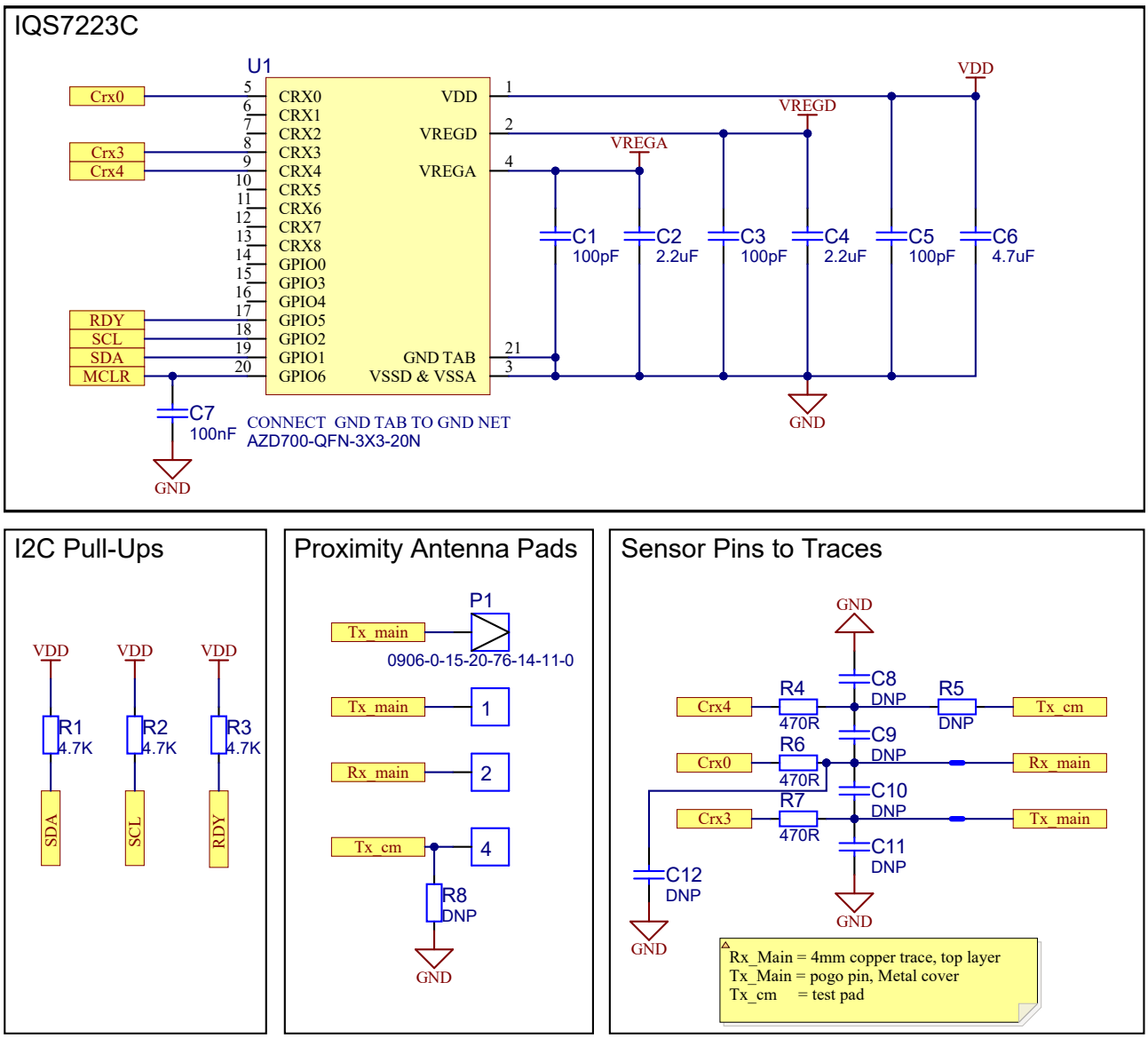


Figure 2.1: Simplified Schematic Design[v]

[v] Although this design makes use of self-capacitive sensing, provision is made for mutual capacitive and differential capacitive sensing with additional sensor pads Crx3 and Crx4.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	–40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz	1.71		3.6	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	2×C_{VREGA}	3×C_{VREGA}		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{CTx–CRx}$	Capacitance between receiving and transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{CRx–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, F_{xfer} = 1 MHz Mutual-capacitance mode, F_{xfer} = 4 MHz			 100[ii] 25[ii]	pF
$\frac{Cp_{CRx–VSS}}{Cm_{CTx–CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.
[ii] RCx = 0 Ω.

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

3.4 Current Consumption

Wear UI Mode Setup: CH0 and CH1: Base = 100, Target = 500
Interface Selection: Event mode

Table 3.4: Typical Current Consumption for IQS7223C001[vi]

Power mode	Active channels	Charge transfer frequency (kHz)	Report rate (Sampling rate) [ms]	Typical current consumption [µA]
NP	Wear UI and Temperature channel	250	20	199.3
	Wear UI and Temperature channel	1000	20	92.4
LP	Wear UI and Temperature channel	1000	100	20.3
ULP	Wear UI and Temperature channel (8 Cycle AutoProx)	1000	100	10.3
	Wear UI and Temperature channel (32 Cycle AutoProx)	1000	100	8.5

[iii] Please note that the maximum values for Cp and Cm are subject to this ratio.
[iv] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.
[v] Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times F_{xfer})}$ where C is the pin capacitance to VSS.
[vi] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.
[vi] Please refer to product information notice PIN-230172 for more details

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

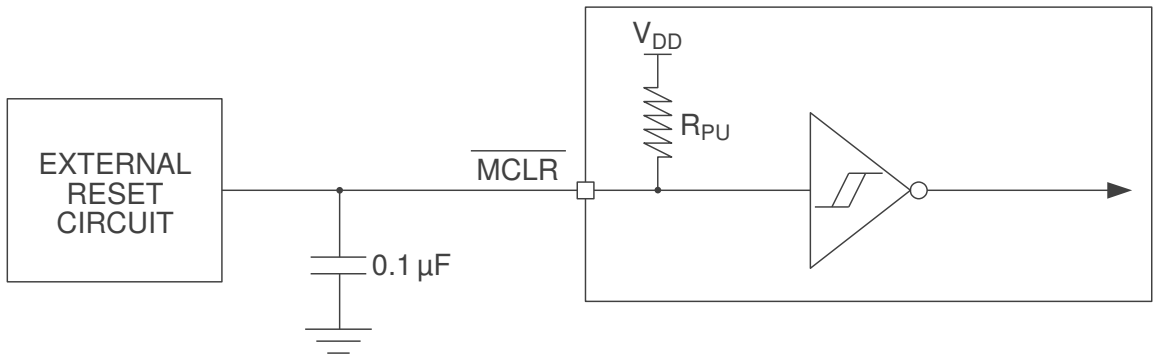


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
F_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
F_{xfer}	Charge transfer frequency (derived from F_{OSC})	42	500 – 1500	3500	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA		0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA		0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2		V
V_{IL}	Input low voltage			VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7		V
C_{b_max}	SDA & SCL maximum bus capacitance			550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

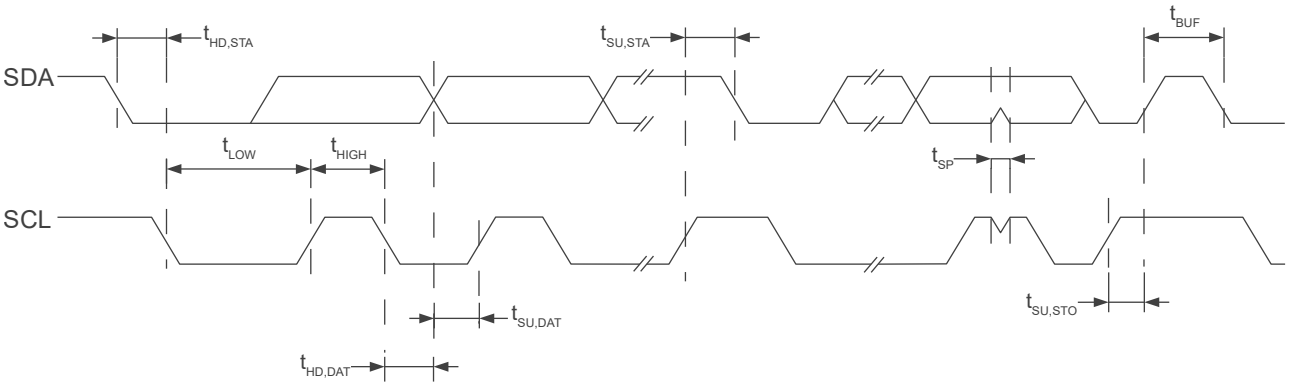


Figure 4.2: I²C Mode Timing Diagram

[i] Refers to OUT, CTx10, CTx11, and RDY pins.

5 Wear UI

The Wear UI provides a novel capacitive sensing solution to maximize sensor sensitivity while maintaining measurement stability across environmental changes.

5.1 Concept

The Wear UI provides low-power functionality even during activation. This is enabled by the high sensitivity of the wear sensor which allows the sensor to differentiate movement in the sensor from environmental changes.

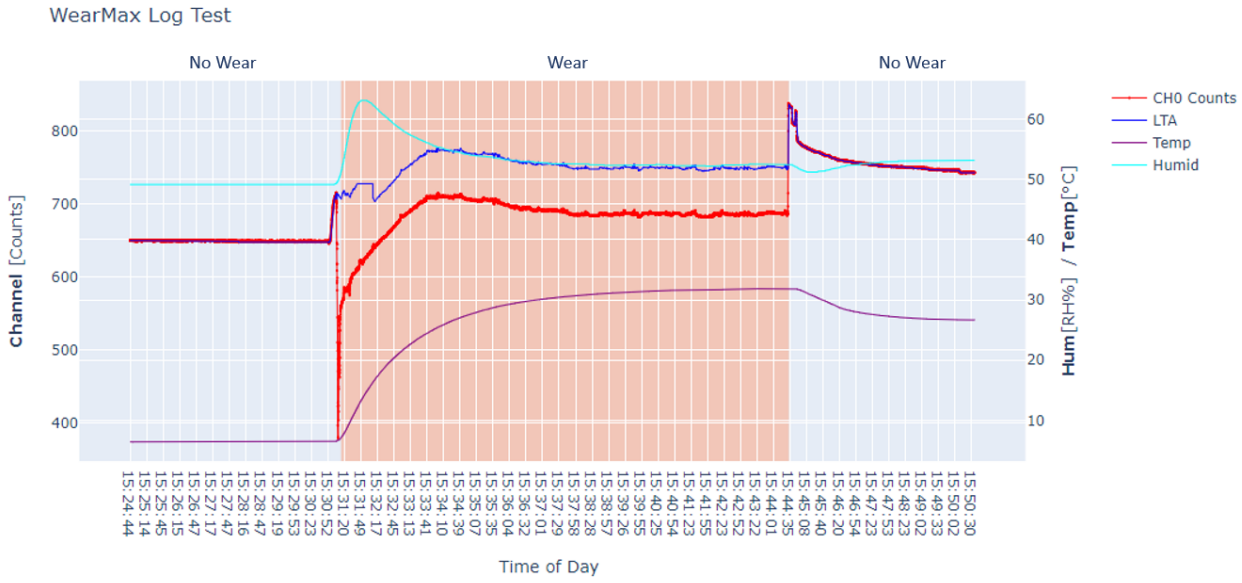


Figure 5.1: Dynamic in-wear threshold adjustment

Figure 5.1 illustrates the performance of the Wear UI by means of a TWS earbud. In the left 'no wear' section, the device was placed in cold environmental conditions at 6 °C, then placed in wear directly after. A delta forms between CH0 counts (red graph) and the LTA (blue graph), indicating the detected wear signal. It can also be seen how the LTA follows the counts signal as it responds to the new body temperature environment of 36.5 °C during wear state. Finally, the earbud is removed and the CH0 counts graph recovers to the LTA graph level, successfully registering a non-wear state.

The detection distance is dependent on the design of the sensor electrodes and the corresponding Wear UI sensitivity augmentation.

The IQS7223C IC can be used in a default setup, where there are four channels present, with a Filter-halt and Activation threshold each. These channels can be changed between a self capacitance, mutual or temperature sensor. When the Wear UI is enabled, Channel 0 is re-purposed as a dedicated wear channel, with additional data-processing added to ensure reliable performance over environmental changes.

The Wear UI can be utilized for a variety of applications, materials and surface area sizes. A separate User Guide is available for the setup of the Wear UI.

6 Absolute Capacitance

The IQS7223C is able to perform self-capacitance measurements and has the ability to enable internal calibration capacitors. These internal calibration capacitors can serve as a reference capacitance, enabling the system MCU to use these capacitors in absolute capacitance measurements.

6.1 Setup Sequence

The internal calibration capacitor can be set to a variety of sizes, which allows these absolute capacitance calculations to be easily tailored to the electrode used in the application. Absolute capacitance measurements are performed over multiple cycles and needs to be setup manually by the system MCU.

To perform an absolute capacitance measurement, the following steps needs to be implemented on the system MCU:

- Set up a self capacitance channel and selected the appropriate CRx pins.
- Set the channel's calibration capacitor to 0pF.
- Set the channel's ATI base to 100 counts and the ATI target to 1000 counts.
- ATI the channel.

6.2 Measurement Sequence

Following the setup routine, the measurement routine will need to be setup and logged by the system MCU to calculate the absolute capacitance:

- **1. Setup the channel for an Absolute capacitance measurement**
  - Log the channel's ATI compensation value.
  - Set the channel's ATI mode to disabled.
- **2. No Compensation measurement:**
  - Ensure the calibration capacitor is set to 0pF.
  - Sample the channel's counts ($Count_{base}$) with the compensation's set to zero.
- **3. No CalCap with Compensation measurement:**
  - Set the channel's compensation to the logged value.
  - Ensure the calibration capacitor is set to 0pF.
  - Sample the channel's counts ($Count_{zero}$).
- **4. Calibration capacitor measurement:**
  - Set the calibration capacitor to the channel specific setting ($Capacitor\ Size$).
  - Sample the channel's counts ($Count_{predefined}$).

6.3 Capacitance Calculation

Once the measurement sequence in section 6.2 has been performed by the system MCU, the following calculations need to be performed on the system MCU:

- **1. Linearize Counts:** Calculate the linearized count value for each measurement result.

$$L_{Base} = \frac{2^{20}}{Count_{Base}} \quad L_{Zero} = \frac{2^{20}}{Count_{Zero}} \quad L_{Predefined} = \frac{2^{20}}{Count_{Predefined}}$$

- **2. Count to pF Relation:** Find the linearized count per pF.

$$\frac{\Delta L}{\Delta C} = \frac{(L_{Predefined} - L_{Zero})}{Capacitor\ Size}$$

- **3. Load Capacitance in pF:** Calculate the load capacitance in pF.

$$C_{Load} = \frac{(L_{Base})}{\frac{\Delta L}{\Delta C}}$$

6.4 Design Considerations

The channels used in the absolute capacitance measurements functions as self capacitance channels that are sampled periodically according to the power mode of the device. The absolute capacitance sequence is only executed upon request by the system MCU.

Depending on the application, these channels can be advantageously applied to calculate two separate absolute load capacitance values. By routing a reference and a signal trace, a robust detection method can be provided to supplement the independent Wear UI sensor also offered by this device.

Design guidelines for wear detection with self capacitance can be found in AZD110: Wear Detection Application Note.

7 ProxFusion® Module

7.1 Low Power Options

The IQS7223C offers four customizable power modes:

- Normal power mode (NP)
  - Highest power mode, aimed at measuring user interaction windows.
- Low power mode (LP)
  - Typically set to a slower rate than NP
  - Automatically selected if the sensor state has stabilized
- Ultra Low power mode (ULP)[i]
  - CH0 is measured at the selected LP interval, with the other channels only measured every *Auto Prox* amount of CH0 measurements.
  - Automatically selected if the sensor state has stabilized for a long period
- Halt Mode
  - Lowest possible power consumption.
  - State entered and exited through MCU command.
  - No capacitance measurements are completed.

The system MCU can select either NP, LP, Halt or automatic power mode through the *Power Mode* register. In automatic power mode, the IQS7223C automatically switches from NP mode, to LP and eventually ULP mode, as long as the "Switch to NP" flag is not set. The conditions which sets the "Switch to NP" flag can be configured through *Power Mode switch* register as follows:

- Switch to NP mode upon movement on channel 0.
- Switch to NP mode upon an event on of the channels (Channel events are maskable)
- Stay in NP mode when an event is active on any of the channels (Channel states are maskable)

The channel events/states are maskable per channel and per event level (Filter-halt/Activation), see the *Power Mode switch mask* register.

7.2 Count Value

The capacitive sensing measurement returns a *count value* for each channel. Count values are inversely proportional[ii] to capacitance, and all outputs are derived from this.

7.2.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit *(Maximum_Counts)*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

7.3 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

[i] Please refer to product information notice PIN-230172 for more details
[ii] Unless 'linearized counts' is set in the device settings

7.4 Counts and LTA Filters

An IIR filter is applied to the digitized raw input to offer various damping options of the counts, as well as to calculate a Long-Term-Average (LTA). These damping options can be adjusted per sensing mode, as defined in Table A.7, Table A.8 and Table A.9

Damping factor = Beta/256

7.4.1 Reseed

Since the *LTA* for each channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (See section 11).

7.5 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

7.6 Automatic Re-ATI

7.6.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7223C, a status bit will be set momentarily to indicate that its occurrence.

7.6.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the LTA of a channel drifts outside the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.24.

$$\textbf{Re-ATI Boundary}_{\textbf{default}} = \textbf{ATI target} \pm (\tfrac{1}{16}\textbf{ATI Target})$$

For example, assume that the ATI target is configured to 800 and the default boundary value is 1/16*800 = 50. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

LTA > 850 or LTA < 750

The ATI algorithm execution is near instantaneous and will not be noticed by the user.

7.6.3 ATI Error

After the ATI algorithm is performed, a check is done to determine whether an error occurred within the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation $\geq$ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should, however, not occur under normal circumstances.

8 Hardware Settings

Hardware-specific settings and the ProxFusion® Module's charge transfer characteristics can be adjusted.

Certain hardware settings are described below. Please refer to AZD130 for hardware setup.

8.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the IQS7223C GUI, where the relative parameters are provided (Refer to *Charge Transfer frequency* for more information). For high resistance sensors, it might be needed to decrease f_{xfer}.

8.2 Reset

8.2.1 Reset Indication

After a reset, the *(Reset)* bit will be set by the system to indicate that the reset event occurred. This bit will clear when the master sets the *(Ack Reset)*. If it becomes set again, the master will know a reset has occurred and can react appropriately.

8.2.2 Software Reset

The IQS7223C can be reset by means of an I^2C command (*Soft Reset*).

9 Additional Features

9.1 Power-On Detection

The device provides power-on detection functionality. This detection must be manually requested upon any reset condition by the application. This is done when the master sets the *Ack Reset* bit as described in 8.2.1. The device will only start sampling once this request is performed.

After Power-On Detection is requested, the Wear State Output MM will return "Undefined" until the Power-On detection is complete. Thereafter, the determined state will be persistent in the Memory Map. Refer to the IQS7223C User Guide document for more information on the power-on detection feature.

9.2 Compensation Adjustment

When using the Follow UI's ATI parameter tracking functionality (*Follow ATI Parameters*), it is possible to implement a compensation adjust parameter to better match two channels. This scales the compensation value of the reference with the compensation adjust parameter (*Compensation Adjustment*) to the following channel. This provides a fine tune parameter to correct small imbalances between the signal and reference electrodes. Note that for temperature sensitive applications, large imbalances will negatively affect the overall sensor performance and cannot be compensated for with this adjustment alone.

9.3 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (Low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.
- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.

9.4 RF Immunity

The IQS7223C has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are recommended on V_{REG} and V_{DDHI}.

Place a 100pF in parallel with the 2.2μF ceramic on V_{REG}. Place a 2.2μF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads. Note that these are the effective capacitance values, i.e. after considering capacitor derating.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the electrode pads. Normally these are in the range of 100Ω-1kΩ. PCB ground planes also improve noise immunity.

10 I²C Interface

10.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The communications interface of the IQS7223C supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as a configurable event mode.
- The provided interrupt line (RDY) is an open-drain, active-low implementation and indicates a communication window.

The IQS7223C implements 8-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

10.2 I²C Address

The default 7-bit device address is 0x56 ('1010110'). The full address byte will thus be 0xAD (read) or 0xAC (write).

Other address options exist on special request. Please contact Azoteq.

10.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

10.4 Memory Map Addressing

10.4.1 8-bit Address

The memory map implements an 8-bit addressing scheme for the required user data.

10.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

The h-file generated by the GUI will display the start address of each block of data, with each address containing 2 bytes. The data of all the addresses can be written consecutively in a single block of data or the entire memory map, or data can be written explicitly to a specific address. An example of the h-file exported by the GUI and the order of the data, is shown in Fig. 10.1 below.

```
/* Change the Report Rates and Timing */
/* Memory Map Position 0x84 - 0x89 */
#define ATI_MODE_0                              0xD0
#define ATI_MODE_1                              0x07
#define ATI_PERIOD_0                            0x00
```

Figure 10.1: Example of an H file exported by the GUI

10.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. This, however, should be avoided since the corresponding data was missed/lost. The default I²C timeout period is set to 10 ms and can be adjusted in register 0x83. However, the recommended period for most applications is 500 ms.

10.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 5 register 0x80) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

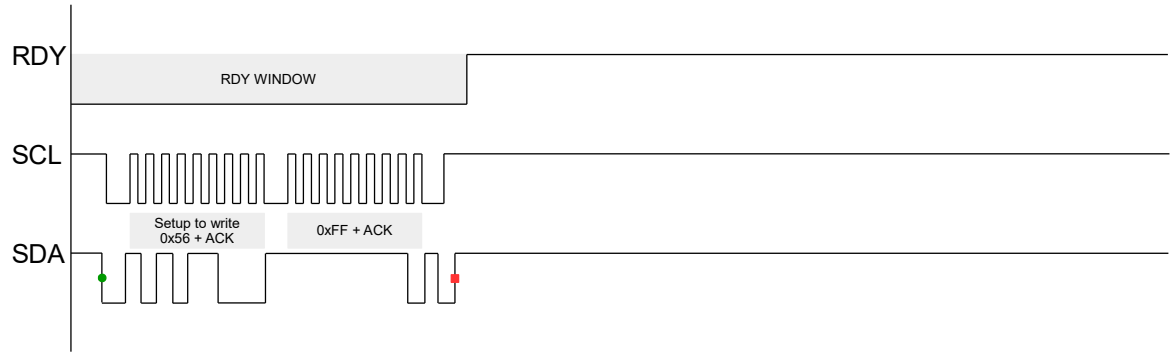


Figure 10.2: Force Stop Communication Sequence

10.8 RDY/IRQ

The communication has an open-drain active-low RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep allowing wake-up from the touch device when user presence is detected. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

10.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside a communication window (i.e. while RDY = high)

10.10 Event Mode Communication

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). Enabling event mode will ensure that the master MCU is not needlessly interrupted. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

10.10.1 Events

The following events can be individually enabled to trigger communication:

- Power mode change
- Filter-halt or Activation event
- ATI Event
- In-Wear ATI Error
- Wear State change Event

10.10.2 Force Communication / Polling

In streaming mode, the IQS7223C I^2C will provide Ready (RDY) windows at intervals specified in the power mode report rate. Ideally, communication with the IQS7223C should only be initiated in a Ready window but a communication request described in figure 10.3 below, will force a Ready window to open. In event mode Ready windows are only provided when an event is reported and a Ready window must be requested to write or read settings outside of this window. The time between the communication request and the opening of a RDY window (t_{wait}), is dependent on the report rate of the current power mode. t_{wait} can extend up to the current report rate +20% due to variability in the clock. Example, if a report rate of 100ms is chosen, the report rate may vary between 80ms and 120ms [i].

There is a possibility of a communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period. However, it is essential to retry at different timings that are not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional precautionary measure, the IC can be reset using the MCLR pin and reinitialized if there is no response after a specified number of retries.

A force communication request should be avoided while RDY is in the LOW state. If a communication request is sent at the exact moment when an event causes RDY to go low, the window will close again after sending the I^2C STOP signal. In such a scenario, the device will provide an invalid communication response (0xEE) because the host is attempting to read from the device outside of a communication window (i.e. while RDY is high). To prevent this issue, it is recommended to read the product number during each ready window to ensure that the response received is valid.

A slight delay may occur in receiving an acknowledgement (ACK) when attempting force communication while the device is in an internal lower power mode with certain peripherals switched off. This delay can occur regardless of the state of the current system power mode.

The communication request sequence is shown in figure 10.3 below.

[i] Please contact Azoteq for an application specific value of t_{wait}

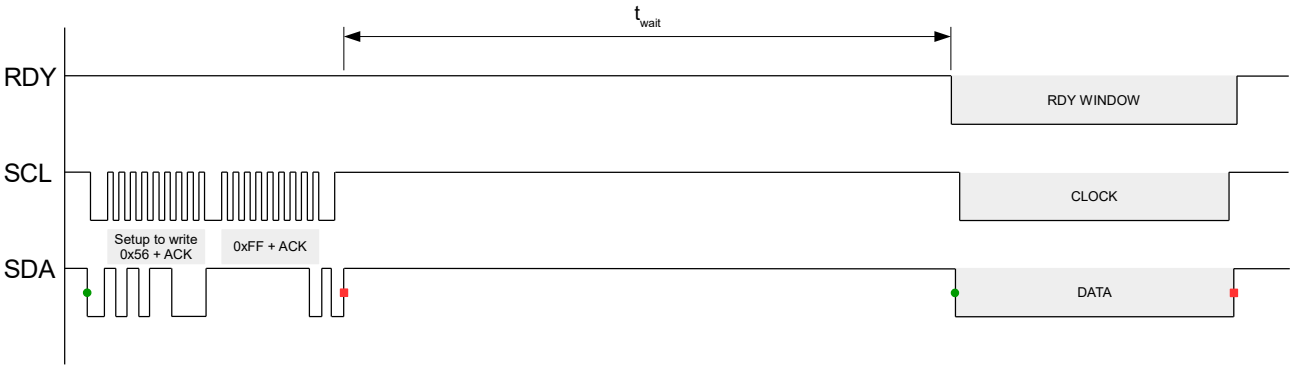


Figure 10.3: Force Communication Sequence

11 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
	Device Status	
0x10	System Fields	See Table A.2
0x11	PXS Status	See Table A.3
	Channel Counts	
0x12	Channel 0 Filtered	16-bit value
0x13	Channel 1 Filtered	
0x14	Channel 2 Filtered	
0x15	Channel 3 Filtered	
0x16	Channel 0 LTA	
0x17	Channel 1 LTA	
0x18	Channel 2 LTA	
0x19	Channel 3 LTA	
0x1A	CH0 Positive Gradient	
0x1B	CH0 In Wear LTA	
0x1C	Reserved	Reserved
0x1D	CH0 Negative Gradient	16-bit value
	Follow UI Settings	
0x30	Channel 0 Follow Settings	See Table A.4
0x31	Channel 1 Follow Settings	
0x32	Channel 2 Follow Settings	
0x33	Channel 3 Follow Settings	
0x34	Channel 0 Follow Weight	See Table A.5
0x35	Channel 1 Follow Weight	
0x36	Channel 2 Follow Weight	
0x37	Channel 3 Follow Weight	
0x38	Channel 0 Compensation Adjustment Ratio	See Table A.6
0x39	Channel 1 Compensation Adjustment Ratio	
0x3A	Channel 2 Compensation Adjustment Ratio	
0x3B	Channel 3 Compensation Adjustment Ratio	
	Measurement Settings	
0x40	Self Capacitance Beta values	See Table A.7
0x41	Self Capacitance Beta values	See Table A.8
0x42	Mutual Capacitance Beta values	See Table A.9
0x43	Mutual Capacitance Beta values	See Table A.10
0x44	Self Capacitance measurement settings	See Table A.11
0x45	Mutual Capacitance measurement settings	
	ATI Parameters	
0x60	Channel 0 Fine and Coarse Multipliers	See Table A.12
0x61	Channel 0 ATI Compensation	See Table A.13
0x62	Channel 1 Fine and Coarse Multipliers	See Table A.12
0x63	Channel 1 ATI Compensation	See Table A.13
0x64	Channel 2 Fine and Coarse Multipliers	See Table A.12
0x65	Channel 2 ATI Compensation	See Table A.13
0x66	Channel 3 Fine and Coarse Multipliers	See Table A.12
0x67	Channel 3 ATI Compensation	See Table A.13

	Wear Detect settings	
0x70	General Wear Detect settings	See Table A.14
0x71	ATI Delay time	16-bit value (ms)
0x72	Wear Settle time	16-bit value (ms)
0x73	Wear Beta Values	See Table A.15
0x74	Positive Gradient Trip threshold	16-bit value
0x75	Negative Gradient Trip threshold	16-bit value
0x76	Temperature tracking ratio	See Table A.16
0x77	Channel 0 Out of Wear Target Value	16-bit value
0x78	Channel 0 Wear Threshold Value	See Table A.17
	PMU and System Settings	
0x80	System Setup and Commands	See Table A.18
0x81	Watchdog Timeout and Event Mode mask	See Table A.19
0x82	Power Mode state change mask	See Table A.20
0x83	I2C timeout	16-bit value (ms)
0x84	Retry ATI on error period	16-bit value (ms)
0x85	Minimum ATI sample period	16-bit value (ms)
0x86	Normal Power Mode Timeout	16-bit value (ms)
0x87	Normal Power Mode Report Rate	16-bit value (ms)
0x88	Low Power Mode Timeout	16-bit value (ms)
0x89	Low Power Mode Report Rate	16-bit value (ms)
	Channel 0 PXS, ATI Settings and Detection Settings	
0xA0	Filter-halt State Timeout	16-bit value (ms)
0xA1	Activation State Timeout	16-bit value (ms)
0xA2	Filter-halt Threshold	16-bit value
0xA3	Filter-halt Debounce	See table A.21
0xA4	Activation Threshold	See table A.22
0xA5	Activation Hysteresis	See table A.23
0xA6	General sensor settings	See table A.24
0xA7	Sensor measurement settings	See table A.25
0xA8	Conversion Frequency settings	See table A.26
0xA9	ATI Base value	16-bit value
0xAA	ATI Target value	16-bit value
0xAB	Sensor input selection	See table A.27
0xAC	Offset current selection	See table A.28
0xAD	CTx Selection	See Table A.29
0xAE	CM CTx Selection	See Table A.30
	Channel 1 PXS, ATI Settings and Detection Settings	
0xB0	Filter-halt State Timeout	16-bit value (ms)
0xB1	Activation State Timeout	16-bit value (ms)
0xB2	Filter-halt Threshold	16-bit value
0xB3	Filter-halt Debounce	See table A.21
0xB4	Activation Threshold	See table A.22
0xB5	Activation Hysteresis	See table A.23
0xB6	General sensor settings	See table A.24
0xB7	Sensor measurement settings	See table A.25
0xB8	Conversion Frequency settings	See table A.26
0xB9	ATI Base value	16-bit value
0xBA	ATI Target value	16-bit value
0xBB	Sensor input selection	See table A.27
0xBC	Offset current selection	See table A.28

0xBD	CTx Selection	See Table A.29
0xBE	Charge reduction CTx Selection	See Table A.30
	Channel 2 PXS, ATI Settings and Detection Settings	
0xC0	Filter-halt State Timeout	16-bit value (ms)
0xC1	Activation State Timeout	16-bit value (ms)
0xC2	Filter-halt Threshold	16-bit value
0xC3	Filter-halt Debounce	See table A.21
0xC4	Activation Threshold	See table A.22
0xC5	Activation Hysteresis	See table A.23
0xC6	General sensor settings	See table A.24
0xC7	Sensor measurement settings	See table A.25
0xC8	Conversion Frequency settings	See table A.26
0xC9	ATI Base value	16-bit value
0xCA	ATI Target value	16-bit value
0xCB	Sensor input selection	See table A.27
0xCC	Offset current selection	See table A.28
0xCD	CTx Selection	See Table A.29
0xCE	Charge reduction CTx Selection	See Table A.30
	Channel 3 PXS, ATI Settings and Detection Settings	
0xD0	Filter-halt State Timeout	16-bit value (ms)
0xD1	Activation State Timeout	16-bit value (ms)
0xD2	Filter-halt Threshold	16-bit value
0xD3	Filter-halt Debounce	See table A.21
0xD4	Activation Threshold	See table A.22
0xD5	Activation Hysteresis	See table A.23
0xD6	General sensor settings	See table A.24
0xD7	Sensor measurement settings	See table A.25
0xD8	Conversion Frequency settings	See table A.26
0xD9	ATI Base value	16-bit value
0xDA	ATI Target value	16-bit value
0xDB	Sensor input selection	See table A.27
0xDC	Offset current selection	See table A.28
0xDD	CTx Selection	See Table A.29
0xDE	Charge reduction CTx Selection	See Table A.30

12 Implementation and Layout

12.1 Layout Fundamentals

Note: Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

12.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

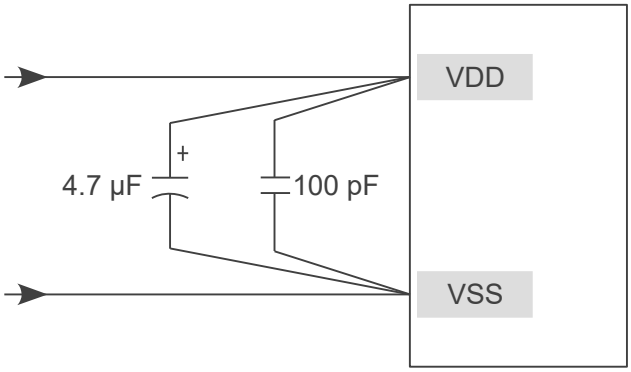


Figure 12.1: Recommended Power Supply Decoupling

12.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. Figure 12.2 below shows an example placement of the VREG capacitors.

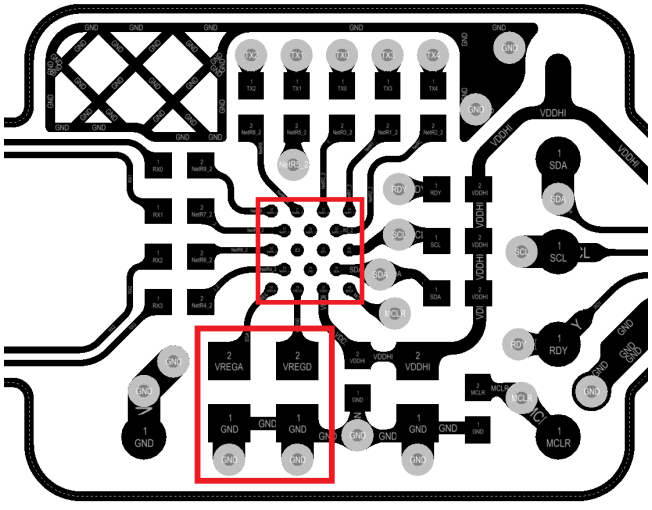


Figure 12.2: VREG Capacitor Placement Close to IC

12.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

13 Ordering Information

13.1 Ordering Code

IQS7223C zzz ppb

Table 13.1: Order Code Description

IC NAME				IQS7223C
CONFIGURATION	zzz	=	001	I^2C with initialize settings requirement
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
			QF	QFN-20 package
			QN	QFN-20 package (On special order only[i])
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000 pcs/reel) QFN-20 Reel (2000 pcs/reel)

Example : IQS7223C001QFR

13.2 Top Marking

13.2.1 WLCSP18 Package Marking (IQS7223C001CSR)

Package outline can be found in Section 14.5.

Product Name
ppp = product code
xx = batchcode

13.2.2 QFN20 Package Marking Option 1 (IQS7223C001QFR)

Package outline can be found in Section 14.1.

Product Name
ppp = product code
xx = batchcode

[i] Special order codes are subject to larger minimum order quantities, longer lead times and are non-cancelable, non-returnable.

13.2.3 QFN20 Package Marking Option 2 (IQS7223C001QNR)

Package outline can be found in Section 14.3.

Product Name
ppp = product code
xx = batchcode

14 Package Specification

14.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

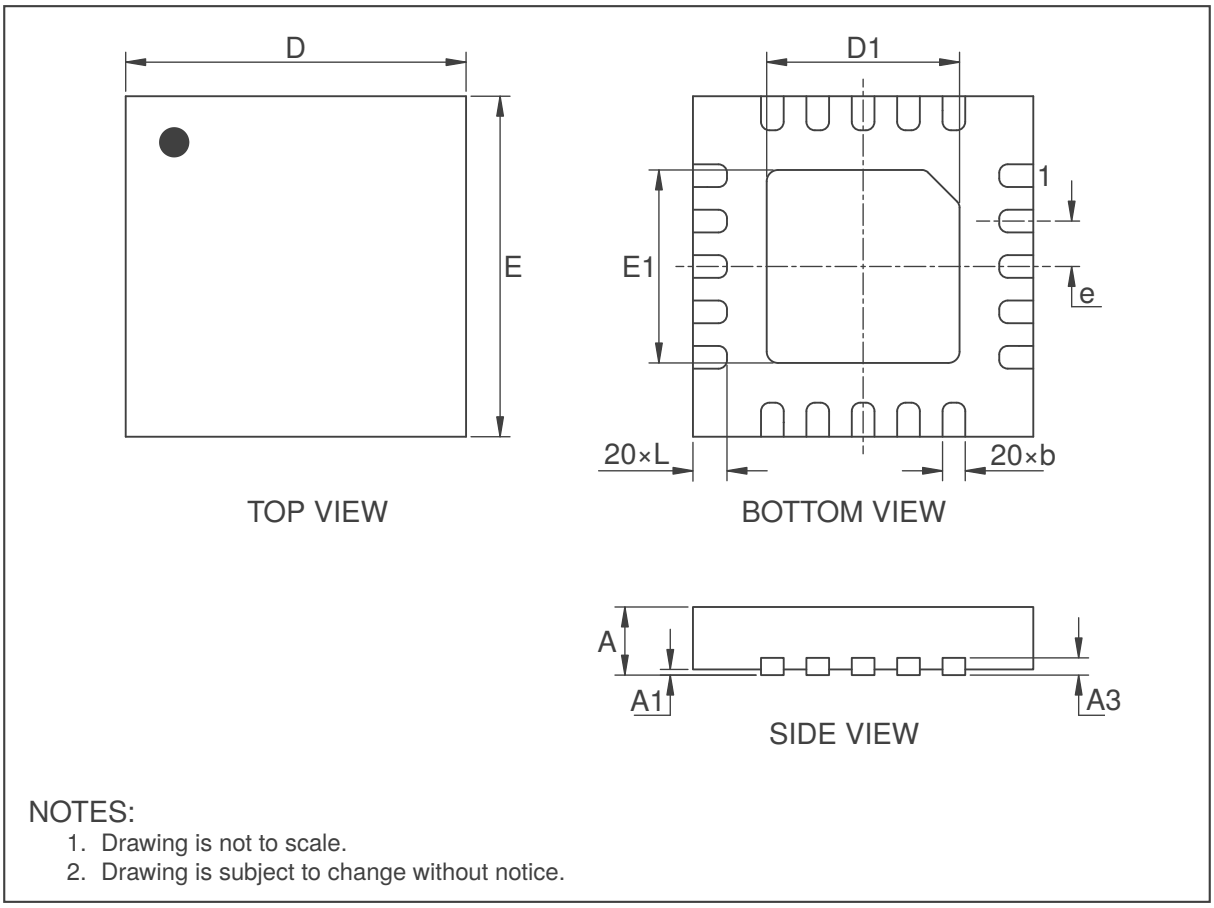
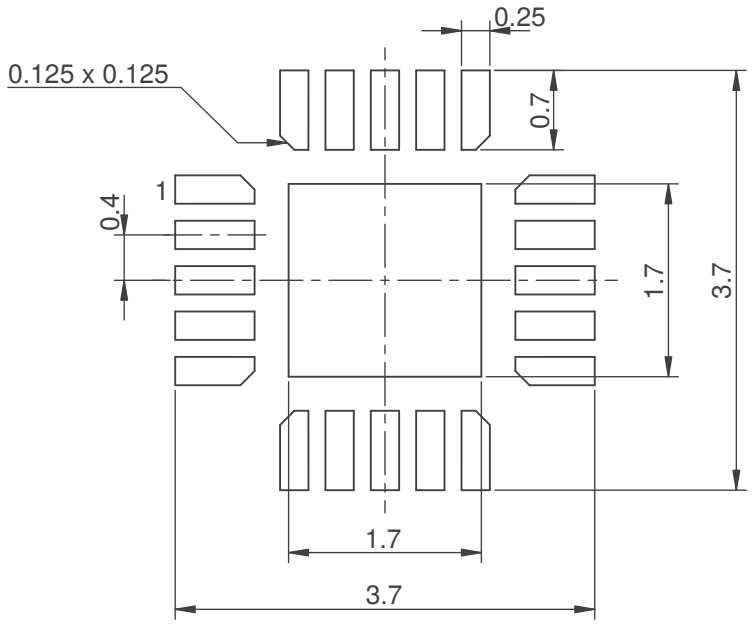


Figure 14.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

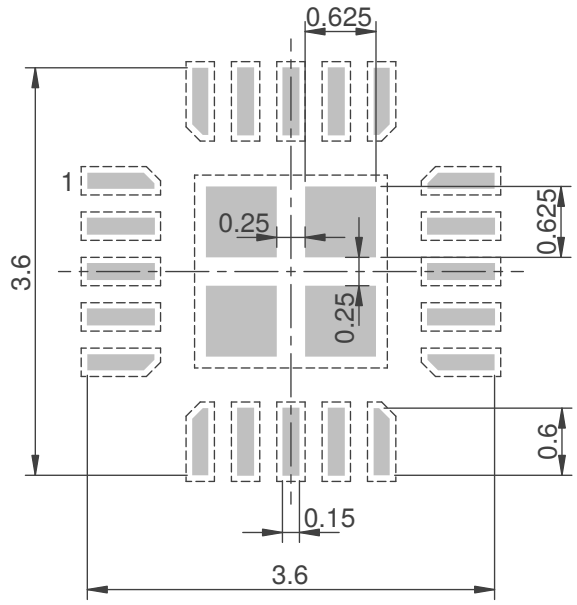
Table 14.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

14.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 14.2: QFN (3x3)-20 (QFR) Recommended Footprint

14.3 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

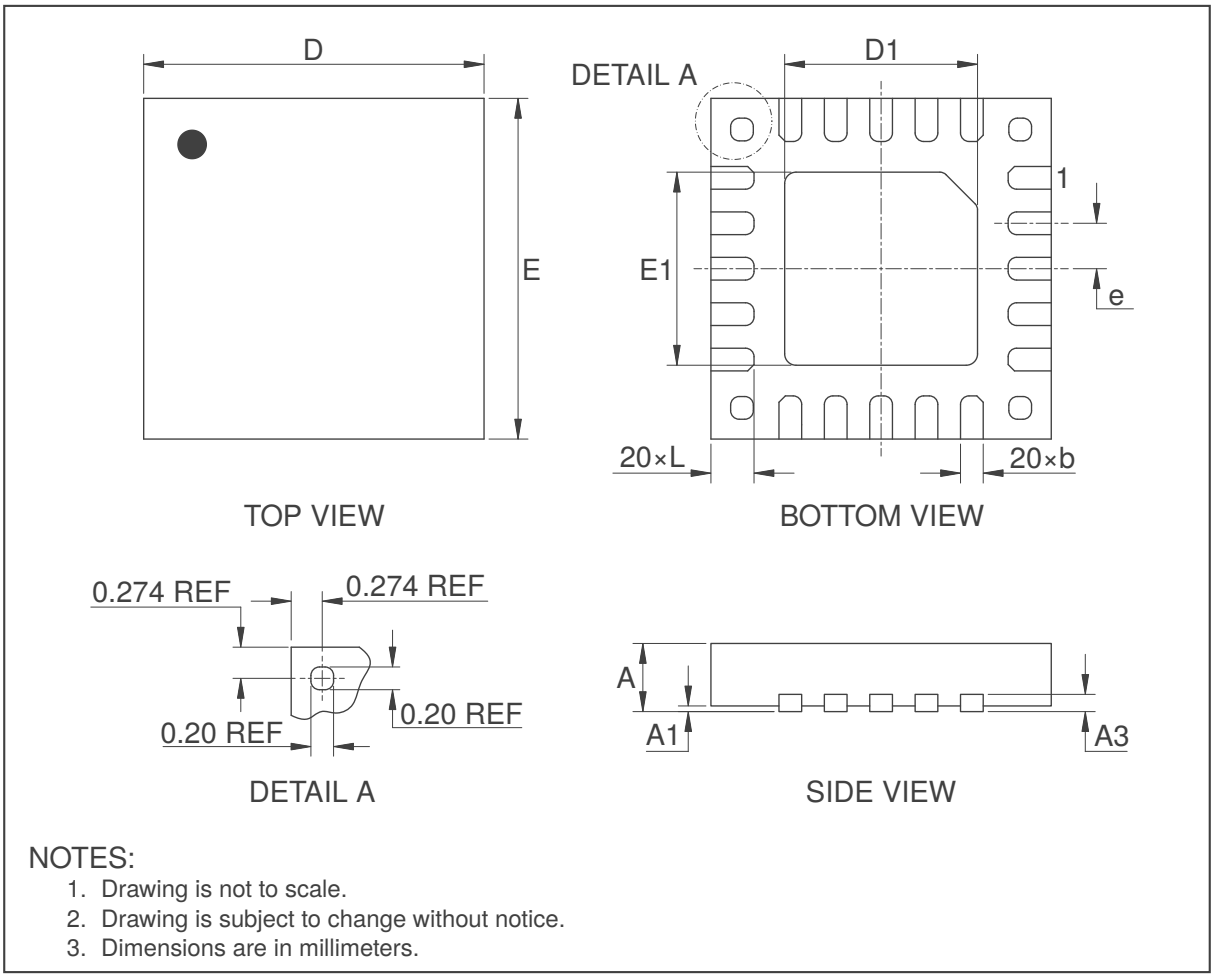
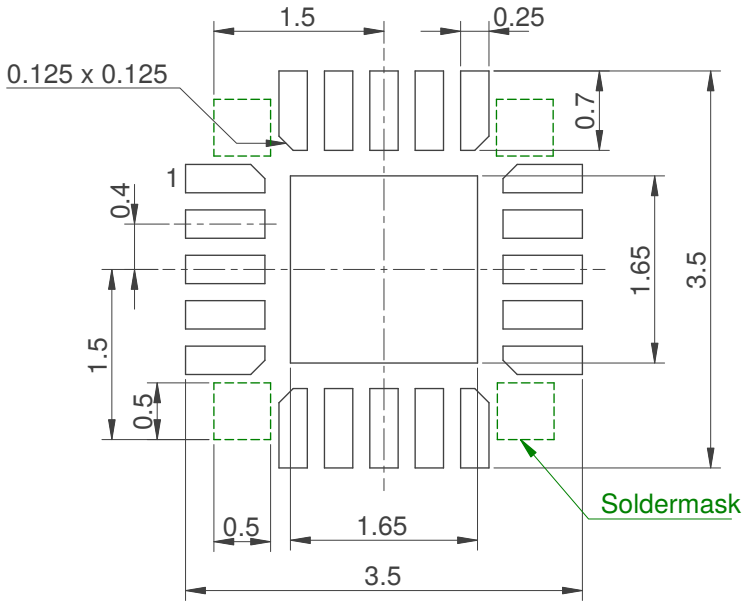


Figure 14.3: QFN (3x3)-20 (QNR) Package Outline Visual Description

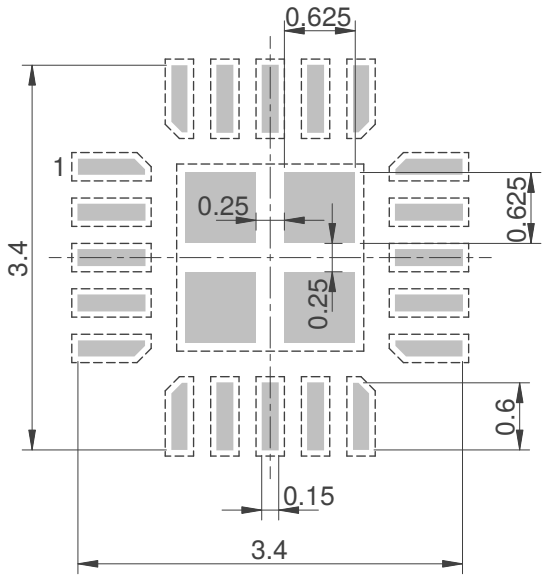
Table 14.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

14.4 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 14.4: QFN (3x3)-20 (QNR) Recommended Footprint

14.5 Package Outline Description – WLCSP18

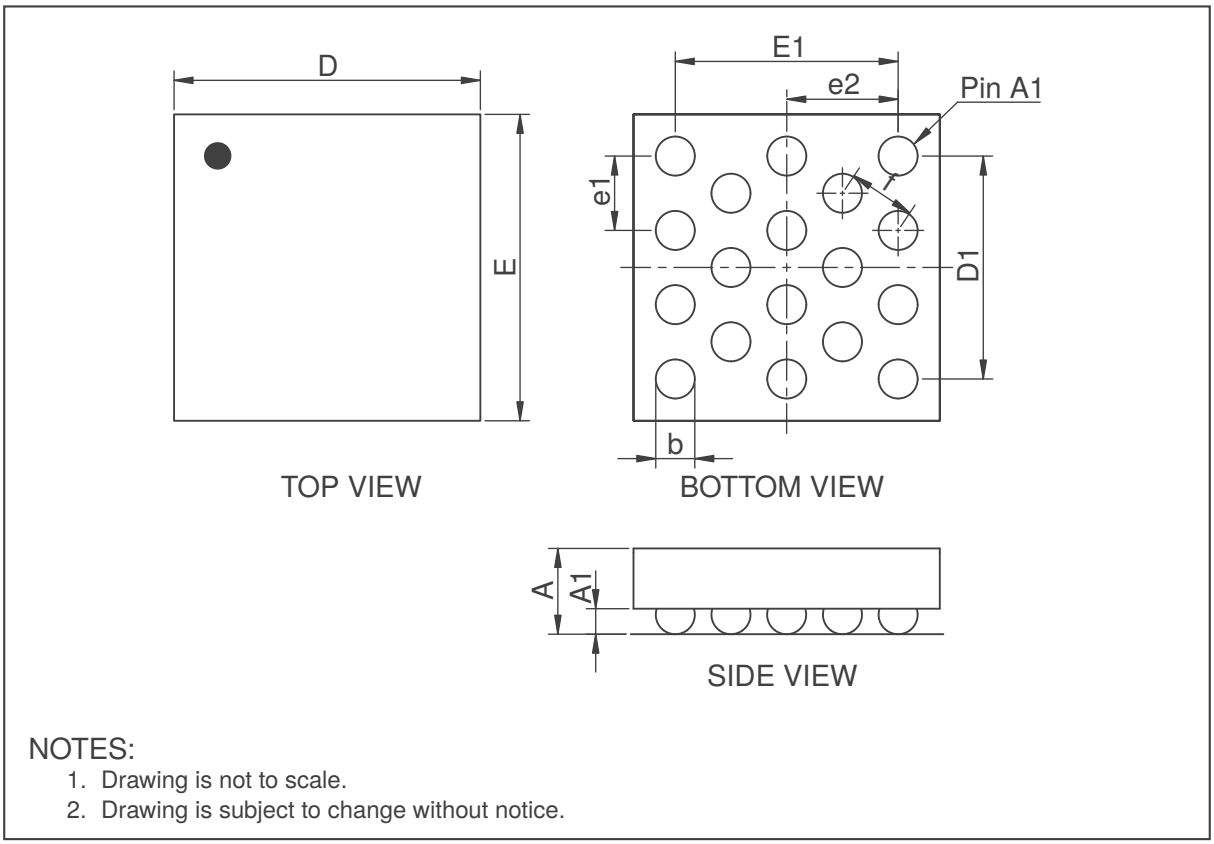
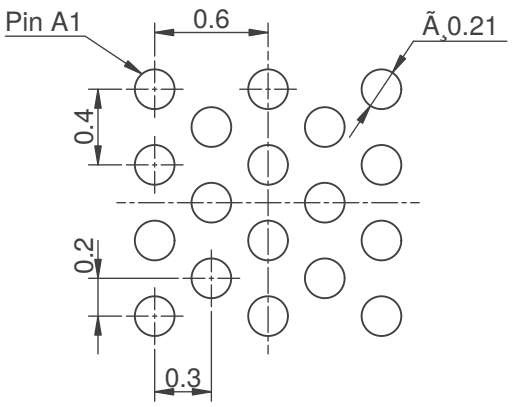


Figure 14.5: WLCSP (1.62x1.62)-18 Package Outline Visual Description

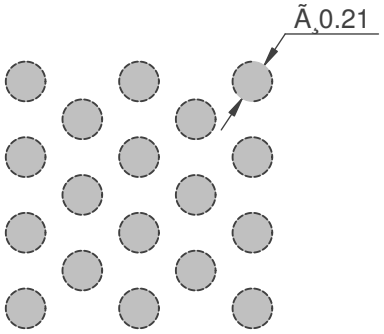
Table 14.3: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1	1.200 BSC		
E1	1.200 BSC		
e1	0.400 BSC		
e2	0.600 BSC		
f	0.360 REF		

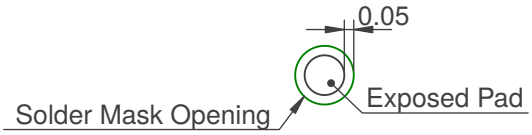
14.6 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



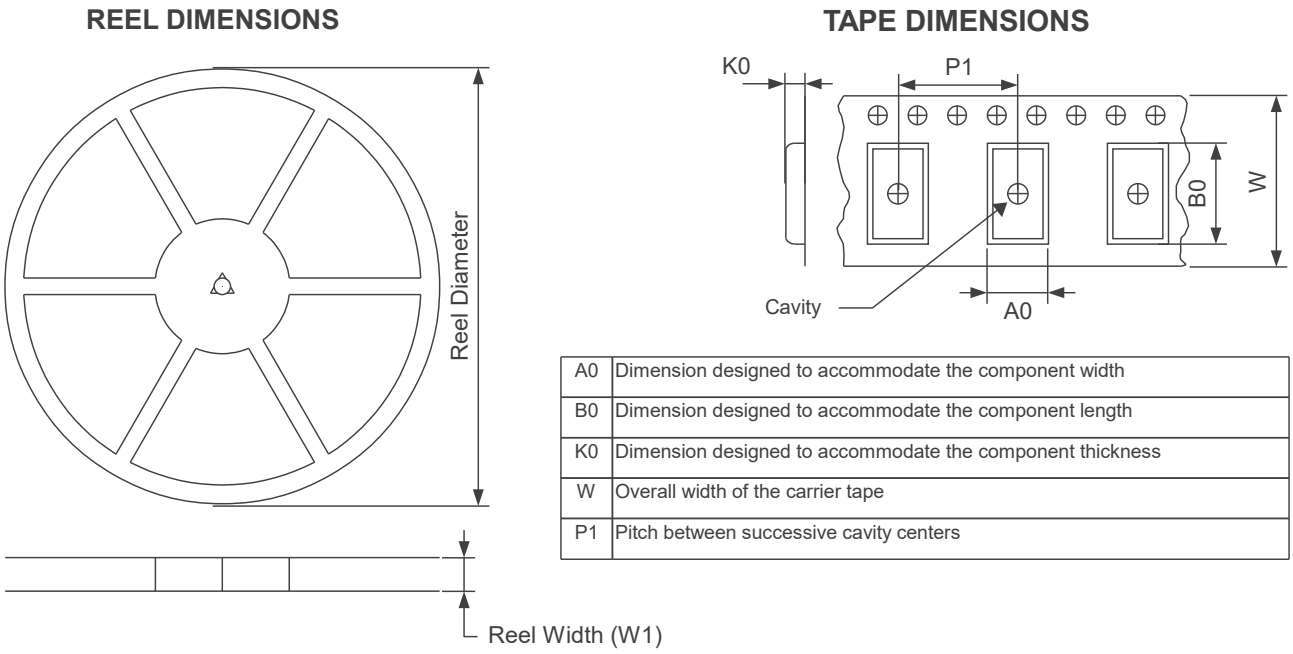
SOLDER MASK BACK-OFF

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 14.6: WLCSP18 Recommended Footprint

14.7 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 14.7: Tape and Reel Specification

Table 14.4: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2
WLCSP18	18	179	8.4	1.78	1.78	0.69	4	8	Q1

14.8 Moisture Sensitivity Levels

Table 14.5: Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

14.9 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Please note: The value of all Read-write bits marked as Reserved, unless otherwise specified, can be set to 0 or 1 depending on customer's preference.

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Catergory	Name	Value	Order Code	
0x00	Application Version Info	Product Number	1064		16-bit value
0x01		Major Version	1		
0x02		Minor Version	0	001	
0x03		Patch Number (commit hash)	Reserved		
0x04					
0x05	ROM Library Version Info	Library Number	Reserved		
0x06		Major Version	Reserved		
0x07		Minor Version	Reserved		
0x08		Patch Number (commit hash)	Reserved		
0x09					

Table A.2: System Flags

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Res	Wear State	Power Mode		Reset	De-bounce	ATI Error	ATI Active	In-Wear ATI Fail	In-Wear	Res	Wear Re-lease	CH Acti-vation	CH Filter Halt	Power	ATI

- Bit 14: **Wear State**
  - 0: Wear not active
  - 1: Wear active
- Bit 12-13: **Power Mode**
  - 00: Normal Power Mode
  - 01: Low Power (LP) Mode
  - 10: Ultra Low Power (ULP) Mode
  - 11: Halt Mode
- Bit 11: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 10: **Debounce Active**
  - 0: Debounce is not Active
  - 1: Debounce is Active
- Bit 9: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 8: **ATI Active**
  - 0: ATI not active
  - 1: ATI active
- Bit 7: **In-Wear ATI Fail**
  - 0: No in-wear ATI failure occurred
  - 1: An in-wear ATI failure occurred
- Bit 6: **In-Wear Event**
  - 0: In Wear event did not occur
  - 1: In Wear event occurred
- Bit 4: **Wear Release Event**
  - 0: Wear Release Event did not occur
  - 1: Wear Release Event occurred
- Bit 3: **Channel Activation Event**
  - 0: Channel Activation did not occur
  - 1: Channel Activation occurred
- Bit 2: **Channel Halt Event**
  - 0: Channel Halt Event did not occur
  - 1: Channel Halt Event occurred
- Bit 1: **Power Mode Event**

- 0: Power Mode Event did not occur
- 1: Power Mode Event occurred

› Bit 0: **ATI Event**
- 0: ATI Event did not occur
- 1: ATI Event occurred

Table A.3: Channel Status

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				CH3 Activation	CH2 Activation	CH1 Activation	CH0 Activation	Reserved		Move	Settled	CH3 Filter Halt	CH2 Filter Halt	CH1 Filter Halt	CH0 Filter Halt

› Bit 11: **CH3 Activation**
- 0: CH3 is not Active
- 1: CH3 is Active

› Bit 10: **CH2 Activation**
- 0: CH2 is not Active
- 1: CH2 is Active

› Bit 9: **CH1 Activation**
- 0: CH1 is not Active
- 1: CH1 is Active

› Bit 8: **CH0 Activation**
- 0: CH0 is not Active
- 1: CH0 is Active

› Bit 5: **Move**
- 0: No Movement
- 1: Movement is detected on CH0

› Bit 4: **Settled**
- 0: Movement UI is not in a settled state
- 1: Movement UI is in a settled state

› Bit 3: **CH3 Filter-Halt**
- 0: CH3 Filter-Halt is not active
- 1: CH3 Filter-Halt is active

› Bit 2: **CH2 Filter-Halt**
- 0: CH2 Filter-Halt is not active
- 1: CH2 Filter-Halt is active

› Bit 1: **CH1 Filter-Halt**
- 0: CH1 Filter-Halt is not active
- 1: CH1 Filter-Halt is active

› Bit 0: **CH0 Filter-Halt**
- 0: CH0 Filter-Halt is not active
- 1: CH0 Filter-Halt is active

Table A.4: Channel Follow Settings

Register: 0x30, 0x31, 0x32, 0x33

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved			Enable LTA scale	Follow ATI Counts				Follow ATI Parameters				Follow ATI Events			

› Bit 12: **Enable LTA scaling**
- 0: No LTA based scaling will be applied
- 1: LTA adjustment due to counts following will be adjusted based on the reference/follow LTA ratio.

› Bits 8-11: **Follow Channel Counts**[i]
- 1000: CH3 will follow channel counts
- 0100: CH2 will follow channel counts
- 0010: CH1 will follow channel counts
- 0001: CH0 will follow channel counts

› Bits 4-7: **Follow ATI Parameters**[i]
- 1000: CH3 will follow channel ATI parameters
- 0100: CH2 will follow channel ATI parameters
- 0010: CH1 will follow channel ATI parameters

- 0001: CH0 will follow channel ATI parameters

› Bits 0-3: **Follow ATI Events**[i]
- 1000: CH3 will follow channel ATI events
- 0100: CH2 will follow channel ATI events
- 0010: CH1 will follow channel ATI events
- 0001: CH0 will follow channel ATI events

Table A.5: Follow Weight

Register: 0x34,0x35,0x36,0x37

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Follow Weight Integer								Follow Weight Decimal							

› Bit 8-15: **Follow Weight Integer**
- 8-bit Integer follow weight value

› Bit 0-7: **Follow Weight Decimal**
- 8-bit decimal follow weight factor

Table A.6: Compensation Ratio

Register: 0x38,0x39,0x3A,0x3B

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Scale Integer								Compensation Scale Decimal							

› Bit 8-15: **Compensation Scale Integer**
- 8-bit Integer scaling value

› Bit 0-7: **Compensation Scale Decimal**
- 8-bit decimal scaling factor

Table A.7: Self Capacitance Filter Beta Values

Register: 0x40

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Self-Cap LTA LP Beta				Self-Cap LTA NP Beta				Self-Cap Counts LP Beta				Self-Cap Counts NP Beta			

› Bit 12-15: **Self-Capacitance LTA Low Power Beta Filter Value**
- 4-bit value

› Bit 8-11: **Self-Capacitance LTA Normal Power Beta Filter Value**
- 4-bit value

› Bit 4-7: **Self-Capacitance Counts Low Power Beta Filter Value**
- 4-bit value

› Bit 0-3: **Self-Capacitance Counts Normal Power Beta Filter Value**
- 4-bit value

Table A.8: Self-Capacitance Filter Betas continues

Register: 0x41

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Self-Cap Filter Band								Self-Cap LTA LP Fast Beta				Self-Cap LTA NP Fast Beta			

› Bit 8-15: **Self-Capacitance Filter band**
- 8-bit value, which determines the inverse delta required for a fast LTA beta.

› Bit 4-7: **Self-Capacitance LTA Low Power Fast Beta Filter Value**
- 4-bit value

› Bit 0-3: **Self-Capacitance LTA Normal Power Fast Beta Filter Value**
- 4-bit value

[i] Note that a channel cannot follow itself. For example, writing ’0001’ for bits 8-11 (CH0 will follow counts) to register 0x30 (register for CH0 follow settings) is invalid and may lead to a malfunction.

Table A.9: Mutual Capacitance Filter Beta Values

Register:		0x42													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mutual Cap LTA LP Beta				Mutual Cap LTA NP Beta				Mutual Cap Counts LP Beta				Mutual Cap Counts NP Beta			

- Bit 12-15: **Mutual Capacitance LTA Low Power Beta Filter Value**
  - 4-bit value
- Bit 8-11: **Mutual Capacitance LTA Normal Power Beta Filter Value**
  - 4-bit value
- Bit 4-7: **Mutual Capacitance Counts Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Mutual Capacitance Counts Normal Power Beta Filter Value**
  - 4-bit value

Table A.10: Mutual Capacitance Filter Betas continues

Register:		0x43													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mutual Cap Filter Band								Mutual Cap LTA LP Fast Beta				Mutual Cap LTA NP Fast Beta			

- Bit 8-15: **Mutual Capacitance Filter band**
  - 8-bit value, which determines the inverse delta required for a fast LTA beta.
- Bit 4-7: **Mutual Capacitance LTA Low Power Fast Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Mutual Capacitance LTA Normal Power Fast Beta Filter Value**
  - 4-bit value

Table A.11: Hardware Measurement Settings

Register:		0x44, 0x45													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bias	Inactive Pad Sel		Fine Divider Preload					Reserved			Coarse Divider Preload				

- Bit 15: **Cx8 Bias enable**
  - 0: 0.5V Bias is disabled on Cx8
  - 1: 0.5V Bias is enabled on Cx8
- Bit 13-14: **Inactive Pad Select**
  - 00: Inactive pads are left as Floating
  - 01: Inactive pads are connected to Cx8/Floating
  - 10: Inactive pads are driven to VSS
  - 11: Inactive pads are driven to VREGA
- Bit 8-12: **Fine Divider Preload**
  - 0 - 31: Fine Divider Preload Value
- Bit 0-4: **Coarse Divider Preload**
  - 0 - 31: Coarse Divider Preload Value

Table A.12: Fine and Coarse Multipliers

Register:		0x60,0x62,0x64,0x66													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.13: ATI Compensation

Register: 0x61,0x63,0x65,0x67

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.14: General Wear UI settings

Register: 0x70

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI upon Release	Temp Tracking	Out-of-Wear ATI Mode			In-Wear ATI Mode			Crosscheck Band		Reseed upon Release	Dynamic ATI Target	LTA Adjustment Fixed	Adjust ATI mode	Use Movement as Filter Halt	Enable Wear UI

- Bit 15: **ATI upon Release**
  - 0: Do not ATI when wear is released
  - 1: Execute ATI routine when wear is released
- Bit 14: **Temperature Tracking**
  - 0: No Ch0/Ch1 tracking is enabled
  - 1: CH0's LTA will be adjusted based on counts shift on CH1, when movement is present on CH0.
- Bit 11-13: **Out-of-Wear ATI mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI
- Bit 8-10: **In-Wear ATI mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI
- Bit 6-7: **In Wear ATI Crosscheck Band**
  - 00: 50% Band
  - 01: 25% Band
  - 10: 12.5% Band
  - 11: 6.25% Band
- Bit 5: **Reseed upon release**
  - 0: Do not reseed when wear is released
  - 1: Reseed when wear is released
- Bit 4: **Dynamic Target**
  - 0: Ch0 will re-ATI to its original ATI target when an ATI routine occurs In-Wear
  - 1: Ch0 will re-ATI to a new ATI target based on its base value
- Bit 3: **LTA Adjustment Fixed**
  - 0: When an in Wear ATI occurred, CH0's LTA is set to the new post ATI counts plus the pre-ATI counts delta.
  - 1: When an in Wear ATI occurred, CH0's LTA is set to the new post ATI counts multiplied with the Pre-ATI LTA, divide by Pre-ATI Counts ratio
- Bit 2: **Dynamic ATI modes**
  - 0: No ATI mode switching will occur
  - 1: The ATI mode will be set based on the wear-state.
- Bit 1: **Use Movement as Filter Halt**
  - 0: CH0's LTA will be halted based on the proximity event level
  - 1: CH0's LTA will be halted based if movement is present on the channel or not.
- Bit 0: **Enable Wear UI**
  - 0: Wear UI is enabled
  - 1: Wear UI is disabled

Table A.15: Wear UI beta values

Register:				0x73											
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				LP Gradient Beta value				NP Gradient Beta value				In-Wear LTA Beta Value			

- Bit 8-11: **Low Power Gradient Beta value**
  - 4-bit value
- Bit 4-7: **Normal Power Gradient Beta value**
  - 4-bit value
- Bit 0-3: **In-Wear LTA Beta Value**
  - 4-bit value

Table A.16: Temperature tracking ratio

Register:				0x76											
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Temperature Scaling Ratio Integer								Temperature Scaling Ratio Decimal							Track sign

- Bit 8-15: **Temperature Scaling Ratio Integer**
  - 8-bit Integer Temperature scaling ratio value
- Bit 1-7: **Temperature Scaling Ratio Decimal**
  - 7-bit decimal Temperature scaling ratio factor
- Bit 0: **Temperature Tracking Sign**
  - 0: CH0's LTA will be adjusted in the same direction as CH1's counts
  - 1: CH0's LTA will be adjusted in the opposite direction as CH1's counts

Table A.17: Channel 0's Activation threshold (Wear Threshold)

Register:				0x78											
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH0's Activation Threshold (Wear Threshold)															

- Bit 0-15: **CH0's Activation Threshold**
  - $\frac{LTA}{65535} * 16\ bit\ value$

Table A.18: System Settings

Register:				0x80											
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NP Wake settings			WDT enabled	AutoProx cycles		Power mode		Event Mode	Standalone Output	Stop end comms disable	RW Check disable	Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 13-15: **NP Wake settings**
  - 001: Switch to NP mode upon movement on CH0
  - 010: Switch to NP mode upon an event on of the channels (Channel events are maskable)
  - 100: Stay in NP mode when an event is active on any of the channels (Channel states are maskable)
- Bit 12: **WDT enabled**
  - 0: Watchdog timer is disabled
  - 1: Watchdog timer is enabled
- Bit 10-11: **Number of AutoProx cycles**
  - 00: 4 cycles
  - 01: 8 cycles
  - 10: 16 cycles
  - 11: 32 cycles
- Bit 8-9: **Power Mode Selection**
  - 00: Normal power
  - 01: Low power
  - 10: Halt Mode
  - 11: Automatic power mode switching
- Bit 7: **Event Mode**

- 0: Streaming Mode
- 1: Event Mode (comms windows will only be opened upon Force Comms requests or if an non-masked event occured)

- Bit 6: **Standalone Output**
  - 0: Standalone Output is disabled
  - 1: Wear State will be presented on OUT(Push-Pull, Active Low)
- Bit 5: **Stop end comms disable**
  - 0: Sending a stop-bit will close the I2C comms window
  - 1: Sending a stop-bit will not close the I2C comms window, comms window will close with ready-timeout
- Bit 4: **RW Check disable**
  - 0: Write protection is enabled
  - 1: Write protection is disabled
- Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
- Bit 2: **Execute ATI Command**
  - 0: Do not ATI
  - 1: ATI
- Bit 1: **Soft Reset**
  - 0: Do not reset device
  - 1: Reset device after communication window terminates
- Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

Table A.19: Watchdog Timeout and Event Mode mask

Register: 0x81

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Event Mode mask								WDT timeout							

- Bit 15: **In Wear ATI failure Event mask**
  - 0: In Wear ATI failure event enabled
  - 1: In Wear ATI failure event masked
- Bit 14: **Wear Event mask**
  - 0: Wear event enabled
  - 1: Wear event masked
- Bit 12: **Wear release Event mask**
  - 0: Wear release event enabled
  - 1: Wear release event masked
- Bit 11: **Activation Event Mask**
  - 0: Activation event enabled
  - 1: Activation event masked
- Bit 10: **Filter Halt Event Mask**
  - 0: Filter Halt event enabled
  - 1: Filter Halt event masked
- Bit 9: **Power Mode Event Mask**
  - 0: Power Mode event enabled
  - 1: Power Mode event masked
- Bit 8: **ATI Event Mask**
  - 0: ATI event enabled
  - 1: ATI event masked
- Bit 0-7: **Watchdog timeout**
  - 8-bit value (ms)

Table A.20: Switch to Normal Power Mode mask

Register: 0x82

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				CH3 Activation	CH2 Activation	CH1 Activation	CH0 Activation	Reserved				CH3 Filter Halt	CH2 Filter Halt	CH1 Filter Halt	CH0 Filter Halt

- Bit 11: **CH3 Activation normal power switch mask**
  - 0: CH3 Activation can cause a power mode jump to normal power
  - 1: CH3 Activation is masked
- Bit 10: **CH2 Activation normal power switch mask**
  - 0: CH2 Activation can cause a power mode jump to normal power
  - 1: CH2 Activation is masked
- Bit 9: **CH1 Activation normal power switch mask**
  - 0: CH1 Activation can cause a power mode jump to normal power
  - 1: CH1 Activation is masked
- Bit 8: **CH0 Activation normal power switch mask**
  - 0: CH0 Activation can cause a power mode jump to normal power
  - 1: CH0 Activation is masked
- Bit 3: **CH3 Filter Halt normal power switch mask**
  - 0: CH3 Filter Halt can cause a power mode jump to normal power
  - 1: CH3 Filter Halt is masked
- Bit 2: **CH2 Filter Halt normal power switch mask**
  - 0: CH2 Filter Halt can cause a power mode jump to normal power
  - 1: CH2 Filter Halt is masked
- Bit 1: **CH1 Filter Halt normal power switch mask**
  - 0: CH1 Filter Halt can cause a power mode jump to normal power
  - 1: CH1 Filter Halt is masked
- Bit 0: **CH0 Filter Halt normal power switch mask**
  - 0: CH0 Filter Halt can cause a power mode jump to normal power
  - 1: CH0 Filter Halt is masked

Table A.21: Channel Filter-halt Debounce

Register: 0xA3, 0xB3, 0xC3, 0xD3

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Debounce Exit				Debounce Enter				Reserved							

- Bit 12-15: **Exit Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 8-11: **Enter Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value

Table A.22: Activation threshold

Register: 0xA4, 0xB4, 0xC4, 0xD4

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH's Activation Threshold															

- Bit 0-15: **CH's Activation Threshold**
  - $\frac{LTA}{65535} * 16\ bit\ value$

Table A.23: Activation Hysteresis

Register: 0xA5, 0xB5, 0xC5, 0xD5

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								CH's Activation Hysteresis							

- Bit 0-7: **Activation Hysteresis**
  - Activation hysteresis value determines the release threshold. Release threshold can be determined as follows:
  - $\frac{LTA * Threshold\ bit\ value}{2^8} - \frac{Threshold\ bit\ value * Hysteresis\ bit\ value * LTA}{2^{16}}$

Table A.24: General sensor settings

Register: 0xA6, 0xB6, 0xC6, 0xD6

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI-Band								ATI-Mode			Zero-Comp	Linear-ize	Inverse	Dual	CalCap effect

- Bit 8-15: **ATI Band**
  - Size of the Re-ATI band: $ATI\ Target * \frac{8\ bit\ value}{255}$
- Bit 5-7: **ATI mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI
- Bit 4: **Zero Compensation**
  - 0: Compensation is added to the channel
  - 1: No Compensation is added to the channel
- Bit 3: **Linearize**
  - 0: Channel's filtered counts is not linearized
  - 1: Channel's filtered counts is linearized.
- Bit 2: **Inverse**
  - 0: Filter-halt and Activation Events are detected when Counts<LTA
  - 1: Filter-halt and Activation Events are detected when Counts>LTA
- Bit 1: **Dual Direction Threshold**
  - 0: Filter-halt and Activation Events are only detected in a single direction
  - 1: Filter-halt and Activation Events are detected in both delta directions
- Bit 0: **Calibration Capacitor effect**
  - 0: Calibration Capacitor adds charge to the sensor
  - 1: Calibration Capacitor removes charge from the sensor

Table A.25: Sensor measurement settings

Register: 0xA7, 0xB7, 0xC7, 0xD7

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH En	CS 0V5 Dis-charge	RF filter	Cs size	Proj Bias		Max Counts		Reserved		1	CalCap size			Sensing mode	

- Bit 15: **Channel enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 14: **CS 0V5 Discharge enabled**
  - 0: CS 0V5 Discharge disabled
  - 1: CS 0V5 Discharge enabled
- Bit 13: **RF Filter Enable**
  - 0: RF Filter disabled
  - 1: RF Filter enabled
- Bit 12: **Cs 80pF**
  - 0: 40pF
  - 1: 80pF
- Bit 10-11: **Mutual Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA
- Bit 8-9: **Maximum counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384
- Bit 2-4: **Calibration cap size selection**

- 001: 0.5pF
- 010: 1pF
- 011: 1.5pF
- 100: 2pF
- 101: 2.5pF
- 110: 3pF
- 111: 3.5pF

› Bit 0-1: **Sensing mode selection**
- 00: Self-capacitance mode
- 01: Mutual-capacitance mode[i]
- 10: Temperature sensing mode

Table A.26: Charge transfer settings

Register: 0xA8, 0xB8, 0xC8, 0xD8

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

› Bit 8-15: **Conversion Period**
- Range: 0 - 127

› Bit 0-7: **Frequency Fraction**
- $256 * \frac{f_{conv}}{f_{clk}}$
- Range: 0 - 127
- Set to 127

› Note: With the frequency fraction set to 127, the following values of the conversion period will result in the corresponding charge transfer frequencies:
- 1: 2.3MHz
- 5: 1MHz[ii]
- 12: 500kHz
- 17: 350kHz
- 26: 250kHz
- 53: 125kHz

Table A.27: Channel Input selection

Register: 0xAB, 0xBB, 0xCB, 0xDB

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved									Temp	Offset current	CalCap	Rx3	Rx2	Rx1	Rx0

› Bit 6: **Temperature**
- 0: Temperature sensor is not selected as input
- 1: Temperature sensor is selected as input

› Bit 5: **Offset current**
- 0: Offset current is not selected as input
- 1: Offset current is selected as input

› Bit 4: **Calibration Capacitor**
- 0: Calibration Capacitor is not selected as input
- 1: Calibration Capacitor is selected as input

› Bit 3: **CRx3**
- 0: CRx3 is not selected as input
- 1: CRx3 is selected as input

› Bit 2: **CRx2**
- 0: CRx2 is not selected as input
- 1: CRx2 is selected as input

› Bit 1: **CRrx1**
- 0: CRx1 is not selected as input
- 1: CRx1 is selected as input

› Bit 0: **CRx0**
- 0: CRx0 is not selected as input

[i] Ensure that at least one Cx pin is selected as an Rx before switching to Mutual-capacitance mode
[ii] Please note: The maximum charge transfer frequency for Mutual capacitance mode is 1MHz

- 1: CRx0 is selected as input

Table A.28: Channel Offset current selection

Register: 0xAC, 0xBC, 0xCC, 0xDC

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Offset				Trim			

- Bits 4-7: **Offset**
  - Offset current, Sign and magnitude for power level i.e. -7 .. 7 in 3uA steps.
- Bits 0-3: **Trim**
  - Increase the DC output current in 200nA steps

Table A.29: Channel Tx Selection

Register: 0xAD, 0xBD, 0xCD, 0xDD

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				CTx11	CTx10	Res	CTx8	CTx7	CTx6	CTx5	CTx4	CTx3	CTx2	CTx1	CTx0

- Bit 11: **CTx11**
  - 0: CTx11 disabled as Tx
  - 1: CTx11 enabled as Tx
- Bit 10: **CTx10**
  - 0: CTx10 disabled as Tx
  - 1: CTx10 enabled as Tx
- Bit 8: **CTx8**
  - 0: CTx8 disabled as Tx
  - 1: CTx8 enabled as Tx
- Bit 7: **CTx7**
  - 0: CTx7 disabled as Tx
  - 1: CTx7 enabled as Tx
- Bit 6: **CTx6**
  - 0: CTx6 disabled as Tx
  - 1: CTx6 enabled as Tx
- Bit 5: **CTx5**
  - 0: CTx5 disabled as Tx
  - 1: CTx5 enabled as Tx
- Bit 4: **CTx4**
  - 0: CTx4 disabled as Tx
  - 1: CTx4 enabled as Tx
- Bit 3: **CTx3**
  - 0: CTx3 disabled as Tx
  - 1: CTx3 enabled as Tx
- Bit 2: **CTx2**
  - 0: CTx2 disabled as Tx
  - 1: CTx2 enabled as Tx
- Bit 1: **CTx1**
  - 0: CTx1 disabled as Tx
  - 1: CTx1 enabled as Tx
- Bit 0: **CTx0**
  - 0: CTx0 disabled as Tx
  - 1: CTx0 enabled as Tx

Table A.30: Channel CM Tx Selection

Register: 0xAE, 0xBE, 0xCE, 0xDE

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				CTx11	CTx10	Res	CTx8	CTx7	CTx6	CTx5	CTx4	CTx3	CTx2	CTx1	CTx0

- Bit 11: **CTx11**
  - 0: CTx11 disabled as CM Tx
  - 1: CTx11 enabled as CM Tx
- Bit 10: **CTx10**
  - 0: CTx10 disabled as CM Tx

- 1: CTx10 enabled as CM Tx

- Bit 8: **CTx8**
  - 0: CTx8 disabled as CM Tx
  - 1: CTx8 enabled as CM Tx
- Bit 7: **CTx7**
  - 0: CTx7 disabled as CM Tx
  - 1: CTx7 enabled as CM Tx
- Bit 6: **CTx6**
  - 0: CTx6 disabled as CM Tx
  - 1: CTx6 enabled as CM Tx
- Bit 5: **CTx5**
  - 0: CTx5 disabled as CM Tx
  - 1: CTx5 enabled as CM Tx
- Bit 4: **CTx4**
  - 0: CTx4 disabled as CM Tx
  - 1: CTx4 enabled as CM Tx
- Bit 3: **CTx3**
  - 0: CTx3 disabled as CM Tx
  - 1: CTx3 enabled as CM Tx
- Bit 2: **CTx2**
  - 0: CTx2 disabled as CM Tx
  - 1: CTx2 enabled as CM Tx
- Bit 1: **CTx1**
  - 0: CTx1 disabled as CM Tx
  - 1: CTx1 enabled as CM Tx
- Bit 0: **CTx0**
  - 0: CTx0 disabled as CM Tx
  - 1: CTx0 enabled as CM Tx

B Revision History

Release	Date	Changes
v1.0	August 2022	Initial Release
v1.1	September 2022	Updated QFN dimensions
v1.2	September 2022	Matched Order Code to Package Top Marking
v1.3	August 2023	Updated Formatting Revision History Added Updated Pin Descriptions Updated Block Diagram Updated Reference Schematic Force Communication Section Updated Added reference to "PIN-230172" Corrections in Memory Map Descriptions
v1.4	November 2023	Updated I^2C Timeout Recommendation
v1.5	March 2025	Updated order codes section

Contact Information

	South Africa (Headquarters)	China
Physical Address	1 Bergsig Avenue Paarl 7646 South Africa	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC
Tel	+27 21 863 0033	+86 755 8303 5294 ext 808
Email	info@azoteq.com	info@azoteq.com

	USA	Taiwan
Physical Address	7000 North Mopac Expressway Suite 200 Austin TX 78731 USA	Xintai 5th Road, Sec. 1 No. 99, 9F-12C Xizhi District 221001 New Taipei City Taiwan
Tel	+1 512 538 1995	+886 932 219 444
Email	info@azoteq.com	info@azoteq.com

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