IQS7222A DATASHEET

12 Channel Mutual-/Self-capacitive, Inductive force and Hall sensing controller with I²C communications interface and low power options

1 Device Overview

The IQS7222A ProxFusion® IC is a sensor fusion device for applications that require multiple sensing capabilities from a single sensor IC. The sensor is fully I²C compatible, and on-chip calculations enable multiple application options. Various UIs, from gestures to power mode switching, allow the IC to respond effectively in the intended application with ultra-low power consumption.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) / 8 (WLCSP)external sensor pad connections
- Self-/Mutual capacitive sensors configuration for display wake-up
- ULP wake-up on touch
  - Dedicated ultra-low-power wake-up touch sensor
- Configure up to 12[i] Channels using the external connections or internal sensor
- External sensor options:
  - Up to 8 self-capacitive buttons
  - Up to 4 self-capacitive wear detection pairs (with physical reference)
  - Up to 10 mutual capacitive touch/proximity sensors
  - Up to 4 inductive sensor elements (metal detection/force sensing)
- Internal sensor options:
  - Hall Switch
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Active environment tracking with reference sensor
  - Debounce and Hysteresis
  - Dual direction trigger indication
- Built-in Signal processing options:
  - Slider output
  - Up to 4 elements per slider
  - Up to 2 sliders simultaneously
  - Slider gesture outputs
- Design simplicity
  - PC software for debugging and obtaining optimal settings and performance
  - One-time programmable settings for custom power-on IC configuration
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I²C communication interface with IRQ/RDY(up to fast plus -1 MHz)
- Event and streaming modes
- Configurable dedicated output pin
- Supply Voltage 1.71 V to 3.6 V
- Package options
  - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4 mm x 0.6 mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4 mm pitch

QFN20 Package

WLCSP18 Package

[i] WLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured are less than QFN20 package

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1.2 Applications

- SAR Compliance in Mobile devices
- Low power Wake-up Buttons / Proximity
- Appliance user interface (Slider & Buttons)
- TWS earphones (touch, slider, wear, force and dock detection)
- Waterproof Buttons (Inductive)
- Wear Detection
- HALL-effect Dock Detection

1.3 Block Diagram

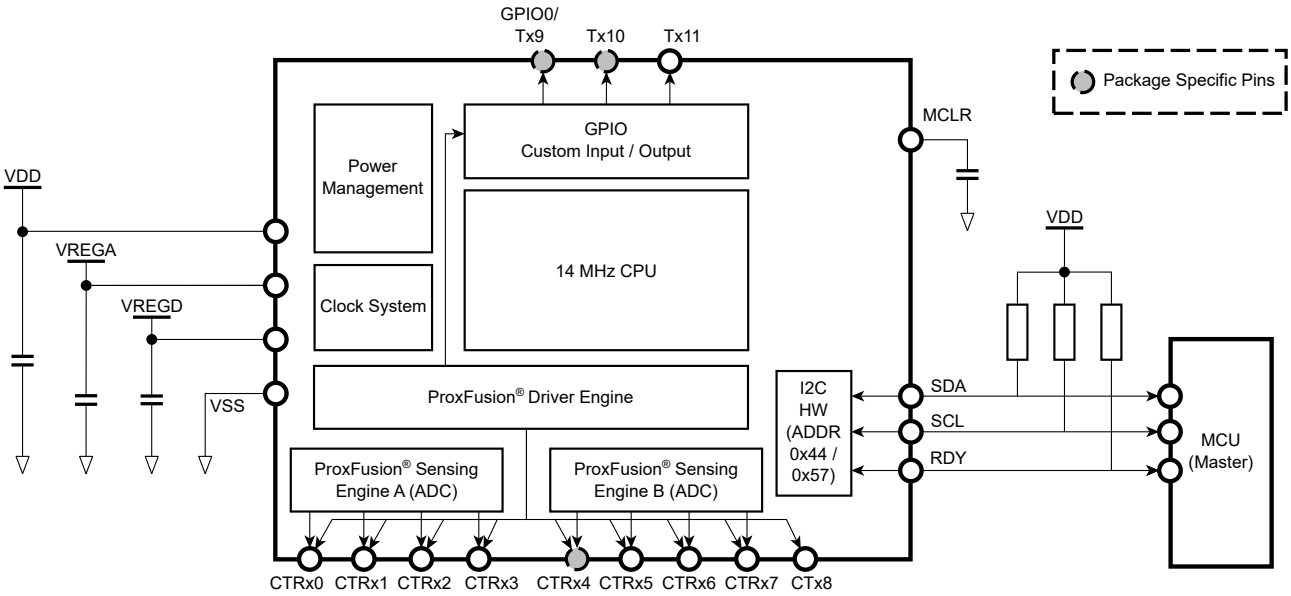

Figure 1.3: Functional Block Diagram[ii]

[ii] WLCSP18 packages do not have a CRX4 and combines GPIO0/Tx9 and Tx10

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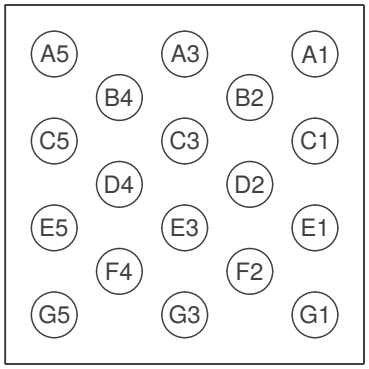
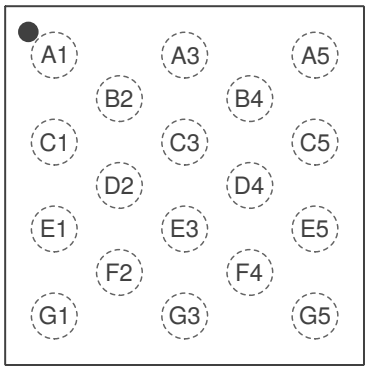
2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

Table 2.1: 18-pin WLCSP18 Package

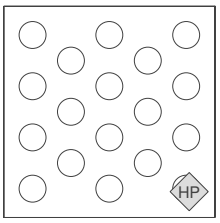


Ball-side View

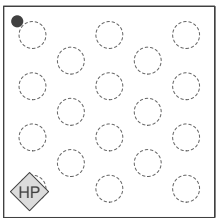


Top-side View

Pin no.	Signal
A1	CTx9/GPIO0/CTx10[i]
A3	SCL
A5	MCLR
B2	CTx11
B4	SDA
C1	CTx8
C3	RDY
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CRx6/CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CRx5/CTx5
F4	CRx0/CTx0
G1	CRx7/CTx7
G3	CRx3/CTx3
G5	VREGA



Ball-side View

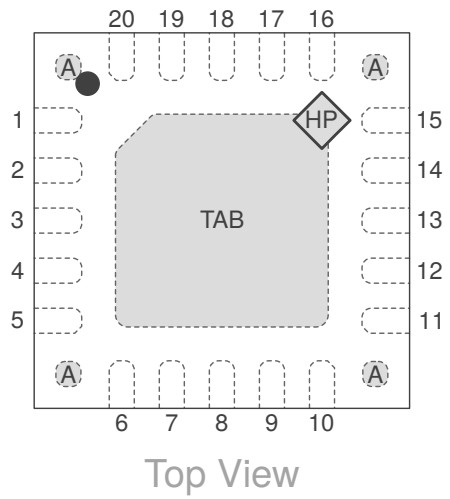


Top-side View

Area Name	Signal Name
HP	Hall Plate

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8
4	VREGA	14	CTx9/GPIO0
5	CRx0/CTx0	15	CTx10
6	CRx1/CTx1	16	CTx11
7	CRx2/CTx2	17	RDY
8	CRx3/CTx3	18	SCL
9	CRx4/CTx4	19	SDA
10	CRx5/CTx5	20	MCLR

Area name	Signal name
TAB[ii]	Thermal pad (floating)
A[iii]	Thermal pad (floating)
HP	Hall Plate

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
A1	14	CTx9/GPIO0	Prox/Digital		VREGA/VDD
B4	19	SDA	Digital		VDD
A3	18	SCL	Digital		VDD
A1	15	CTx10	Prox		VREGA
B2	16	CTx11	Prox		VREGA
C3	17	RDY	Digital		VDD
A5	20	MCLR	Digital		VDD

[i] Please note that CTx9/GPIO0 and CTx10 are connected together in the WLCSP18 package.
[ii] It is recommended to connect the thermal pad (TAB) to VSS.
[iii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

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2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iv]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CRx4/CTx4	-	9	IO	
	CRx5/CTx5	F2	10	IO	
	CRx6/CTx6	E1	11	IO	
	CRx7/CTx7	G1	12	IO	
	CTx8	C1	13	O	CTx8 pad
	CTx9/GPIO0	A1	14	O	Configurable digital output
	CTx10	A1	15	O	CTx10 pad
	CTx11	B2	16	O	CTx11 pad
GPIO	RDY	C3	17	O	RDY pad
	MCLR	A5	20	I	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA	B4	19	IO	I^2C data
	SCL	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[iv] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

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2.5 Reference Schematic

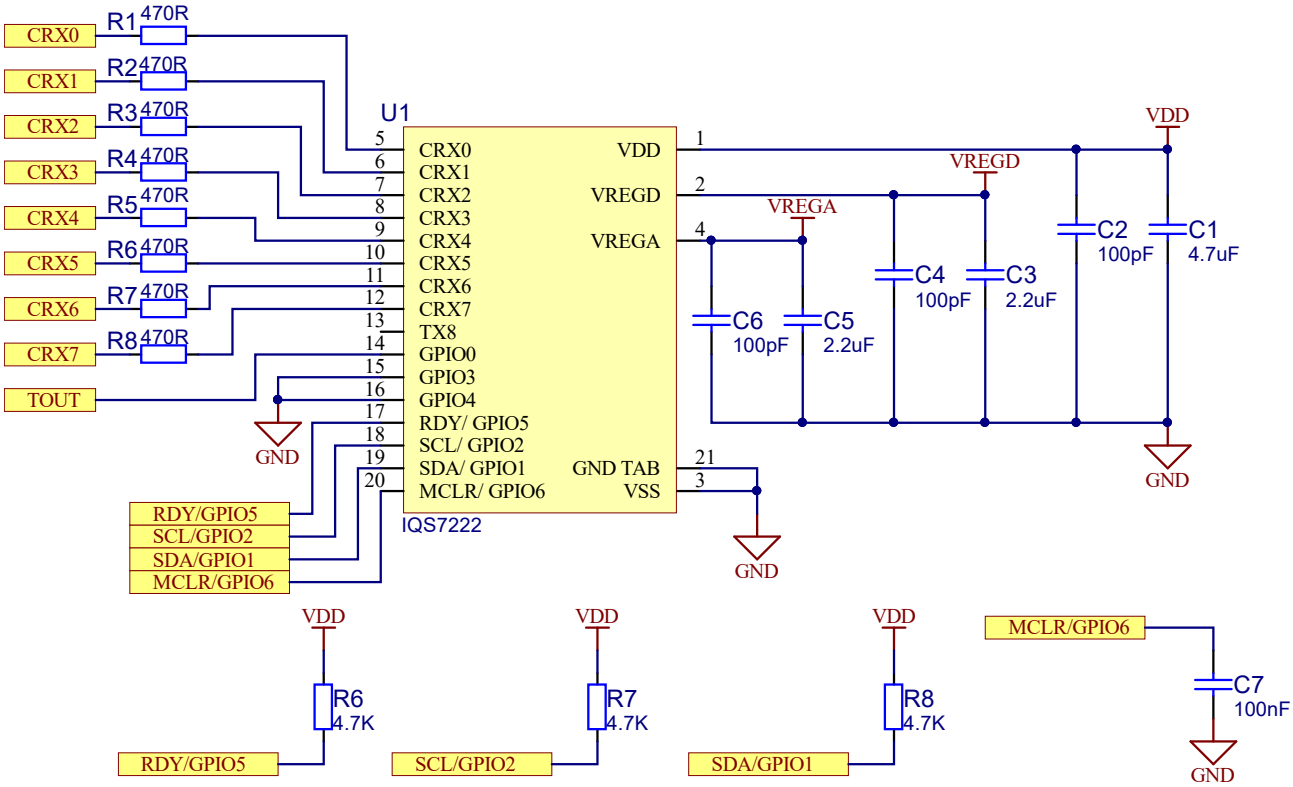

Figure 2.1: 8 Button Self Capacitance Reference Schematic

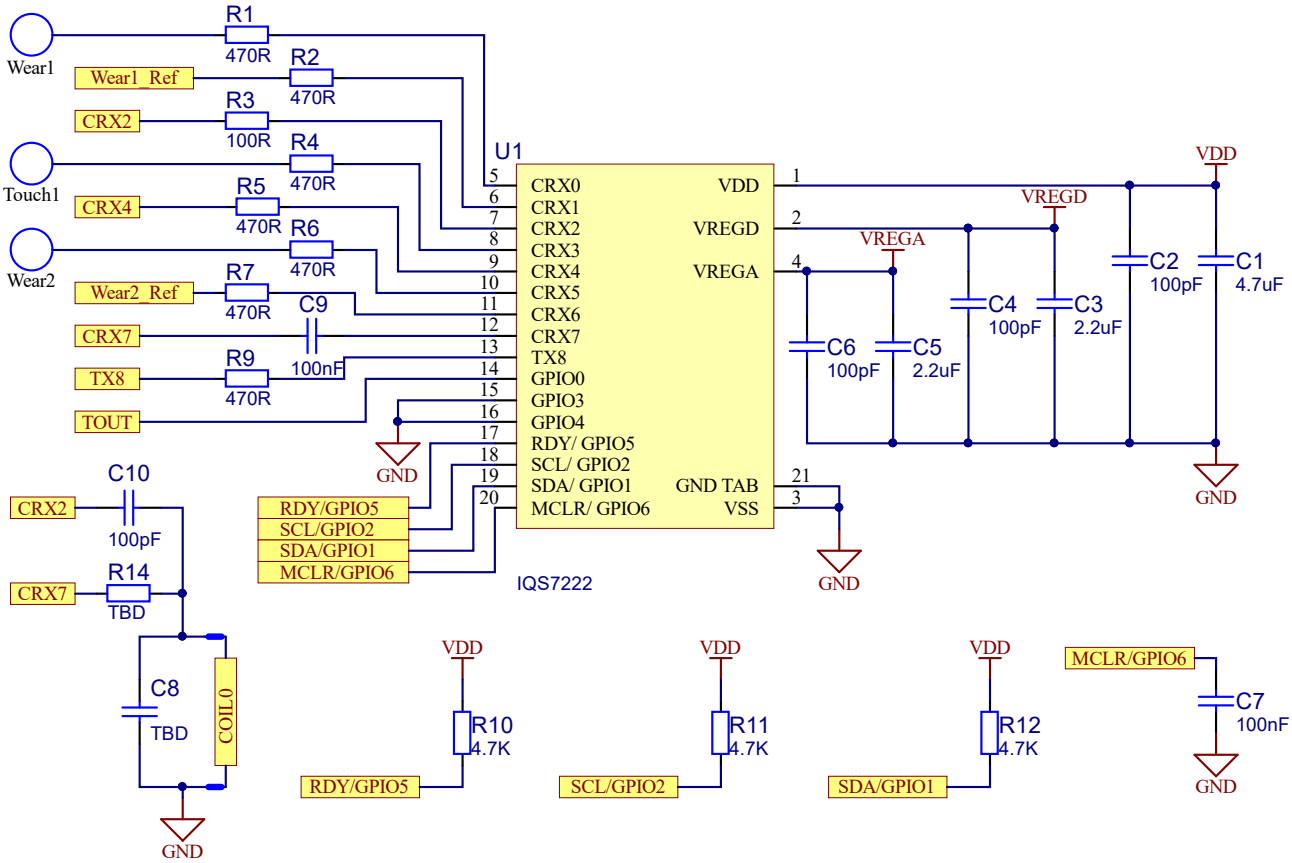

Figure 2.2: Wear, Reference and Inductive Sensing Reference Schematic

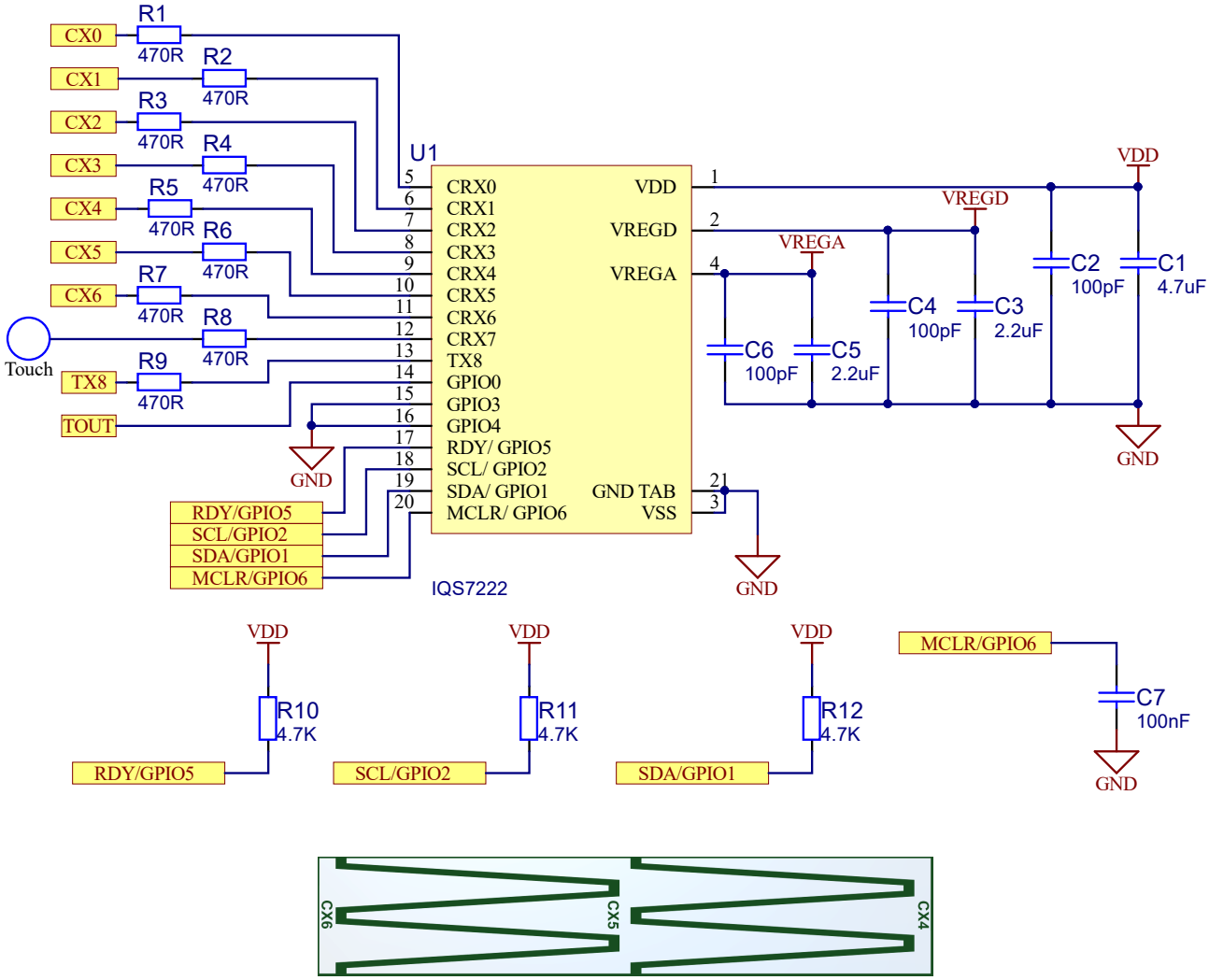

Figure 2.3: 3 Channel Slider with Touch Sensor Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	−0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	−0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	−40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz	1.71		3.6	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	−40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREGA}$	$3\times C_{VREGA}$		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF-VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{CTx-CRx}$	Capacitance between receiving and transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{CRx-VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, F_{xfer} = 1 MHz Mutual-capacitance mode, F_{xfer} = 4 MHz			100[ii] 25[ii]	pF
$\frac{Cp_{CRx-VSS}}{Cm_{CTx-CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.
[ii] RCx = 0 Ω.

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3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

3.4 Hall Effect Sensing Characteristics

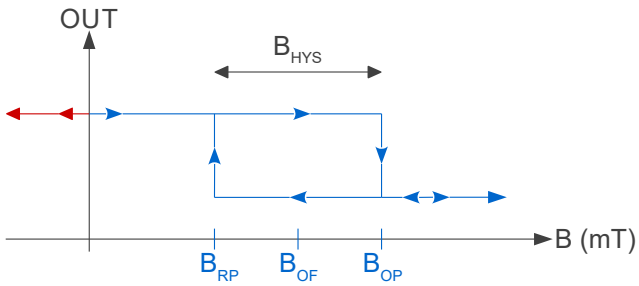

Figure 3.1: Magnet Trigger Level Description (Active Low Output)

Table 3.4: Example Power-on Magnet Detection Options

Hall Sensor Setup	Output Type	B_{RP} (mT)	B_{OP} (mT)	B_{HYS} (mT)	B_{RP} and B_{OP} Accuracy (mT)
					−10 °C to 80 °C
Threshold example 1	Direct	2.1	3	0.9	27%
Adjustable Threshold	I^2C/Direct	0 – 100% of B_{OP} (default 95%)	Software register	0 – 100% of B_{OP} (default 5%)	TBD

iii Please note that the maximum values for Cp and Cm are subject to this ratio.

iv Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

v Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times F_{xfer})}$ where C is the pin capacitance to VSS.

vi JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

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3.5 Current Consumption

Table 3.5: Typical Current Consumption for Order Code 001

Power mode	Active channels	Report rate	Current [µA]	
		(Sampling rate) [ms]	3.3V	1.8V
NP	Defaults (10 channels self-capacitance & Hall)	16	450	445
	TWS: Wear, slider, inductive resonant without bias, Hall	16	484	480
LP	Defaults (10 channels self-capacitance & Hall)	60	126	124
	TWS: Wear, slider, inductive resonant without bias, Hall	60	126	125
ULP	Distributed (2 self-capacitance auto-prox channels), default setup	150	6.7	6.1
	Distributed (2 self-capacitance auto-prox channels), TWS setup	150	5.8	5.5

Table 3.6: Typical Current Consumption for Order Code 102

Power mode	Active channels	Report rate	Current [µA]	
		(Sampling rate) [ms]	3.3V	1.8V
NP	Defaults (10 channels self-capacitance & Hall)	16	426	421
LP	Defaults (10 channels self-capacitance & Hall)	60	110	107
ULP	Distributed (2 self-capacitance auto-prox channels), default setup	150	9.8	9.6

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4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

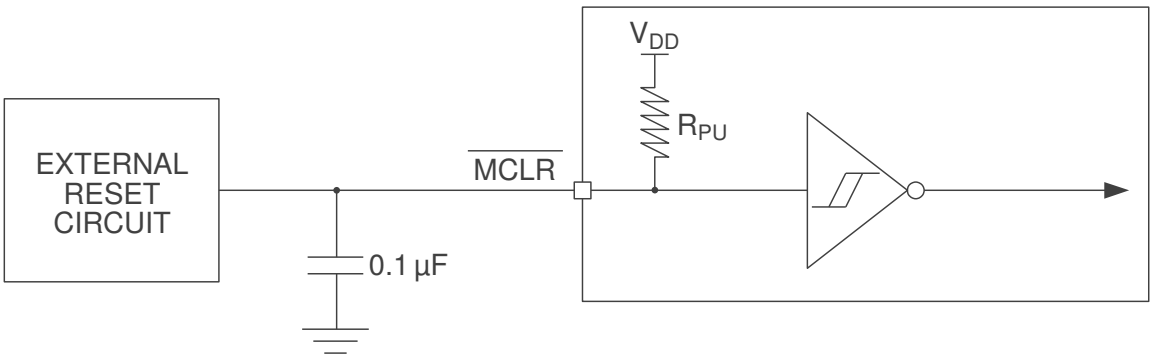

Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
F_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
F_{xfer}	Charge transfer frequency (derived from F_{OSC})	42	500 – 1500	3500	kHz

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4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA		0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA		0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2		V
V_{IL}	Input low voltage			VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7		V
C_{b_max}	SDA & SCL maximum bus capacitance			550	pF

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

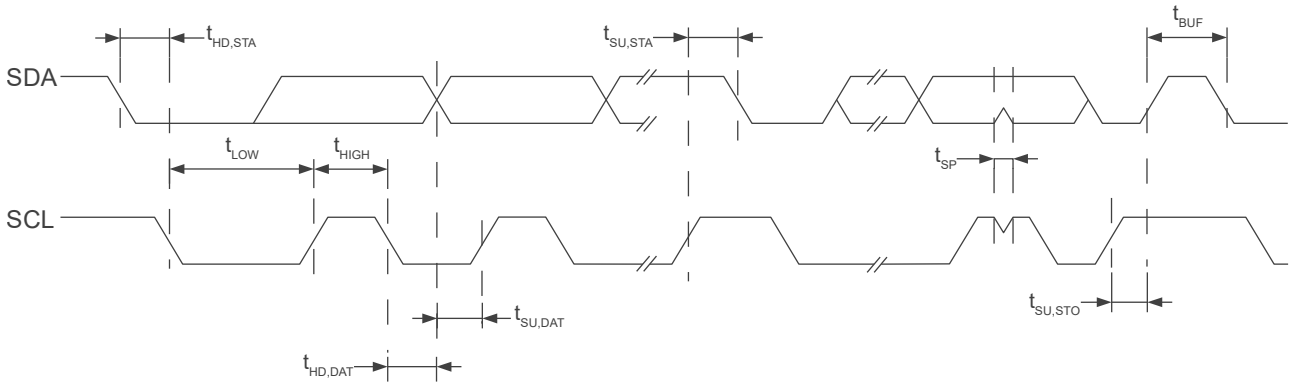

Figure 4.2: I²C Mode Timing Diagram

[i] Refers to CTx9/GPIO0, CTx10, CTx11, and RDY pins.

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5 ProxFusion® Module

The IQS7222A contains dual ProxFusion® modules which use patented technology to measure and process the sensor data. Two modules ensure a rapid response from multi-channel implementations. The multiple touch, proximity and weighted average (slider) outputs are the primary output from the sensor.

5.1 Channel Options

Self-capacitance, Mutual capacitance, Reference tracking, Inductive designs and Hall effect sensing are possible with the IQS7222A.

- Sensor pad design overview: AZD125
- Mutual capacitance button layout guide: AZD125
- Inductive design layout guide: AZD115
- Hall effect Switch UI Sensing: Section 5.1.1

5.1.1 Hall Effect Switch UI

Hall effect sensing is an internal sensing option that requires no external sensor design.

The Hall effect switch UI measures the magnetic field induced on the hall plate of the IC and is, by default, activated when both Hall-effect channels (channel 10 and channel 11) are active. The UI uses two channels to determine the magnetic field induced on the Hall plate. Using two channels ensures that the ATI (refer to Section 5.4) can still be used in the presence of the magnet. An inverted channel allows the capability of calculating a reference value which will always be the same regardless of the presence of a magnet. Enabling the UI will enable the IC to display the effects of the magnet by reading the data in the Hall UI flags and output registers.

The Hall effect switch UI is used for detection of the presence of a single magnet.

There are two channel outputs, and each channel controls different parameters of the Hall effect. Please note that parameters not listed under the relevant channel's setting, below, must be left as default.

Channel 10 output is the signal output, calculated using:

$$\text{Channel 10}_{\text{output}} = \frac{\text{Counts} - \text{Counts}_{\text{inv}}}{2}$$

Settings from Channel 10 used for Hall effect switch UI:

- Touch Threshold
- Prox Threshold
- Touch Hysteresis
- Enter debounce
- Exit debounce

Channel 11 output is the LTA and signal without the output on Channel10, calculated using:

$$\text{Channel 11}_{\text{output}} = \frac{\text{Counts} + \text{Counts}_{\text{inv}}}{2}$$

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Channel 11 allows ATI to be performed without changing the count value on Channel 10.

Settings from Channel 11 used for Hall effect switch UI:

- ATI Mode
- ATI Band
- ATI Compensation
- ATI Compensation Divider
- ATI Coarse Fractional Divider
- ATI Coarse Fractional Multiplier
- ATI Fine Fractional Divider

Settings that should be the same on channel 10 and channel 11 are:

- Frequency fraction
- Frequency period
- Ground inactive Rx's
- Vref 0v5 Enable
- Cs cap size
- ATI Base
- ATI Target

5.2 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance/inductance, and all outputs are derived from this.

5.2.1 Max Count

Each channel is limited to having a count value smaller than the configurable limit of *Maximum counts*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value.

5.3 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

5.3.1 Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (Register 0xD0, bit 3).

5.4 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductances, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

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5.5 Automatic Re-ATI

5.5.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7222A, a status bit will be set momentarily to indicate that this has occurred.

5.5.2 Conditions for Re-ATI to Activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.16.

$$\text{Re-ATI Boundary}_{\text{default}} = \text{ATI Target} \pm \frac{1}{8}\text{ATI Band}$$

For example, assume that the ATI target is configured to 800 and that the default boundary value is (1/8) x 800 = 100. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\text{Reference} > 900 \text{ or Reference} < 700$$

The ATI algorithm executes in a short time, so it goes unnoticed by the user.

5.5.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation $\geq$ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should, however not occur under normal circumstances.

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6 Sensing Modes

6.1 Power Mode and Mode Timeout

The IQS7222A offers 3 power modes:

- Normal power mode (NP):
  - Flexible key scan rate.
- Lower power mode (LP):
  - Flexible key scan rate.
  - Typically set to a slower rate than NP.
- Ultra-low power mode (ULP):
  - Optimised firmware setup.
  - Intended for rapid wake-up on a single channel (e.g., distributed proximity event), enabling immediate button response for an approaching user.
  - The wake-up channels are sampled at the ULP report rate. These channels are updated at the rate calculated by ULP-RR $\times$ AUTO Mode Register Value.
  - The other sensors are sampled at the rate specified in the normal power update rate in the ultra-low power register.

To optimise power consumption and performance, power modes are "stepped" by default to move to power-efficient modes when no interaction has been detected for a certain (configurable) time known as the "mode timeout". The value for the power mode to never timeout (i.e, the current power mode will never progress to a lower power mode) is 0x00.

6.1.1 Ultra-Low Power Mode

In ULP mode, only Cycle 0 (Channels 0 and 5) are sampled. These channels should be used as wake-up channels, allowing the IQS7222A to wake up and switch to a higher power mode when detecting any user interaction.

CH0 and CH5 are sampled at the *ULP report rate*. LTA and filter values for CH0 and CH5 are not processed every cycle, but are processed once every N cycles, based on the *Auto Mode* setting in *Global Cycle Setup*.

The IQS7222A will also wake up periodically to perform a full “Normal Power” cycle. Here, all channels are sampled, and their respective LTAs updated, in order to maintain consistent environmental tracking. The rate at which the IQS7222A performs these “Normal Power” cycles is controlled by the *Normal Power Update Rate in ULP* parameter, also known as the *ULP Timeout*. After this cycle, the IQS7222A returns to ULP mode.

6.2 Count Filter

6.2.1 IIR Filter

The IIR filter applied to the digitised raw input offers various damping options as defined in Tables A.23 and A.24

$$\text{Damping factor} = \frac{\text{Beta}}{256}$$

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7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Below, some are described; the other hardware parameters are not discussed, as they should only be adjusted under the guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high-resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*. If it becomes set again, the master will know a reset has occurred and can react appropriately.

While the *Reset* bit remains set:

- The device will not be able to enter into I²C Event mode operation (i.e. streaming communication behavior will be maintained until the Reset bit is cleared).
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in much longer time to finish the ATI routine.

7.2.2 Software Reset

The IQS7222A can be reset by means of an I²C command (*Soft Reset*).

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8 Additional Features

8.1 Slider

The IQS7222A is capable of processing a slider with on-chip gesture recognition. The IQS7222A supports processing two slider simultaneously, with each slider consisting of up to four touch channels.

Enabled gestures are reported in the *Slider Gesture Status* register. The position of the touch on the slider is reported in the *Slider Position* register.

8.1.1 Slider Setup

The slider is enabled by setting the *Total Channels* field in the *Slider Setup 0* register to a non-zero value and enabling the slider channels by setting the *Channel X Enable* bits in the *Slider Enable Mask* register.

The *Enable Status Link* register must be linked to touch. This activates the slider when any of the enabled channels are in touch.

The *Delta Link* registers, from Delta Link 0 to Delta Link 3, determine the order in which the enabled channels are processed. For example, if channel 1 is the first element in the slider, the *Delta Link 0* register must be set to the appropriate value. Refer to Table A.30 for specific values.

The *Slider Resolution* value defines the output range of the slider position. The gesture setup registers must be set in accordance with the *Slider Resolution*. The touch position ranges from 0 to the *Slider Resolution*, where 0 is the start of the first slider element and the *Slider Resolution* is the end of the last slider element.

The *Upper Calibration Value* field in the *Slider Calibration and Bottom Speed* register and the *Lower Calibration Value* field in the *Slider Setup and Calibration* register are used to offset the end-points of the slider position so that they match the end-points of the physical slider.

The slider output position is dynamically filtered based on the *Slow/Static Beta* in the *Slider Setup and Calibration* register, the *Bottom Speed* field in the *Slider Calibration and Bottom Speed* register, and the value in the *Slider Top Speed* register. The *Slider Top Speed* and *Bottom Speed* are specified in pixels per sample period. Therefore, giving an indication of finger movement speed, i.e. how much the slider output (in pixels) has changed in a sampling period. Figure 8.1 shows the behaviour of the dynamic filter.

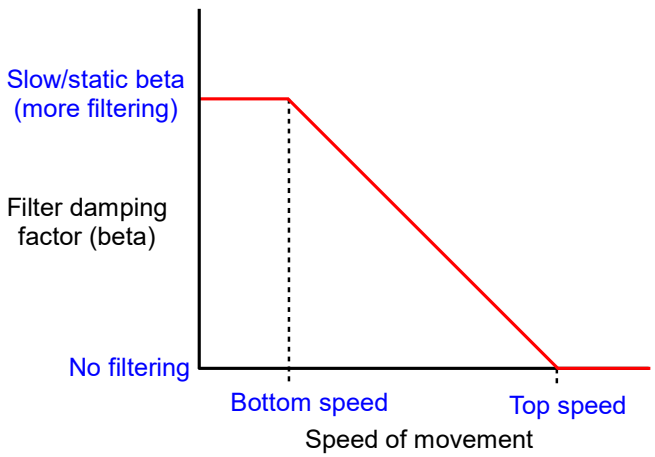

Figure 8.1: Slider Filtering When the Static Filter Bit is Not Set

Bottom and top speed parameters ensure stronger filtering when changes in slider position are in the region of the bottom speed, while ensuring no filtering when the slider position changes rapidly as defined in the top speed parameter. This has value in precise slider applications with very fine adjustment requirements while not losing reactivity when larger movements are made.

If the *Static Filter* bit in the *Slider Setup and Calibration* register is set, the *Slow/Static Beta* is used to filter the slider position regardless of the touch's movement speed.

8.1.2 Gestures

The IQS7222A does on-chip gesture recognition when a slider is enabled.

All gestures are configurable and can be individually enabled using the *Gesture Enable* register. Gestures are reported in the *Slider Gesture Status* register.

The recognised gestures are:

- Single Tap
- Swipe
- Flick

Gesture parameters are specified in pixels and milliseconds.

For any gesture to be reported, a touch must be registered for at least as long as the value in the *Minimum Tap Time* register. This prevents false touches from triggering the gestures.

Tap

A tap gesture will be reported if the touch lasts longer than the *Minimum Tap Time* but less than the time specified in the *Maximum Tap Time* register, and the touch does not move further than the value in the *Minimum Swipe Distance* register from its starting point. The tap will be reported only for the cycle in which it is detected.

Swipe and Flick

Swipe and flick gestures are reported if there is a touch lasting longer than the *Minimum Tap Time*, and the touch moves further from its starting point than the value in the *Minimum Swipe Distance* register. Given that the above conditions have been met, if the touch is released before the time specified in the *Maximum Swipe Time* register, a flick is reported. Otherwise, a swipe is reported.

All gesture flags are cleared once a touch is no longer detected on the slider. This means that taps and flicks are reported once, in the cycle in which they are detected. Swipes are reported for as long as the slider remains in touch. Additionally, there is a 4 second timeout on the slider. All slider gesture events are cleared automatically if the touch on the slider lasts longer than 4 seconds.

8.2 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (Low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.

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- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.
- The default, fixed value of the watchdog timer is 1500 ms.

8.3 RF Immunity

The IQS7222A has immunity to high-power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100pF in parallel with the 2.2μF ceramic on V_{REG}. Place a 4.7μF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470Ω-1kΩ. PCB ground planes also improve noise immunity.

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9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two-wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS7222A supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7222A implements 8-bit addressing with 2 bytes at each address with the exception of extended addresses, which implement 16-bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

The 7-bit device address for order code 001 is 0x44 ('01000100'), while the 7-bit device address for order code 102 is 0x57 ('01010111'). The full address byte for address 0x44 will thus be 0x89 (read) or 0x88 (write), and the full address byte for address 0x57 will be 0xAF (read) or 0xAE (write).

Other address options exist on special request. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement a 16-bit addressing scheme.

9.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to only address each block as an 8-bit address and then continue to clock into the next address locations. For example, if the procedure depicted below is followed, you will read the values from the hypothetical address 0xE000 to 0xE300:

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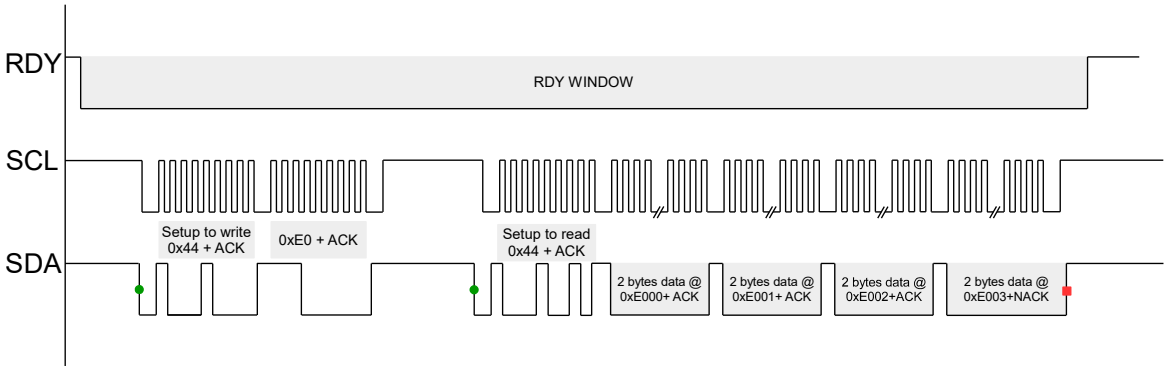

Figure 9.1: Extended 16-bit Addressing for Continuous Block

However, if you need to address a specific byte in that extended memory map space, then you will need to address using the full 16-bit address (note the 16-bit address is high byte first, unlike the data which is low byte first):

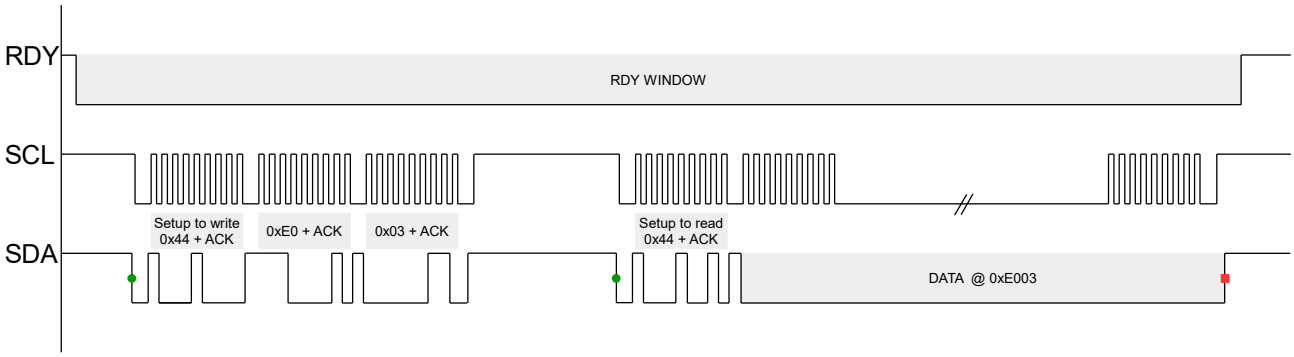

Figure 9.2: Extended 16-bit Addressing for a Specific Register

9.5 Data

The data is 16-bit words, meaning that each address obtains 2 bytes of data. For example, address 0x10 will provide two bytes, and then the next two bytes read will be from address 0x11.

The 16-bit data is sent in little-endian byte order (least significant byte first).

The H file generated by the GUI will display the start address of each block of data, with each address containing 2 bytes. The data of all the addresses can be written consecutively in a single block of data or the entire memory map (refer to Figure 9.1), or data can be written explicitly to a specific address (refer to Figure 9.2). An example of the H file exported by the GUI and the order of the data is shown in Figure 9.3 below.

```
/* Change the Sensor 0 Settings */
/* Memory Map Position 0x30 - 0x39 */
#define SENSOR_0_SETUP_0                    0x01
#define SENSOR_0_SETUP_1                    0x07
```

Start address
LSB
MSB

Figure 9.3: Example of an H file Exported by the GUI

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive; however, the corresponding data was missed/lost, and this should be avoided. The default I²C timeout period is set to 500 ms and can be adjusted in register 0xDD .

9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 0 register 0xDC) is cleared, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

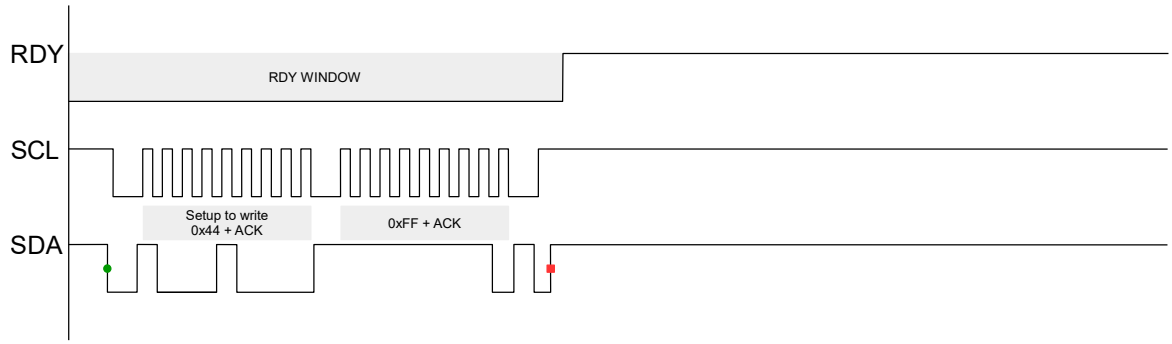

Figure 9.4: Force Stop Communication Sequence

9.8 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep mode, allowing wake-up from the touch device when user presence is detected. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

9.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

9.10 I²C Interface

The IQS7222A has 3 *I²C interface options*, as described in the sections below.

9.10.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register *0xD4* (normal power), register *0xD6* (low power) and register *0xD8* (ultra low power),

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respectively.

9.10.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs.

9.10.3 I²C Stream in Touch Mode

Stream in touch is a hybrid I²C mode between streaming mode and event mode. The device follows event mode I²C protocol, but when a touch is registered on any channel, the device enters streaming mode until the touch is released.

The hybrid I²C interface is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

9.11 Event Mode Communication

Event mode can only be entered if the following requirements are met:

- *Reset* bit must be cleared by acknowledging the device reset condition occurrence through writing *Ack Reset* bit to clear the System status flag.
- Events must be serviced by reading from the *Events* register 0x11 to ensure all events flags are cleared otherwise continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode

9.11.1 Events

Numerous events can be individually enabled to trigger communication; bit definitions can be found in Tables A.2 and A.3:

- Power mode change
- Prox or touch event
- ATI error
- ATI active
- ATI Event
- Slider Event

9.11.2 Force Communication

In streaming mode, the IQS7222A I²C will provide Ready (RDY) windows at intervals specified in the power mode report rate. Ideally, communication with the IQS7222A should only be initiated in a Ready window, but a communication request described in Figure 9.5 below will force a Ready window to open. In event mode, Ready windows are only provided when an event is reported, an Ready window must be requested to write or read settings outside of this window. The time between the communication request and the opening of a RDY window (t_{wait}) is dependent on the report rate of the current power mode. The t_{wait} can extend up to the current report rate +20% due to variability in the clock. For example, if a report rate of 100 ms is chosen, the report rate may vary between 80 ms and 120 ms[i].

[i] Please contact Azoteq for an application specific value of t_{wait}

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There is a possibility of a communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period. However, it is essential to retry at different timings that are not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional precautionary measure, the IC can be reset using the MCLR pin and reinitialised if there is no response after a specified number of retries.

A force communication request should be avoided while RDY is in the LOW state. If a communication request is sent at the exact moment when an event causes RDY to go low, the window will close again after sending the I^2C STOP signal. In such a scenario, the device will provide an invalid communication response (0xEE) because the host is attempting to read from the device outside of a communication window (i.e., while RDY is high). To prevent this issue, it is recommended to read the product number during each ready window to ensure that the response received is valid.

A slight delay may occur in receiving an acknowledgement (ACK) when attempting force communication while the device is in an internal lower power mode with certain peripherals switched off. This delay can occur regardless of the state of the current system power mode.

The communication request sequence is shown in Figure 9.5 below.

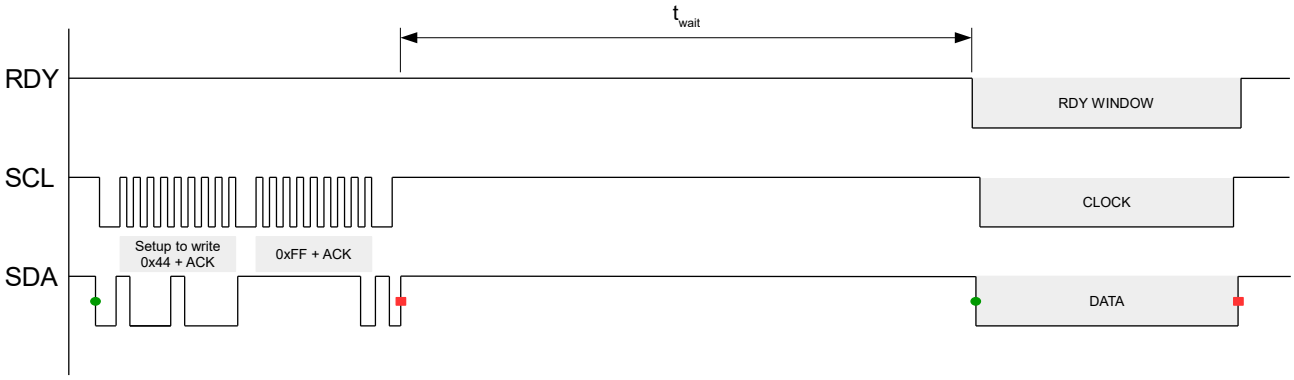

Figure 9.5: Force Communication Sequence

9.12 Program Flow Diagram

The program flow for event mode communication is shown in 9.6

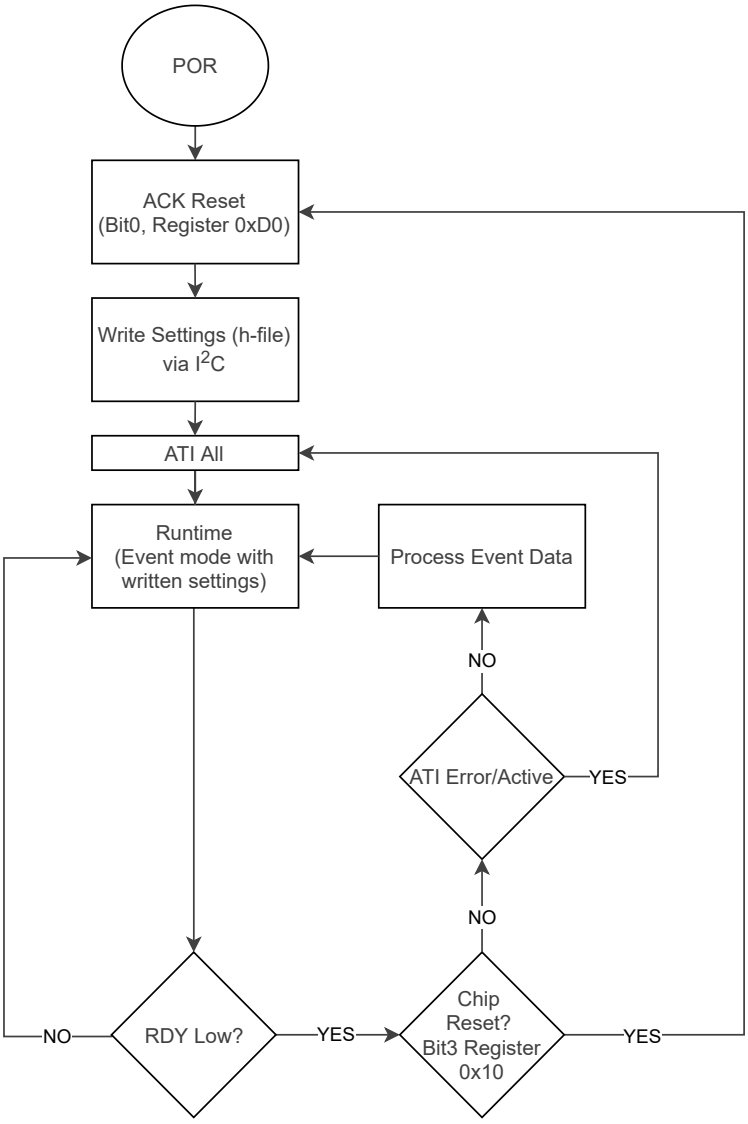

Figure 9.6: Progam Flow Diagram

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
Read Only		
0x10	System Status	See Table A.2
0x11	Events	See Table A.3
0x12	Proximity event States	See Table A.4
0x13	Touch event States	See Table A.5
0x14	Slider 0 Position	16-bit value
0x15	Slider 1 Position	
0x16	Slider 0 Gesture Status	See Table A.6
0x17	Slider 1 Gesture Status	
Read Only	**Channel Counts**	
0x20	Channel 0 Counts	16-bit value
0x21	Channel 1 Counts	
0x22	Channel 2 Counts	
0x23	Channel 3 Counts	
0x24	Channel 4 Counts	
0x25	Channel 5 Counts	
0x26	Channel 6 Counts	
0x27	Channel 7 Counts	
0x28	Channel 8 Counts	
0x29	Channel 9 Counts	
0x2A	Channel 10 Counts	
0x2B	Channel 11 Counts	
Read Only	**Channel LTA**	
0x30	Channel 0 LTA	16-bit value
0x31	Channel 1 LTA	
0x32	Channel 2 LTA	
0x33	Channel 3 LTA	
0x34	Channel 4 LTA	
0x35	Channel 5 LTA	
0x36	Channel 6 LTA	
0x37	Channel 7 LTA	
0x38	Channel 8 LTA	
0x39	Channel 9 LTA	
0x3A	Channel 10 LTA	
0x3B	Channel 11 LTA	
Read-Write	Cycle Setup	
0x8000	Cycle Setup 0	See Table A.7
0x8001		See Table A.8
0x8002		See Table A.9
0x8100	Cycle Setup 1	See Table A.7
0x8101		See Table A.8
0x8102		See Table A.9
0x8200	Cycle Setup 2	See Table A.7
0x8201		See Table A.8
0x8202		See Table A.9

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0x8300	Cycle Setup 3	See Table A.7
0x8301		See Table A.8
0x8302		See Table A.9
0x8400	Cycle Setup 4	See Table A.7
0x8401		See Table A.8
0x8402		See Table A.9
0x8500	Cycle Setup 5	See Table A.7
0x8501		See Table A.8
0x8502		See Table A.9
0x8600	Cycle Setup 6	See Table A.7
0x8601		See Table A.8
0x8602		See Table A.9
0x8700	Global Cycle Setup	See Table A.10
0x8701	Coarse and Fine Divider Preloads	See Table A.11
0x8702	Compensation Preload	See Table A.12
Read-Write	**Button Setup - Thresholds, Hysteresis and Debounce**	
0x9000	Button Setup 0	See Table A.13
0x9001		See Table A.14
0x9002		See Table A.15
0x9100	Button Setup 1	See Table A.13
0x9101		See Table A.14
0x9102		See Table A.15
0x9200	Button Setup 2	See Table A.13
0x9201		See Table A.14
0x9202		See Table A.15
0x9300	Button Setup 3	See Table A.13
0x9301		See Table A.14
0x9302		See Table A.15
0x9400	Button Setup 4	See Table A.13
0x9401		See Table A.14
0x9402		See Table A.15
0x9500	Button Setup 5	See Table A.13
0x9501		See Table A.14
0x9502		See Table A.15
0x9600	Button Setup 6	See Table A.13
0x9601		See Table A.14
0x9602		See Table A.15
0x9700	Button Setup 7	See Table A.13
0x9701		See Table A.14
0x9702		See Table A.15
0x9800	Button Setup 8	See Table A.13
0x9801		See Table A.14
0x9802		See Table A.15
0x9900	Button Setup 9	See Table A.13
0x9901		See Table A.14
0x9902		See Table A.15
0x9A00	Button Setup 10	See Table A.13
0x9A01		See Table A.14
0x9A02		See Table A.15
0x9B00	Button Setup 11	See Table A.13
0x9B01		See Table A.14
0x9B02		See Table A.15

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Read-Write	Channel Setup - ATI Parameters, Reference Channel and Rx Select	
	Channel 0	
0xA000	CRX Select and General Channel Setup	See Table A.16
0xA001	ATI Base and Target	See Table A.18
0xA002	Fine and Coarse Multipliers	See Table A.19
0xA003	ATI Compensation	See Table A.20
0xA004	Reference Channel Settings 0	See Table A.21
0xA005	Reference Channel Settings 1	See Table A.22
	Channel 1	
0xA100	CRX Select and General Channel Setup	See Table A.16
0xA101	ATI Base and Target	See Table A.18
0xA102	Fine and Coarse Multipliers	See Table A.19
0xA103	ATI Compensation	See Table A.20
0xA104	Reference Channel Settings 0	See Table A.21
0xA105	Reference Channel Settings 1	See Table A.22
	Channel 2	
0xA200	CRX Select and General Channel Setup	See Table A.16
0xA201	ATI Base and Target	See Table A.18
0xA202	Fine and Coarse Multipliers	See Table A.19
0xA203	ATI Compensation	See Table A.20
0xA204	Reference Channel Settings 0	See Table A.21
0xA205	Reference Channel Settings 1	See Table A.22
	Channel 3	
0xA300	CRX Select and General Channel Setup	See Table A.16
0xA301	ATI Base and Target	See Table A.18
0xA302	Fine and Coarse Multipliers	See Table A.19
0xA303	ATI Compensation	See Table A.20
0xA304	Reference Channel Settings 0	See Table A.21
0xA305	Reference Channel Settings 1	See Table A.22
	Channel 4	
0xA400	CRX Select and General Channel Setup	See Table A.16
0xA401	ATI Base and Target	See Table A.18
0xA402	Fine and Coarse Multipliers	See Table A.19
0xA403	ATI Compensation	See Table A.20
0xA404	Reference Channel Settings 0	See Table A.21
0xA405	Reference Channel Settings 1	See Table A.22
	Channel 5	
0xA500	CRX Select and General Channel Setup	See Table A.17
0xA501	ATI Base and Target	See Table A.18
0xA502	Fine and Coarse Multipliers	See Table A.19
0xA503	ATI Compensation	See Table A.20
0xA504	Reference Channel Settings 0	See Table A.21
0xA505	Reference Channel Settings 1	See Table A.22
	Channel 6	
0xA600	CRX Select and General Channel Setup	See Table A.17
0xA601	ATI Base and Target	See Table A.18
0xA602	Fine and Coarse Multipliers	See Table A.19
0xA603	ATI Compensation	See Table A.20
0xA604	Reference Channel Settings 0	See Table A.21
0xA605	Reference Channel Settings 1	See Table A.22

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	Channel 7	
0xA700	CRX Select and General Channel Setup	See Table A.17
0xA701	ATI Base and Target	See Table A.18
0xA702	Fine and Coarse Multipliers	See Table A.19
0xA703	ATI Compensation	See Table A.20
0xA704	Reference Channel Settings 0	See Table A.21
0xA705	Reference Channel Settings 1	See Table A.22
	Channel 8	
0xA800	CRX Select and General Channel Setup	See Table A.17
0xA801	ATI Base and Target	See Table A.18
0xA802	Fine and Coarse Multipliers	See Table A.19
0xA803	ATI Compensation	See Table A.20
0xA804	Reference Channel Settings 0	See Table A.21
0xA805	Reference Channel Settings 1	See Table A.22
	Channel 9	
0xA900	CRX Select and General Channel Setup	See Table A.17
0xA901	ATI Base and Target	See Table A.18
0xA902	Fine and Coarse Multipliers	See Table A.19
0xA903	ATI Compensation	See Table A.20
0xA904	Reference Channel Settings 0	See Table A.21
0xA905	Reference Channel Settings 1	See Table A.22
	Hall Switch Channel	
0xAA00	CRX Select and General Channel Setup	See Table A.17
0xAA01	ATI Base and Target	See Table A.18
0xAA02	Fine and Coarse Multipliers	See Table A.19
0xAA03	ATI Compensation	See Table A.20
0xAA04	Reserved	Value = 0x0000
0xAA05	Reserved	Value = 0x0000
	Hall effect Control Channel	
0xAB00	CRX Select and General Channel Setup	See Table A.17
0xAB01	ATI Base and Target	See Table A.18
0xAB02	Fine and Coarse Multipliers	See Table A.19
0xAB03	ATI Compensation	See Table A.20
0xAB04	Reserved	Value = 0x0000
0xAB05	Reserved	Value = 0x0000
Read-Write	**Filter Betas**	
0xAC00	Filter Beta	See Table A.23
0xAC01	Fast Filter Beta	See Table A.24
Read-Write	**Slider 0 Setup**	
0xB000	Slider 0 General Setup	See Table A.25
0xB001	Calibration and Bottom Speed	See Table A.26
0xB002	Top Speed/Resolution	See table A.27
0xB003	Slider Enable Mask	See Table A.28
0xB004	Slider Enable Status Link	See Table A.29
0xB005	Delta Link 0	See Table A.30
0xB006	Delta Link 1	See Table A.30
0xB007	Delta Link 2	See Table A.30
0xB008	Delta Link 3	See Table A.30
0xB009	Gesture Setup 0	See Table A.31
0xB00A	Gesture Setup 1	See Table A.32

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Read-Write	Slider 1 Setup	
0xB100	Slider 1 General Setup	See Table A.25
0xB101	Calibration and Bottom Speed	See Table A.26
0xB102	Top Speed/Resolution	See table A.27
0xB103	Slider Enable Mask	See Table A.28
0xB104	Slider Enable Status Link	See Table A.29
0xB105	Delta Link 0	See Table A.30
0xB106	Delta Link 1	See Table A.30
0xB107	Delta Link 2	See Table A.30
0xB108	Delta Link 3	See Table A.30
0xB109	Gesture Setup 0	See Table A.31
0xB10A	Gesture Setup 1	See Table A.32
Read-Write	**GPIO0 Settings**	
0xC000	GPIO0 Enable and Configuration Settings	See Table A.33
0xC001	GPIO0 Mask	See Table A.34
0xC002	GPIO0 Enable Status Link	See Table A.29
Read-Write	**PMU and System Settings**	
0xD0	Control settings	See Table A.36
0xD1	ATI Error Timeout	16-bit value * 0.5 (s)
0xD2	ATI Report Rate	16-bit value (ms)
0xD3	Normal Power Mode Timeout	16-bit value (ms)
0xD4	Normal Power Mode Report Rate	16-bit value (ms) Range: 0 - 3000
0xD5	Low Power Mode Timeout	16-bit value (ms)
0xD6	Low Power Mode Report Rate	16-bit value (ms) Range: 0 - 3000
0xD7	Normal Power Update rate in Ultra-low Power Mode	16-bit value (ms)
0xD8	Ultra-low Power Mode Report Rate	16-bit value (ms) Range: 0 - 3000
0xD9	ULP Entry Mask	See Table A.37
0xDA	Event Enable	See Table A.38
0xDB	Hall Offset and Bias Current	See Table A.39
0xDC	I^2C Communication	See Table A.40
0xDD	Communication Timeout	See Table A.41

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11 Implementation and Layout

11.1 Layout Fundamentals

Note: Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

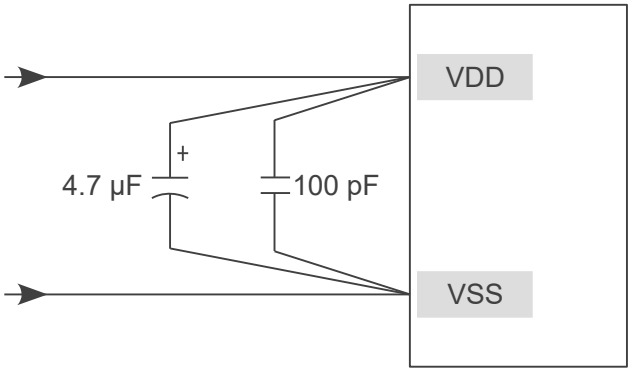

Figure 11.1: Recommended Power Supply Decoupling

11.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. Figure 11.2 below shows an example placement of the VREG capacitors.

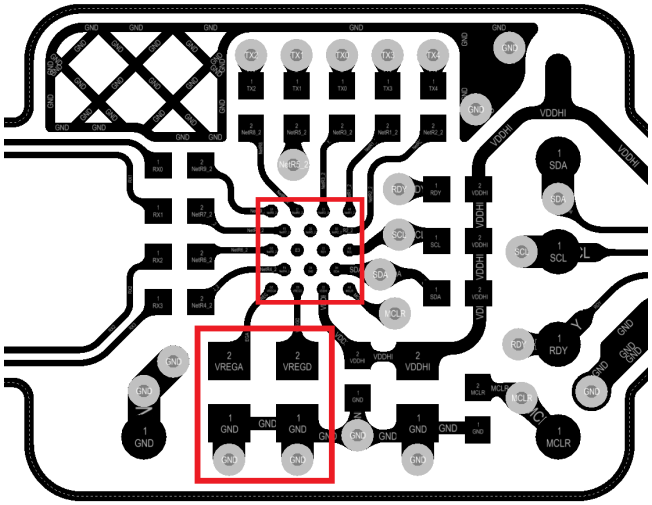

Figure 11.2: VREG Capacitor Placement Close to IC

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11.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

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12 Ordering Information

12.1 Ordering Code

IQS7222A zzz ppb

Table 12.1: Order Code Description

IC NAME				IQS7222A
POWER-ON CONFIGURATION	zzz	=	001	I^2C address 0x44
		=	102	I^2C address 0x57[i]
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
		=	QN	QFN-20 package
		=	QF	QFN-20 package
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Example : IQS7222A001QFR

12.2 Top Marking

12.2.1 WLCSP18 Package Marking (IQS7222AzzzCSR)

Package outline can be found in Section 13.5.

Product Name
ppp = product code
xx = batchcode

12.2.2 QFN20 Package Marking Option 1 (IQS7222AzzzQFR)

Package outline can be found in Section 13.1.

Product Name
ppp = product code
xx = batchcode

[i] Please refer to product information notice PIN-230172 for more details

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12.2.3 QFN20 Package Marking Option 2 (IQS7222AzzzQNR)

Package outline can be found in Section 13.3.

Product Name
ppp = product code
xx = batchcode

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13 Package Specification

13.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

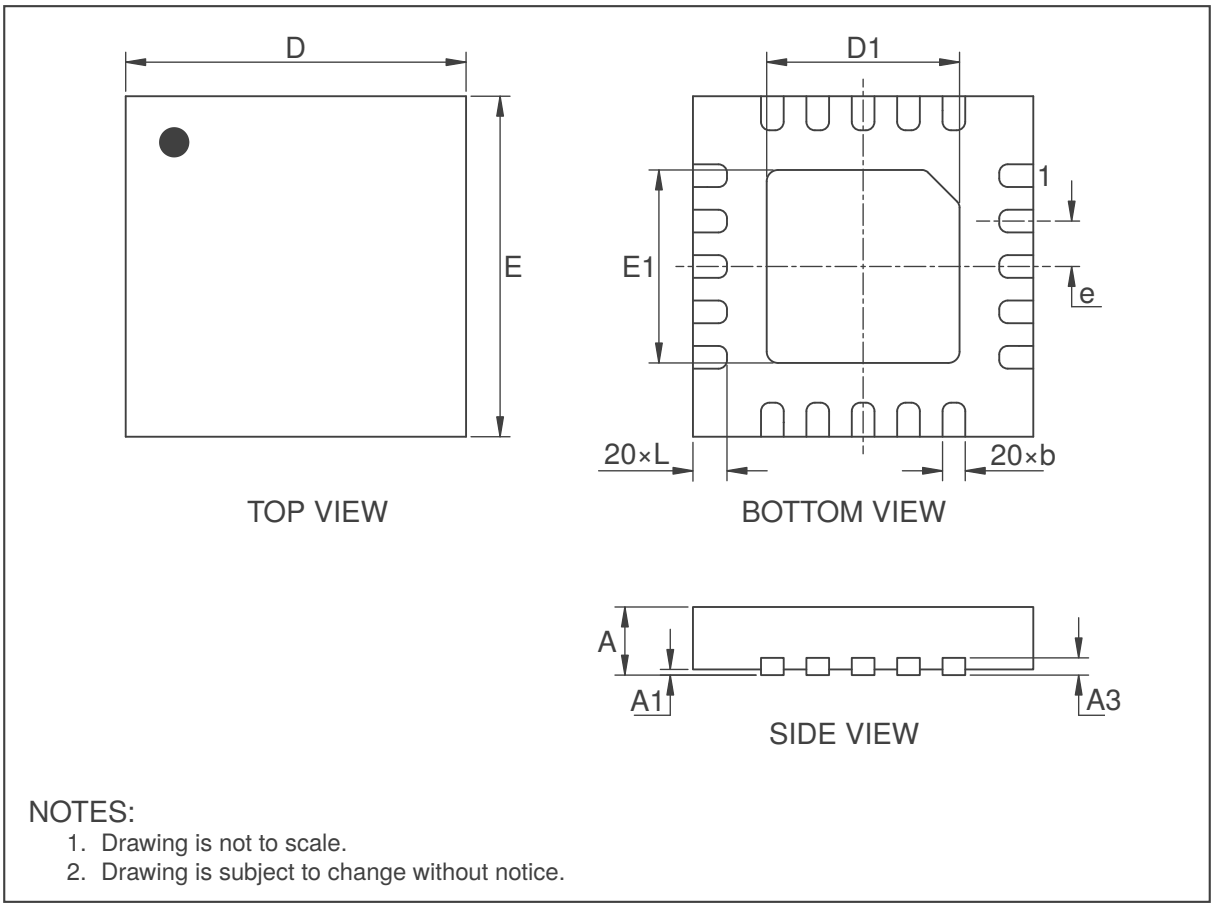

Figure 13.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

Table 13.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

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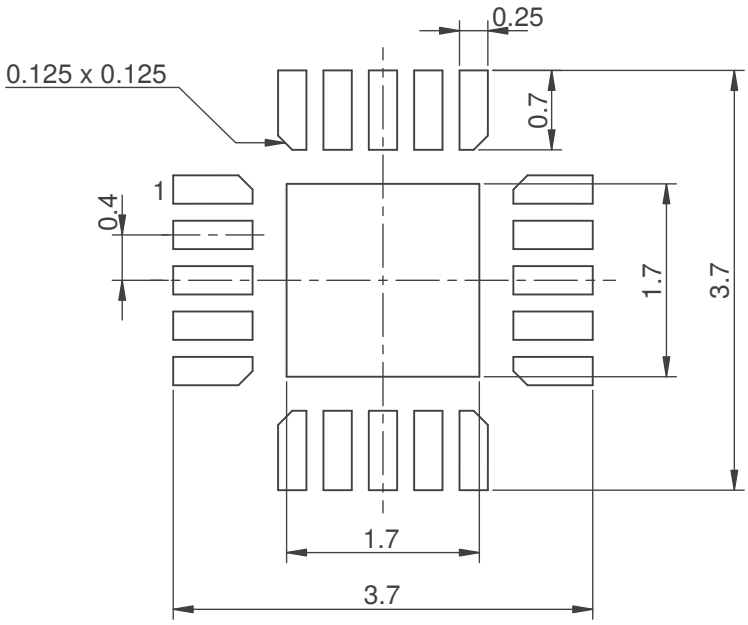
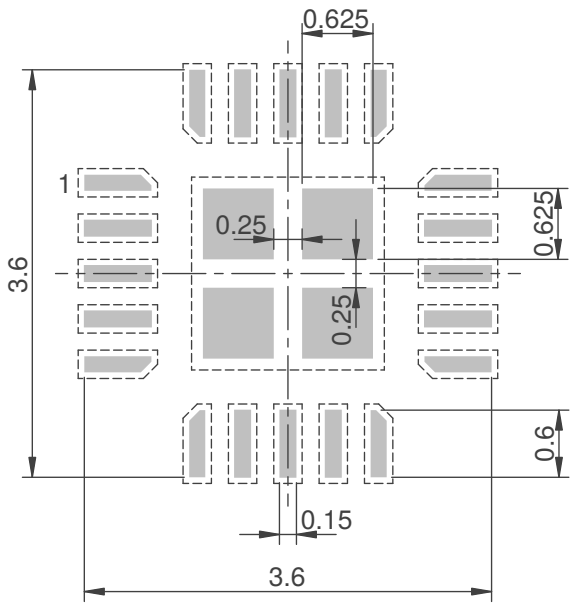
13.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.2: QFN (3x3)-20 (QFR) Recommended Footprint

13.3 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

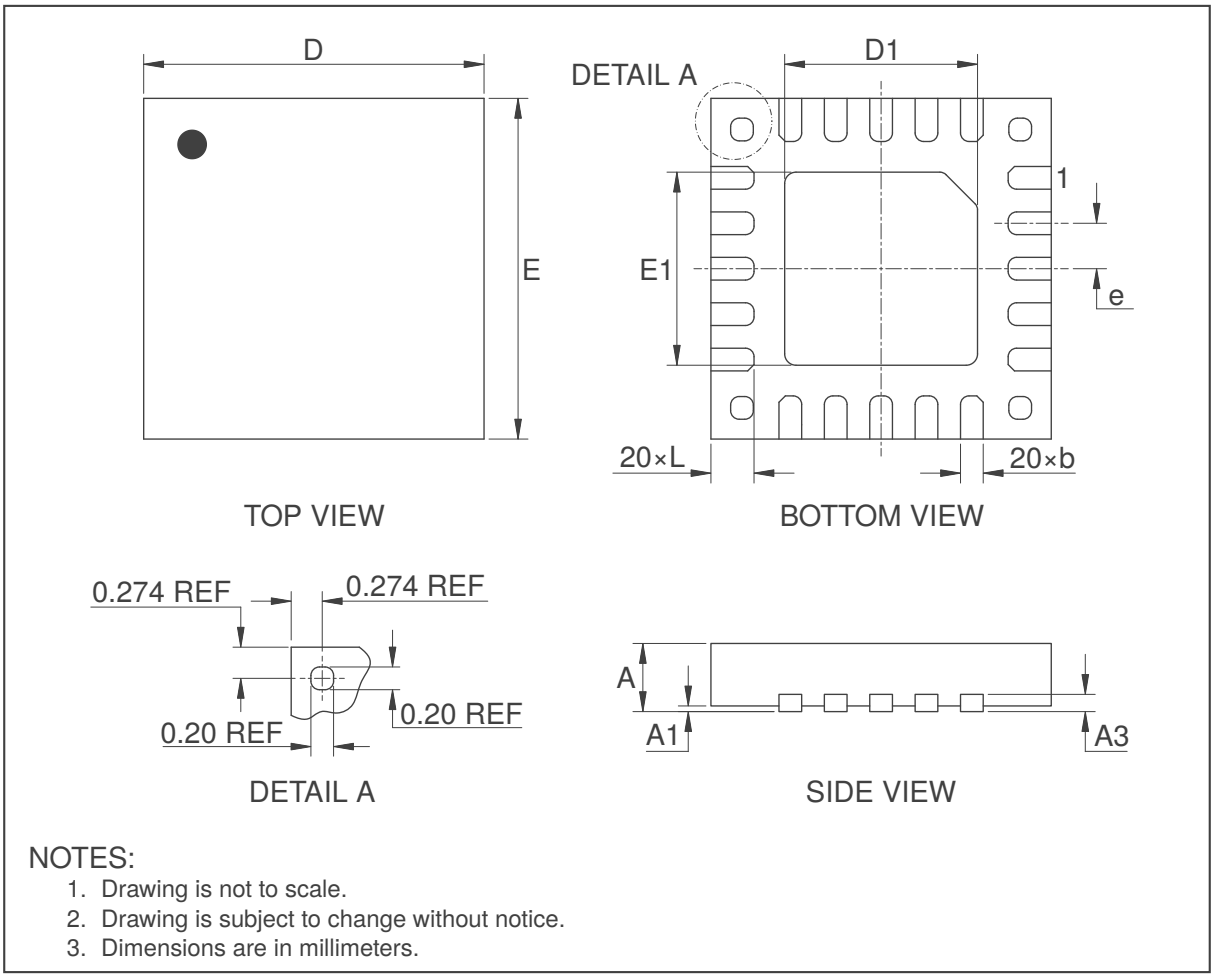


Figure 13.3: QFN (3x3)-20 (QNR) Package Outline Visual Description

Table 13.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

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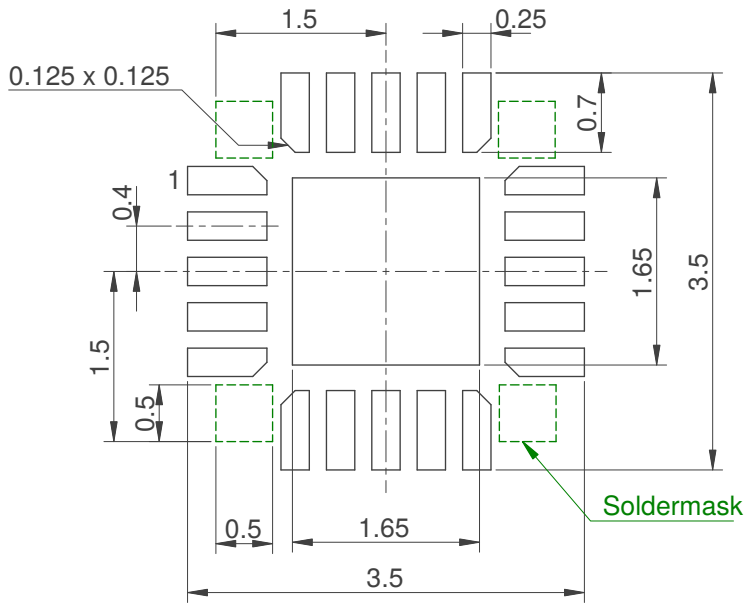
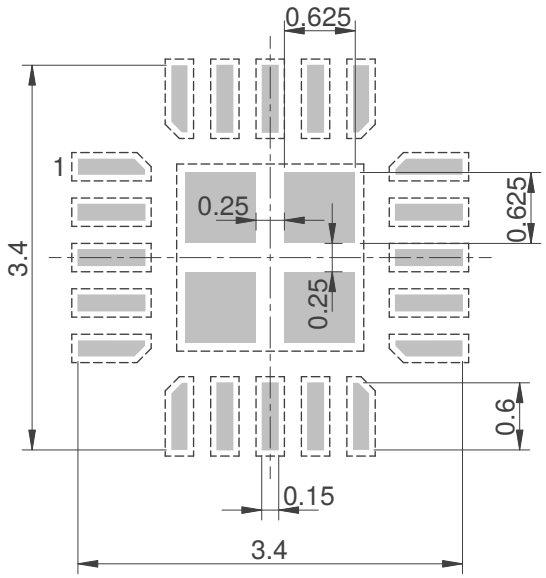
13.4 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 13.4: QFN (3x3)-20 (QNR) Recommended Footprint

13.5 Package Outline Description – WLCSP18

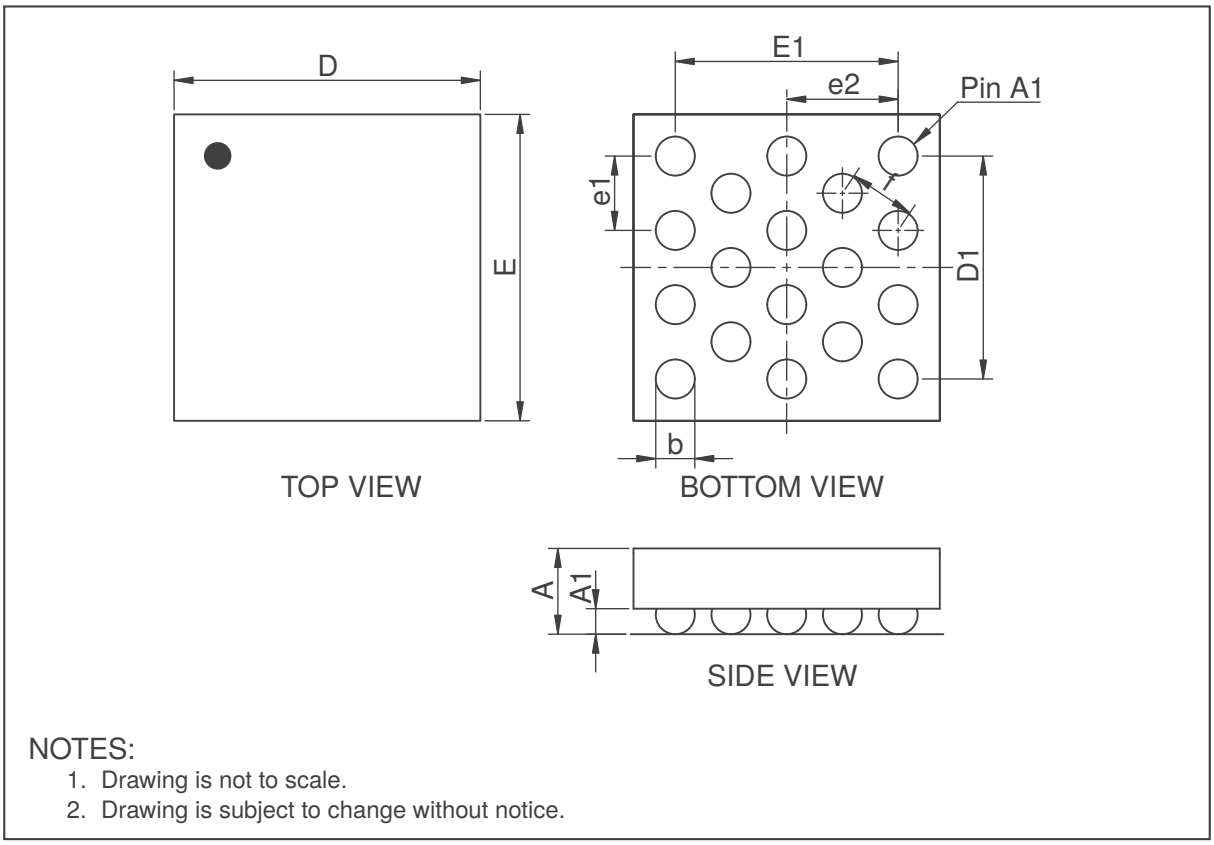


Figure 13.5: WLCSP (1.62x1.62)-18 Package Outline Visual Description

Table 13.3: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1	1.200 BSC		
E1	1.200 BSC		
e1	0.400 BSC		
e2	0.600 BSC		
f	0.360 REF		

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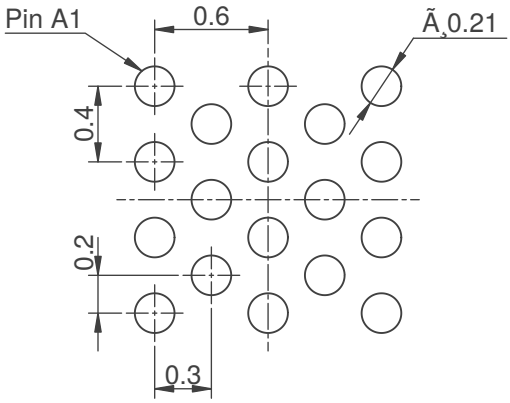
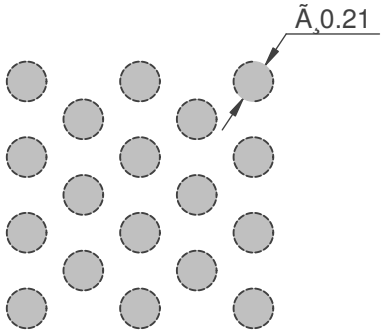
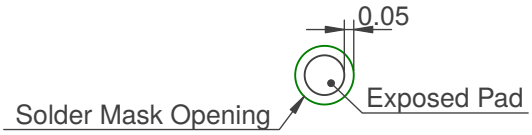
13.6 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



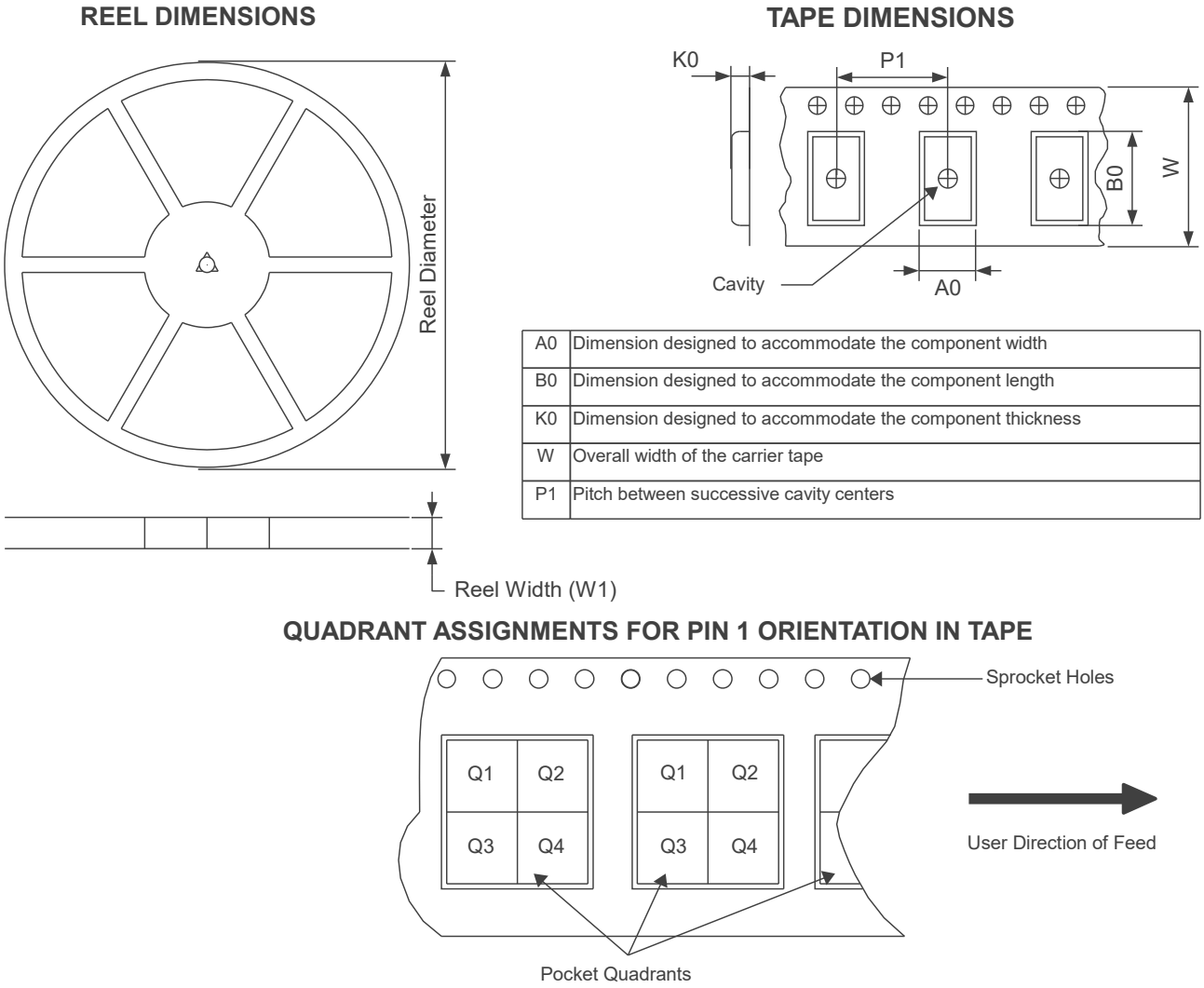
SOLDER MASK BACK-OFF

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.6: WLCSP18 Recommended Footprint

13.7 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 13.7: Tape and Reel Specification

Table 13.4: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2
WLCSP18	18	179	8.4	1.78	1.78	0.69	4	8	Q1

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13.8 Moisture Sensitivity Levels

Table 13.5: Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

13.9 Reflow Specifications

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A Memory Map Descriptions

Please note: The value of all Read-write bits marked as Reserved, unless otherwise specified, can be set to 0 or 1 depending on customer's preference.

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Catergory	Name	Value	Order Code	
0x00	Application Version Info	Product Number	840		16-bit value
0x01		Major Version	1		
0x02		Minor Version	15	001	
			18	102[i]	
0x03		Patch Number (commit hash)	Reserved		
0x04					
0x05	ROM Library Version Info	Library Number	Reserved		
0x06		Major Version	Reserved		
0x07		Minor Version	Reserved		
0x08		Patch Number (commit hash)	Reserved		
0x09					

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	NP up-date	Power mode		Reset	Res	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global Halt not active
  - 1: Global Halt active
- Bit 6: **Normal Power Update**
  - 0: No Normal Power Update occured
  - 1: Normal Power update occured
- Bit 4-5: **Current Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.3: Events

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Event	ATI Event	Slider 1	Slider 0	Reserved								Touch Event	Prox Event

- Bit 13: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 12: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 11: **Slider 1 Event**

[i] Please refer to product information notice PIN-230172 for more details

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- 0: No Event occurred on Slider 1
- 1: Event occurred on Slider 1

- Bit 10: **Slider 0 Event**
  - 0: No Event occurred on Slider 0
  - 1: Event occurred on Slider 0
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Proximity Event**
  - 0: No Proximity Event occurred
  - 1: Proximity Event occurred

Table A.4: Proximity Event States

Register: 0x12

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Hall	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Proximity Event**
  - 0: No Proximity event occurred on channel
  - 1: Proximity event occurred on channel

Table A.5: Touch Event States

Register: 0x13

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Hall	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.6: Slider Gesture Status

Register: 0x16, 0x17

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Busy	Event	Neg	Reserved		Flick	Swipe	Tap

- Bit 7: **Busy**
  - 0: Slider not busy
  - 1: Slider busy
- Bit 6: **Gesture Event**
  - 0: No slider gesture event occurred
  - 1: Slider gesture event occurred
- Bit 5: **Negative**
  - 0: Gesture event occurred in positive direction
  - 1: Gesture event occurred in negative direction
- Bit 2: **Flick**
  - 0: No flick event occurred
  - 1: Flick event occurred
- Bit 1: **Swipe**
  - 0: No swipe event occurred
  - 1: Swipe event occurred
- Bit 0: **Tap**
  - 0: No tap event occurred
  - 1: Tap event occurred

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Table A.7: Cycle Setup 0

Register: 0x8000, 0x8100, 0x8200, 0x8300, 0x8400, 0x8500, 0x8600

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 8-15: **Conversion Frequency Period**
  - The calculation of the charge transfer frequency (f_{xfer}) is shown below. The relevant formula is determined by the value of the dead time enabled bit (refer to Table A.8)
  - Dead time disabled: $f_{\text{xfer}} = \frac{f_c lk}{2*period+2}$
  - Dead time enabled: $f_{\text{xfer}} = \frac{f_c lk}{2*period+3}$
  - Range: 0 - 127
- Bit 0-7: **Conversion Frequency Fraction**
  - $256 * \frac{f_{\text{conv}}}{f_{\text{clk}}}$
  - Range: 0 - 255
- **Note:** if Conversion frequency fraction is fixed at 127 and dead time is enabled, the following values of the conversion period will result in the corresponding charge transfer frequencies:
  - 1: 2MHz
  - 5: 1MHz[ii]
  - 12: 500kHz
  - 17: 350kHz
  - 26: 250kHz
  - 53: 125kHz

Table A.8: Cycle Setup 1

Register: 0x8001, 0x8101, 0x8201, 0x8301, 0x8401, 0x8501, 0x8601

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1	CTX0	GND Inactive Rxs	Dead time enabled	FOSC TX Freq	Vbias enable	PXS Mode		

- Bit 15: **CTx8**
  - 0: CTx8 disabled
  - 1: CTx8 enabled
- Bit 14: **CTx7**
  - 0: CTx7 disabled
  - 1: CTx7 enabled
- Bit 13: **CTx6**
  - 0: CTx6 disabled
  - 1: CTx6 enabled
- Bit 12: **Tx5**
  - 0: CTx5 disabled
  - 1: CTx5 enabled
- Bit 11: **CTx4**
  - 0: CTx4 disabled
  - 1: CTx4 enabled
- Bit 10: **CTx3**
  - 0: CTx3 disabled
  - 1: CTx3 enabled
- Bit 9: **CTx2**
  - 0: CTx2 disabled
  - 1: CTx2 enabled
- Bit 8: **CTx1**
  - 0: CTx1 disabled
  - 1: CTx1 enabled
- Bit 7: **CTx0**
  - 0: CTx0 disabled
  - 1: CTx0 enabled
- Bit 6: **Ground Inactive Rx's**
  - 0: Inactive Rx floating

[ii] Please note: The maximum charge transfer frequency for mutual capacitive mode (refer to Table A.8) is 1MHz

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- 1: Inactive Rx Grounded
- Bit 5: **Dead Time Enabled**
  - 0: Deadtime disabled
  - 1: Deadtime enabled
- Bit 4: **FOSC Tx Frequency**
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Vbias Enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-2: **PXS Mode**
  - 000: None
  - 001: Self-capacitive
  - 010: Mutual capacitive [iii]
  - 011: Resonant inductance

Table A.9: Cycle Setup 2

Register: 0x8002, 0x8102, 0x8202, 0x8302, 0x8402, 0x8502, 0x8602

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					Current Reference Enable	Current Reference Output		Current Reference Level				Current Reference Trim			

- Bit 10: **Current Reference Enable**
  - 0: Disable current reference
  - 1: Enable current reference
- Bit 8-9: **Current Reference Output**
  - 00: Disabled
- Bit 4-7: **Current Reference Level**
  - 4 bit value to scale current output
  - Higher values will result in a higher output current
- Bit 0-3: **Current Reference Trim**
  - 4 bit value to adjust current supply output
  - Higher values will result in a higher output current

Table A.10: Global Cycle Setup

Register: 0x8700

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	Maximum counts		0	1	0	1	1	1	0	0	0	Auto Mode		1	1

- Bit 13-14: **Maximum counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384
- Bit 2-3: **Auto Mode**
  - When in ULP mode, this defines how many samples will be done by an autonomous circuit (sensing only CH0 and CH5) before waking up and processing the CH0 and CH5 LTAs. A higher value will ensure lowest possible power consumption where, e.g., 32 samples will be taken of CH0 and CH5 before the device wakes up to process LTAs.
  - 00: 4
  - 01: 8
  - 10: 16
  - 11: 32

[iii] Please note that the maximum allowed charge transfer frequency (see Table A.7) for Mutual capacitive mode is 1MHz i.e frequency period $\geq$ 5

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Table A.11: Coarse and Fine Multipliers Preload

Register: 0x8701

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Divider Preload					Reserved				Coarse Divider Preload				

- Bit 0-4: **Coarse Divider Preload**
  - 5-bit coarse divider preload value
- Bit 9-13: **Fine Divider Preload**
  - 5-bit fine divider preload value

Table A.12: ATI Compensation Preload

Register: 0x8702

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						ATI Compensation Preload									

- Bit 0-9: **ATI Compensation Preload**
  - 10-bit preload value

Table A.13: Button Setup 0

Register: 0x9000, 0x9100, 0x9200, 0x9300, 0x9400, 0x9500, 0x9600, 0x9700, 0x9800, 0x9900, 0x9A00, 0x9B00

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit				Enter				Proximity Threshold							

- Bit 12-15: **Exit Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 8-11: **Enter Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 0-7: **Proximity Threshold**
  - 8-bit value

Table A.14: Button Setup 1

Register: 0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501, 0x9601, 0x9701, 0x9801, 0x9901, 0x9A01, 0x9B01

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 8-15: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
  - $\frac{\text{LTA * Threshold bit value}}{2^8} - \frac{\text{Threshold bit value * Hysteresis bit value * LTA}}{2^{16}}$
- Bit 0-7: **Touch Threshold**
  - $\frac{LTA}{256} * \text{8bit value}$

Table A.15: Button Setup 2

Register: 0x9002, 0x9101, 0x9202, 0x9302, 0x9402, 0x9502, 0x9602, 0x9702, 0x9802, 0x9902

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Event Timeout								Prox Event Timeout							

- Bit 8-15: **Touch Event Timeout**
  - 8-bit value * 500 ms
  - 0: Never timeout (recommended for use with follower and reference channels and required for ULP entry channels retaining an active state in ULP)
- Bit 0-7: **Proximity Event Timeout**
  - 8-bit value * 500 ms
  - 0: Never timeout (recommended for use with follower and reference channels)

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Table A.16: CRX Select and General Channel Setup(CH0-CH4)

Register: 0xA000, 0xA100, 0xA200, 0xA300, 0xA400

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode		ATI Band		Global halt	Invert	Dual	Enabled	CRX3	CRX2	CRX1	CRX0	Cs Size	VRef 0.5V	Proj Bias Select	

- Bit 14-15: **Mode**
  - 00: Independent
  - 01: Reference
  - 10: Follower
- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a proximity/-touch state. The function is aimed at slider applications
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional Sensing**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx3**
  - 0: CRx3 disabled
  - 1: CRx3 enabled
- Bit 6: **CRx2**
  - 0: CRx2 disabled
  - 1: CRx2 enabled
- Bit 5: **CRx1**
  - 0: CRx1 disabled
  - 1: CRx1 enabled
- Bit 4: **CRx0**
  - 0: CRx0 disabled
  - 1: CRx0 enabled
- Bit 3: **Cs Size**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **Vref 0.5V**
  - Decrease internal sampling capacitor size
  - 0: Vref 0.5V disabled - C_s = Value chosen in Cs 80pF bit (40pF/80pF)
  - 1: Vref 0.5V enabled - C_s = Half of the value chosen in Cs 80pF bit (40pF/80pF)
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

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Table A.17: CRX Select and General Channel Setup(CH5-CH9)

Register: 0xA500, 0xA600, 0xA700, 0xA800, 0xA900, 0xAA00, 0xAB00

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode		ATI Band		Global halt	Invert	Dual	Enabled	CRX7	CRX6	CRX5	CRX4	Cs Size	Vref 0.5V	Proj Bias Select	

- Bit 14-15: **Mode**
  - 00: Independent
  - 01: Reference
  - 10: Follower
- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a proximity/-touch state. The function is aimed at slider applications.
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode.
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional Sensing**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx7**
  - 0: CRx7 disabled
  - 1: CRx7 enabled
- Bit 6: **CRx6**
  - 0: CRx6 disabled
  - 1: CRx6 enabled
- Bit 5: **CRx5**
  - 0: CRx5 disabled
  - 1: CRx5 enabled
- Bit 4: **CRx4**
  - 0: CRx4 disabled
  - 1: CRx4 enabled
- Bit 3: **Cs Size**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **Vref 0.5V**
  - Decrease internal sampling capacitor size
  - 0: Vref 0.5 V disabled - C_s = Value chosen in Cs 80 pF bit (40 pF/80 pF)
  - 1: Vref 0.5 V enabled - C_s = Half of the value chosen in Cs 80 pF bit (40 pF/80 pF)
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

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Table A.18: ATI Base and Target

Register:	0xA001, 0xA101, 0xA201, 0xA301, 0xA401, 0xA501, 0xA601, 0xA701, 0xA801, 0xA901, 0xAA01, 0xAB01														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target								ATI Base					ATI Mode		

- Bit 8-15: **ATI Target**
  - 8-bit value * 8
- Bit 3-7: **ATI Base**
  - 5-bit value * 16
- Bit 0-2: **ATI Mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI

Table A.19: Fine and Coarse Multipliers

Register:	0xA002, 0xA102, 0xA202, 0xA302, 0xA402, 0xA502, 0xA602, 0xA702, 0xA802, 0xA902, 0xAA02, 0xAB02														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.20: ATI Compensation

Register:	0xA003, 0xA103, 0xA203, 0xA303, 0xA403, 0xA503, 0xA603, 0xA703, 0xA803, 0xA903, 0xAA03, 0xAB03														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.21: Reference Channel Settings 0

Register:	0xA004, 0xA104, 0xA204, 0xA304, 0xA404, 0xA504, 0xA604, 0xA704, 0xA804, 0xA904														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reference Follower Mask Link Ptr/ Sensor Mask															

- Please note that the register value is used for either Follower Mask Link Ptr or Reference Sensor Ptr based on the mode selected in Tables A.16 / A.17, bit 14-15.
- Bit 0-15: **Reference Follower Mask Link Ptr** - Mode = Reference
  - 0x6E6 (decimal = 1766): Proximity
  - 0x6E8 (decimal = 1768): Touch
- Bit 0-15: **Sensor Mask** - Mode = Follower
  - 0x000 (decimal = 0): None
  - 0x418 (decimal = 1048): Channel 0
  - 0x442 (decimal = 1090): Channel 1
  - 0x46C (decimal = 1132): Channel 2
  - 0x496 (decimal = 1174): Channel 3
  - 0x4C0 (decimal = 1216): Channel 4
  - 0x4EA (decimal = 1258): Channel 5
  - 0x514 (decimal = 1300): Channel 6
  - 0x53E (decimal = 1342): Channel 7
  - 0x568 (decimal = 1384): Channel 8

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- 0x592 (decimal = 1426): Channel 9

Table A.22: Reference Channel Settings 1

Register:	0xA005, 0xA105, 0xA205, 0xA305, 0xA405, 0xA505, 0xA605, 0xA705, 0xA805, 0xA905														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reference Follower Mask/ Reference Sensor Weight															

- Please note that the register value is used for either Follower Mask or Reference Weight based on the mode selected in Tables A.16 / A.17, bit 14-15.
- Bit 0-15: **Reference Follower Mask** (used to enable current sensor as a reference channel for the selected channel) - Mode = Reference
  - 0: Disabled
  - 1: Channel enabled as reference for Channel 0
  - 2: Channel enabled as reference for Channel 1 enabled
  - 4: Channel enabled as reference for Channel 2 enabled
  - 8: Channel enabled as reference for Channel 3 enabled
  - 16: Channel enabled as reference for Channel 4 enabled
  - 32: Channel enabled as reference for Channel 5 enabled
  - 64: Channel enabled as reference for Channel 6 enabled
  - 128: Channel enabled as reference for Channel 7 enabled
  - 256: Channel enabled as reference for Channel 8 enabled
  - 512: Channel enabled as reference for Channel 9 enabled
- Bit 0-15: **Reference Weight** - Mode = Follower
  - 16-bit decimal value/256

Table A.23: Filter Betas

Register:	0xAC00														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Low Power Beta				LTA Normal Power Beta				Counts Low Power Beta				Counts Normal Power Beta			

- Bit 12-15: **LTA Low Power Beta Filter Value**
  - 4-bit value
- Bit 8-11: **LTA Normal Power Beta Filter Value**
  - 4-bit value
- Bit 4-7: **Counts Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Counts Normal Power Beta Filter Value**
  - 4-bit value

Table A.24: Fast Filter Betas

Register:	0xAC01														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

- Bit 4-7: **LTA Low Power Fast Beta Filter Value**
  - 4-bit value
- Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
  - 4-bit value

Table A.25: Slider Setup 0

Register:	0xB000, 0xB100														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Lower Calibration									Static Filter	Slow/Static Beta			Total Channels		

- Bit 8-15: **Lower Calibration**
  - Lower Calibration Value is used to offset the end-points of the slider position so that they match the end-points of the physical slider.
  - 8-bit value
- Bit 6: **Static Filter**

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- If the Static Filter bit is set, the Bottom/Static Beta is used to filter the slider position regardless of the touch's movement speed. This is an IIR filter beta value as described in AZD004.
- 0: Static filter disabled
- 1: Static filter enabled

> Bit 3-5: **Slow/Static Beta**
- If the Static Filter bit is set, the Bottom/Static Beta is used to filter the slider position regardless of the touch's movement speed. This is an IIR filter beta value as described in AZD004.
- 3-bit value

> Bit 0-2: **Total Channels**
- 0010: 2 Channels
- 0011: 3 Channels
- 0100: 4 Channels
- Else: Disabled

Table A.26: Slider Setup 1

Register: 0xB001, 0xB101

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bottom Filter Speed								Upper Calibration							

> Bit 8-15: **Bottom Filter Speed**
- 8-bit value (pixels per conversion)
- Filter value = Bottom/static Beta

> Bit 0-7: **Upper Calibration**
- Upper Calibration Value is used to offset the end-points of the slider position so that they match the end-points of the physical slider.
- 8-bit value

Table A.27: Resolution and Top Speed

Register: 0xB002, 0xB102

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Resolution								Top Speed							

> Bit 8-15: **Resolution**
- 8-bit value * 16 (pixels)

> Bit 0-7: **Top Speed**
- 8-bit value * 4 (pixels per conversion)
- Filter value = no filtering

Table A.28: Slider Enable Mask

Register: 0xB003, 0xB103

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

> Please note that all channels in use must be selected

> Bit 0-9: **Slider Channel Enable Mask**
- If entry is masked, then the touch/proximity event on a specific channel will keep the device in a higher power mode (like during usage) for quick reaction speed. In such case, only when there is no touch/proximity, the device will enter lowest power mode. In some applications like wear detection, unmasked behaviour is best to track long term wear and get best power consumption.
- 0: Disabled
- 1: Channel 0 enabled for slider
- 2: Channel 1 enabled for slider
- 4: Channel 2 enabled for slider
- 8: Channel 3 enabled for slider
- 16: Channel 4 enabled for slider
- 32: Channel 5 enabled for slider
- 64: Channel 6 enabled for slider
- 128: Channel 7 enabled for slider
- 256: Channel 8 enabled as output
- 512: Channel 9 enabled as output

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Table A.29: Enable Status Link

Register:	0xB004, 0xB104														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable Status Link															

- Bit 0-15: **Enable Status Link**
  - 0x6E6 (decimal = 1766): Output linked to channel prox
  - 0x6E8 (decimal = 1768): Output linked to channel touch

Table A.30: Delta Link

Register:	0xB005, 0xB006, 0xB007, 0xB008, 0xB105, 0xB106, 0xB107, 0xB108														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Delta Link															

- Bit 0-15: **Delta Link** - Select element order per channel
- Delta link number corresponds with slider element order
  - 0x000 (decimal = 0): Disabled
  - 0x438 (decimal = 1080): Channel 0 enabled for element
  - 0x462 (decimal = 1122): Channel 1 enabled for element
  - 0x48C (decimal = 1164): Channel 2 enabled for element
  - 0x4B6 (decimal = 1206): Channel 3 enabled for element
  - 0x4E0 (decimal = 1248): Channel 4 enabled for element
  - 0x50A (decimal = 1290): Channel 5 enabled for element
  - 0x534 (decimal = 1332): Channel 6 enabled for element
  - 0x55E (decimal = 1374): Channel 7 enabled for element
  - 0x588 (decimal = 1416): Channel 8 enabled for element
  - 0x5B2 (decimal = 1458): Channel 9 enabled for element

Table A.31: Gesture Setup 0

Register:	0xB009, 0xB109														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Maximum Tap Time								Minimum Tap Time					Flick Gesture Enable	Swipe Gesture Enable	Tap Gesture Enable

- Bit 8-15: **Maximum Tap Time**
  - 8-bit value * 16 (ms)
- Bit 3-7: **Minimum Tap Time**
  - 5-bit value * 16 (ms)
- Bit 2: **Flick Gesture Enable**
  - 0: Flick Disabled
  - 1: Flick Enabled
- Bit 1: **Swipe Gesture Enable**
  - 0: Swipe Disabled
  - 1: Swipe Enabled
- Bit 0: **Tap Gesture Enable**
  - A tap gesture will be reported if the touch lasts longer than the Minimum Tap Time but less than the time specified in the Maximum Tap Time register.
  - 'Minimum Tap Time' <= TAP TIME <= 'Maximum Tap Time'
  - 0: Tap Disabled
  - 1: Tap Enabled

Table A.32: Gesture Setup 1

Register:	0xB00A, 0xB10A														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Minimum Swipe Distance								Maximum Swipe Time							

- Bit 8-15: **Minimum Swipe Distance**
  - 8-bit value * 16 (pixels)

- Bit 0-7: **Maximum Swipe Time**
  - If the touch is released before the time specified in the Maximum Swipe Time register, a flick is reported. Otherwise, a swipe is reported.
  - 8-bit value * 16 (ms)

Table A.33: GPIO0 Enable and Configuration Settings

Register: 0xC000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														Configu-ration	Enable

- Bit 0: **Enable**
  - 0: GPIO0 Output disabled
  - 1: GPIO0 Output Enabled
- Bit 1: **Output Configuration**
  - 0: Push pull active high logic
  - 1: Open Drain active low logic (requires additional pull-up resistance to VDD level, no internal pull-up)

Table A.34: GPIO0 Enable Mask

Register: 0xC001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Channel Enable Mask (Status link = 0x06E6/ 0x06E8)															
Reserved					CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Slider Event Enable Mask (Status link = 0x0620/ 0x063E)															
Reserved													Flick	Swipe	Tap

- Please note that more than one channel can be selected as an output
- Bit 0-7: **Channel Enable Mask** - Status link = Prox/Touch (0x06E6/0x06E8)
  - 0: Disabled
  - 1: Channel 0 enabled as output
  - 2: Channel 1 enabled as output
  - 4: Channel 2 enabled as output
  - 8: Channel 3 enabled as output
  - 16: Channel 4 enabled as output
  - 32: Channel 5 enabled as output
  - 64: Channel 6 enabled as output
  - 128: Channel 7 enabled as output
- Bit 8-9: **Channel Enable Mask** - Status link = Prox/Touch (0x06E6/0x06E8)
  - 256: Channel 8 enabled as output
  - 512: Channel 9 enabled as output
  - 1024: Channel 10/Hall Switch enabled as output
- Bit 0-2: **Slider Event Enable Mask** - Status link = Slider 0/ Slider 1 (0x0620/0x063E)
  - 0: Tap
  - 1: Swipe
  - 2: Flick

Table A.35: Enable Status Link

Register: 0xC002

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable Status Link															

- Bit 0-15: **Enable Status Link**
  - 0x06E6 (decimal = 1766): Output linked to channel prox
  - 0x06E8 (decimal = 1768): Output linked to channel touch
  - 0x0620 (decimal = 1568): Slider 0 event enabled as output
  - 0x063E (decimal = 1598): Slider 1 event enabled as output

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Table A.36: Control Settings

Register: 0xD0

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Interface type		Power mode		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 6-7: **Interface Selection**
  - 00: I^2C streaming
  - 01: I^2C event mode
  - 10: I^2C Stream in touch
- Bit 4-5: **Power Mode Selection**
  - 00: Normal power
  - 01: Low power
  - 10: Ultra-low Power
  - 11: Automatic power mode switching
- Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
- Bit 2: **Execute ATI Command**
  - 0: Do not ATI
  - 1: ATI
- Bit 1: **Soft Reset**
  - 0: Do not reset device
  - 1: Reset device
- Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

Table A.37: Channel ULP Entry Mask

Register: 0xD9

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-9: **Channel ULP Entry Mask**
  - If entry is masked, then the touch/proximity event on a specific channel will keep the device in a higher power mode for quick reaction speed. In such case, only when there is no touch/proximity, the device will enter lowest power mode. In some applications like wear detection, unmasked behaviour is best to track long term wear and get best power consumption.
  - All channels required to enter ULP with an active prox/touch state, must be unmasked.
  - 0: Disabled
  - 1: Channel 0 ULP entry masked
  - 2: Channel 1 ULP entry masked
  - 4: Channel 2 ULP entry masked
  - 8: Channel 3 ULP entry masked
  - 16: Channel 4 ULP entry masked
  - 32: Channel 5 ULP entry masked
  - 64: Channel 6 ULP entry masked
  - 128: Channel 7 ULP entry masked
  - 256: Channel 8 ULP entry masked
  - 512: Channel 9 ULP entry masked
  - 1024: Channel 10/Hall Switch ULP entry masked

Table A.38: Event Enable

Register: 0xDA

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power event	ATI event	Slider 1	Slider 0	Reserved								Touch event	Prox event

- Bit 13: **Power Event**
  - 0: Power event masked
  - 1: Power event enabled
- Bit 12: **ATI Event**

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  - 0: ATI event masked
  - 1: ATI event enabled
- Bit 11: **Slider 1 Event**
  - 0: Slider 1 event masked
  - 1: Slider 1 event enabled
- Bit 10: **Slider 0 Event**
  - 0: Slider 0 event masked
  - 1: Slider 0 event enabled
- Bit 1: **Touch Event**
  - 0: Touch event masked
  - 1: Touch event enabled
- Bit 0: **Prox Event**
  - 0: Prox event masked
  - 1: Prox event enabled

Table A.39: Hall Bias an Offset Current

Register: 0xDB

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Hall Coarse Offset				Hall Fine Offset				Boost Gain	Hall Bias						

- Bit 12-15: **Hall Coarse Offset**
  - Coarse offset current in 3μA steps.
  - Range -21μA to 21μA
- Bit 8-11: **Hall Fine Offset**
  - 4 bit value * 200 (nA)
- Bit 7: **Boost Gain**
  - 0: Boost gain disabled
  - 1: Boost gain enabled
- Bit 0-6: **Hall Bias Current**
  - 7 bit value

Table A.40: I^{2}C Communication

Register: 0xDC

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												Stop received	Start received	RW check disabled	Stop bit disabled

- Bit 3: **Stop Received Flag**
  - 0: No I^{2}C stop received
  - 1: I^{2}C stop received
- Bit 2: **Start Received Flag**
  - 0: No I^{2}C start received
  - 1: I^{2}C start received
- Bit 1: **RW Check Disabled**
  - 0: Write not allowed to read only registers
  - 1: Read and write allowed to read only registers
- Bit 0: **Stop Bit Disabled**
  - 0: I^{2}C communication window terminated by stop bit.
  - 1: I^{2}C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window

Table A.41: I^{2}C Communication Timeout

Register: 0xDD

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I^{2}C Communication Timeout															

- **Note:** I^{2}C To write to this register, the register's address (0xDD) must be commanded explicitly before writing data i.e. in a separate I^{2}C write setup command.
- Bit 0-15: **I^{2}C Communication Timeout**
  - 16-bit value [ms]

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- Range: 0 - 64535
- Default = 500ms

B Revision History

Release	Date	Changes
v0.3	April 2021	Initial release
v1.0	September 2021	Initial release
v1.1	March 2022	Tape and Reel information added Slider events added to Table A.3 Hall boost gain bit definition corrected Firmware version changed to v1.15 Reference schematic updated Bit definition for Read-write check corrected Changed Communication protocol description Read-write permissions added in memory map Stop-bit disable bit definition corrected Revision history added I^2C section extended to include force communication and invalid communication request information Register 0xDD added VREGA electrical characteristics corrected Bit and register names changed to follow user guide and GUI conventions Example of h file from GUI and program flow diagram added Schematic capacitor values corrected
v1.2	August 2022	Add order code QFR and relevant documentation All instances of projected capacitive sensing changed to mutual capacitive sensing
v1.3	September 2022	Updated QFN lead dimensions
v1.4	March 2023	Firmware version updated to v1.18 Added order code 102 Changes implemented for IQS7222A 102 IC option according to "PIN-230172" Updated current consumption tables Updated channel options section Updated addressing information for order code 102 Updated power mode and mode timeout section Update Memory Map version information table Memory Map reserved bits corrected
v1.5	February 2025	Updated Force Communications section Fixed product number in Table A.1

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Release	Date	Changes
v1.6	May 2025	Updated pin names Added Section 6.1.1 describing Ultra-Low Power Mode Added Section 8.1 regarding the Slider UI Added more detailed descriptions of Slider configuration registers in Appendix A Updated supply voltage values in Section 1.1 Added more information in Known Issues Section Style and formatting changes

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C Known Issues

V1.13 and earlier: Polling during start-up may result in device lockup. Suspend polling for at least 25ms after receiving a NACK.

The I^2C initialize can fail if one of the I^2C lines have been kept low for longer than 50ms.

A Tap and Swipe Event is possible at the same time under the following conditions:

- Swipe is made above the minimum swipe distance – then the swipe flag gets set.
- Without lifting off the slider, the swipe is retracted towards the original start position, reducing the total distance moved to less than the minimum swipe distance – the swipe flag remains set from before.
- The slider is then released. If this is all done under the maximum tap time, the tap flag is also set.
- In such case, both a SWIPE and TAP event will be reported.
- Maximum Tap Time may be adapted to limit accidental triggers of both events.

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