IQS7221G DATASHEET

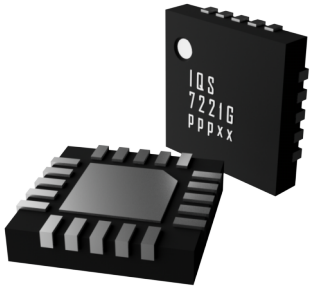
On-Axis Hall-Rotation Sensor With Adjustable Interval UI, Quadrature, Freewheel UI, Two Inductive/Capacitive Channels, and Haptic Interface

1 Device Overview

The IQS7221G ProxFusion® IC is a sensor fusion device for rotation and angle sensing applications using a diametrically-polarised magnet in an on-axis configuration. Two ProxFusion® channels are included for integrated UI applications. The dedicated quadrature outputs make the product a drop-in replacement for mechanical and optical rotary encoders. The IQS7221G includes a virtual freewheel UI for more intuitive scrolling, and a haptic waveform generator to provide haptic feedback with an LRA via a compatible H-bridge.

1.1 Main Features

- Highly Flexible ProxFusion® Device
- Hall-Effect Angle Sensor
  - 4 Hall plates
  - On-axis orientation
  - 16-bit absolute angle output
  - <1° angle error[i]
  - Wide operational range
  - Automatic Tuning Implementation (ATI)
  - Automatic synchronisation with mechanical ratchets
- Two ProxFusion® channels
  - Supports self-capacitance, mutual-capacitance, or inductive sensing
  - Automatic Tuning Implementation (ATI)
  - Button UI to detect large changes
  - Movement UI to detect small/rapid changes
  - Integrates with Hall angle sensor for virtual freewheel UI
- Interval UI
  - Configurable number of intervals per rotation
  - Configurable hysteresis between intervals
- Virtual Freewheel/Hyperscroll UI
  - Integrates the ProxFusion® Movement UI with the Hall sensor to detect “flick” gestures
  - Emulates a freely-spinning wheel – adds hyperscroll functionality to devices without expensive mechanical assemblies
- Haptic Waveform Generator
  - Generate a PWM waveform to drive a Linear Resonant Actuator (LRA) through an H-bridge
  - Automatically trigger a haptic event on interval change or ProxFusion® button activation
- Standalone Mode
  - Quadrature outputs indicate interval change and direction
  - GPIO output to indicate button press on one of the ProxFusion® channels (incompatible with Haptic UI)
- I^2C Interface With IRQ/RDY Signal
- Design Simplicity
  - PC software for configuration and debugging
  - Guidelines for magnet selection and mechanical constraints
- Supply Voltage: 1.8 V to 3.6 V



QFN20 Package

[i] Dependent on magnet alignment and mechanical tolerances

- Small Package
  - QFN20 (3 × 3 × 0.5 mm) – 0.4 mm pitch

1.2 Applications

- Scroll-wheels for computer peripherals
- Mouse wheels
- Applications requiring flexible UI options with sensor fusion
- Mechanical and optical rotary encoder replacements
- Adjustment and control knobs
- Motor encoders

1.3 Block Diagram

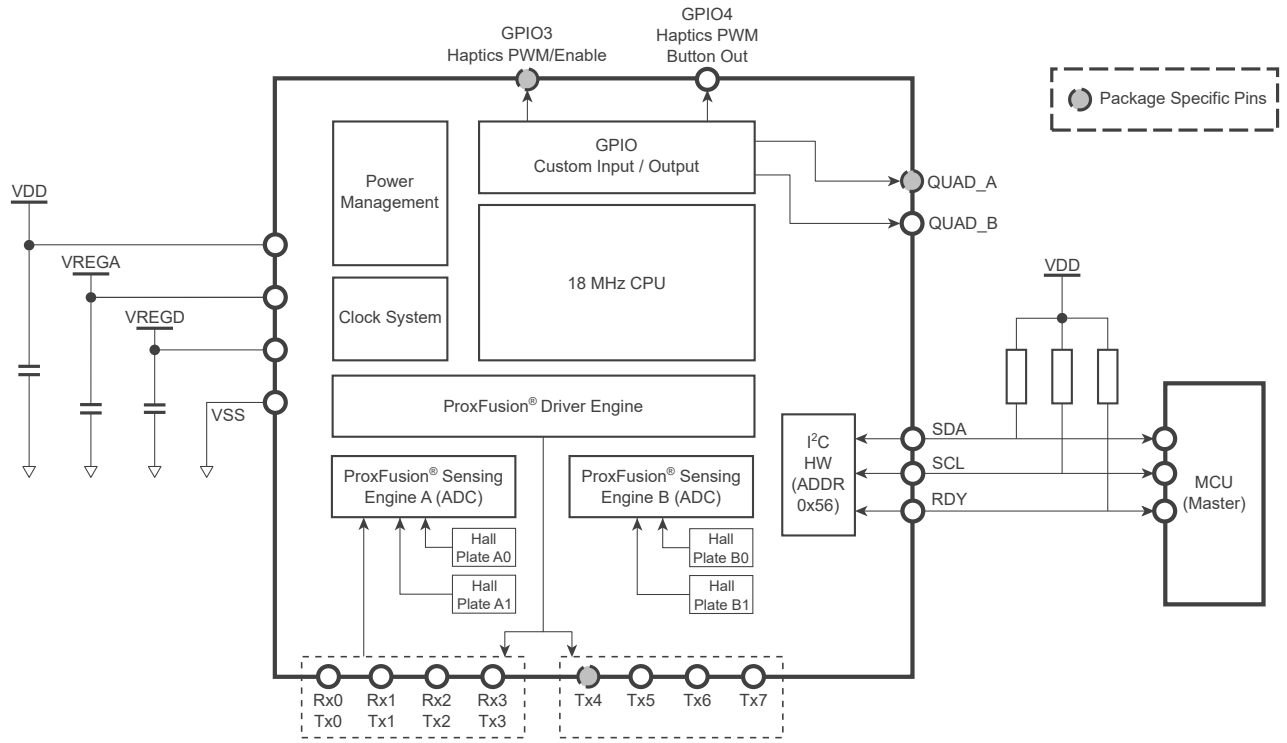


Figure 1.1: IQS7221G Block Diagram

2 Usage Disclaimer

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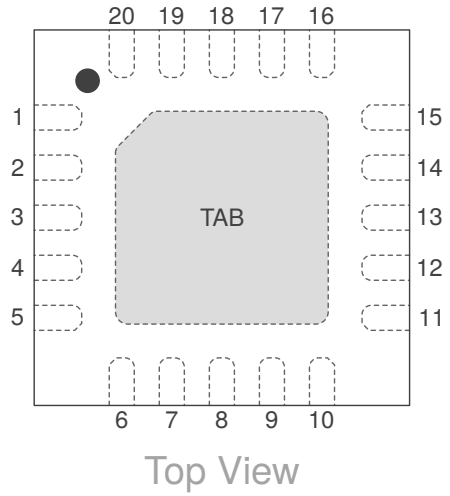
3 Hardware Connections

3.1 QFN20 Pin Diagram

Table 3.1: 20-pin QFN Package (Top View)



Top View

Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	Tx6
2	VREGD	12	Tx7
3	VSS	13	NC
4	VREGA	14	QUAD_A
5	Rx0/Tx0	15	GPIO3
6	Rx1/Tx1	16	GPIO4
7	Rx2/Tx2	17	QUAD_B
8	Rx3/Tx3	18	SCL
9	Tx4	19	SDA
10	Tx5	20	RDY

Area name	Signal name
TAB[i]	Thermal pad (floating)

3.2 Pin Attributes

Table 3.2: Pin Attributes

Pin no. QFN20	Signal name	Signal type	Buffer type	Power source
1	VDD	Power	Power	N/A
2	VREGD	Power	Power	N/A
3	VSS	Power	Power	N/A
4	VREGA	Power	Power	N/A
5	Rx0/Tx0	Analog		VREGA
6	Rx1/Tx1	Analog		VREGA
7	Rx2/Tx2	Analog		VREGA
8	Rx3/Tx3	Analog		VREGA
9	Tx4	Analog		VREGA
10	Tx5	Analog		VREGA
11	Tx6	Analog		VREGA
12	Tx7	Analog		VREGA
13	NC	Analog		VREGA
14	QUAD_A	Digital		VDD
19	SDA	Digital		VDD
18	SCL	Digital		VDD
15	GPIO3	Digital		VDD
16	GPIO4	Digital		VDD
17	QUAD_B	Digital		VDD
20	RDY	Digital		VDD

[i] It is recommended to connect the thermal pad (TAB) to VSS.

3.3 Signal Descriptions

Table 3.3: Signal Descriptions

Function	Signal name	Pin no. QFN20	Pin type[ii]	Description
ProxFusion®	Rx0/Tx0	5	IO	ProxFusion® channel
	Rx1/Tx1	6	IO	
	Rx2/Tx2	7	IO	
	Rx3/Tx3	8	IO	
	Tx4	9	O	
	Tx5	10	O	
	Tx6	11	O	
	Tx7	12	O	
	NC	13	O	NC pad
GPIO	QUAD_A	14	O	Quadrature pin
	GPIO3	15	O	Haptics PWM2/DIR pin
	GPIO4	16	O	Haptic PWM1 or Button output pin
	QUAD_B	17	O	Quadrature pin
	RDY	20	O	RDY pad VPP input for OTP
I^2C	SDA	19	IO	I^2C data
	SCL	18	IO	I^2C clock
Power	VDD	1	P	Power supply input voltage
	VREGD	2	P	Internal regulated supply output for digital domain
	VSS	3	P	Analog/digital ground
	VREGA	4	P	Internal regulated supply output for analog domain

[ii] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

3.4 Reference Schematic

3.4.1 Hall-Rotation Sensing

Minimal example schematic for Hall-rotation sensing and quadrature output.

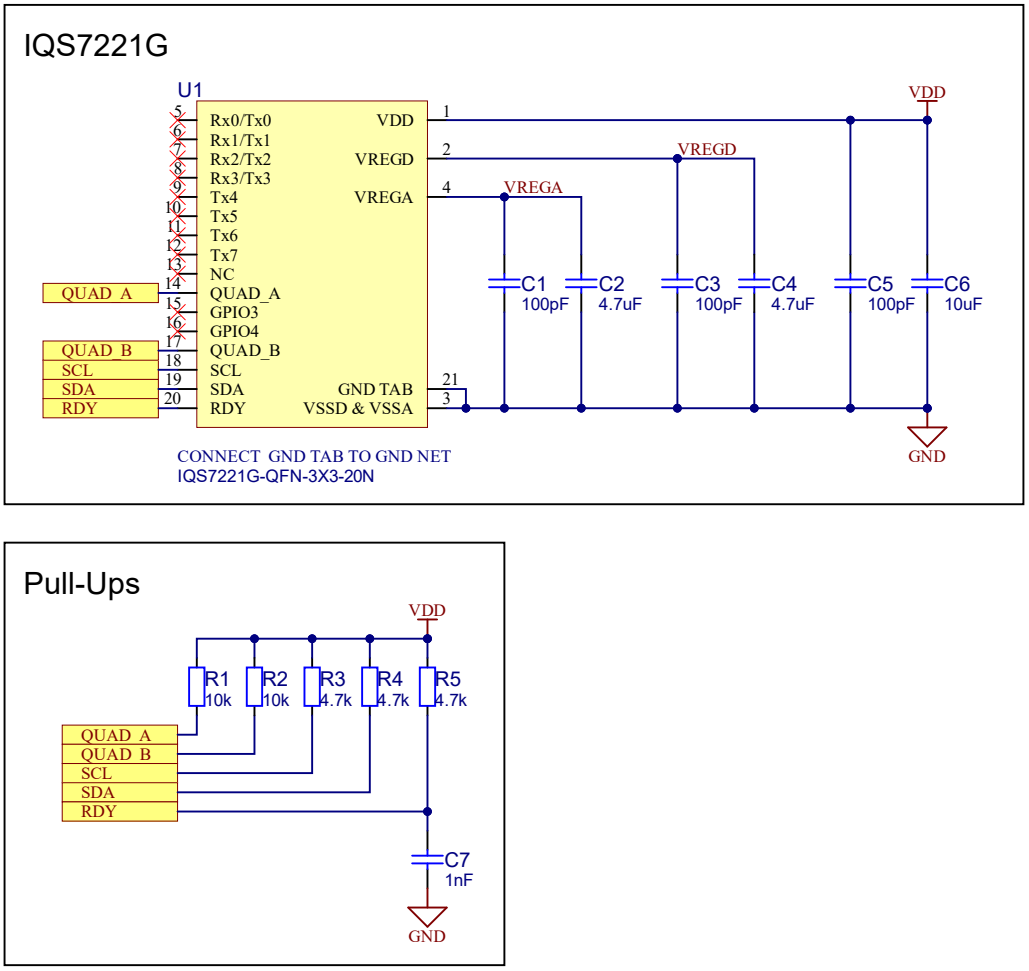


Figure 3.1: IQS7221G Reference Schematic

3.4.2 Hall-Rotation with Self-Capacitance and Inductive Sensing

Example schematic for an application with Hall-rotation sensing, inductive button, and a capacitive wake-up channel. Quadrature pins provide rotation information, and GPIO4 provides the state of the inductive button (open-drain active low).

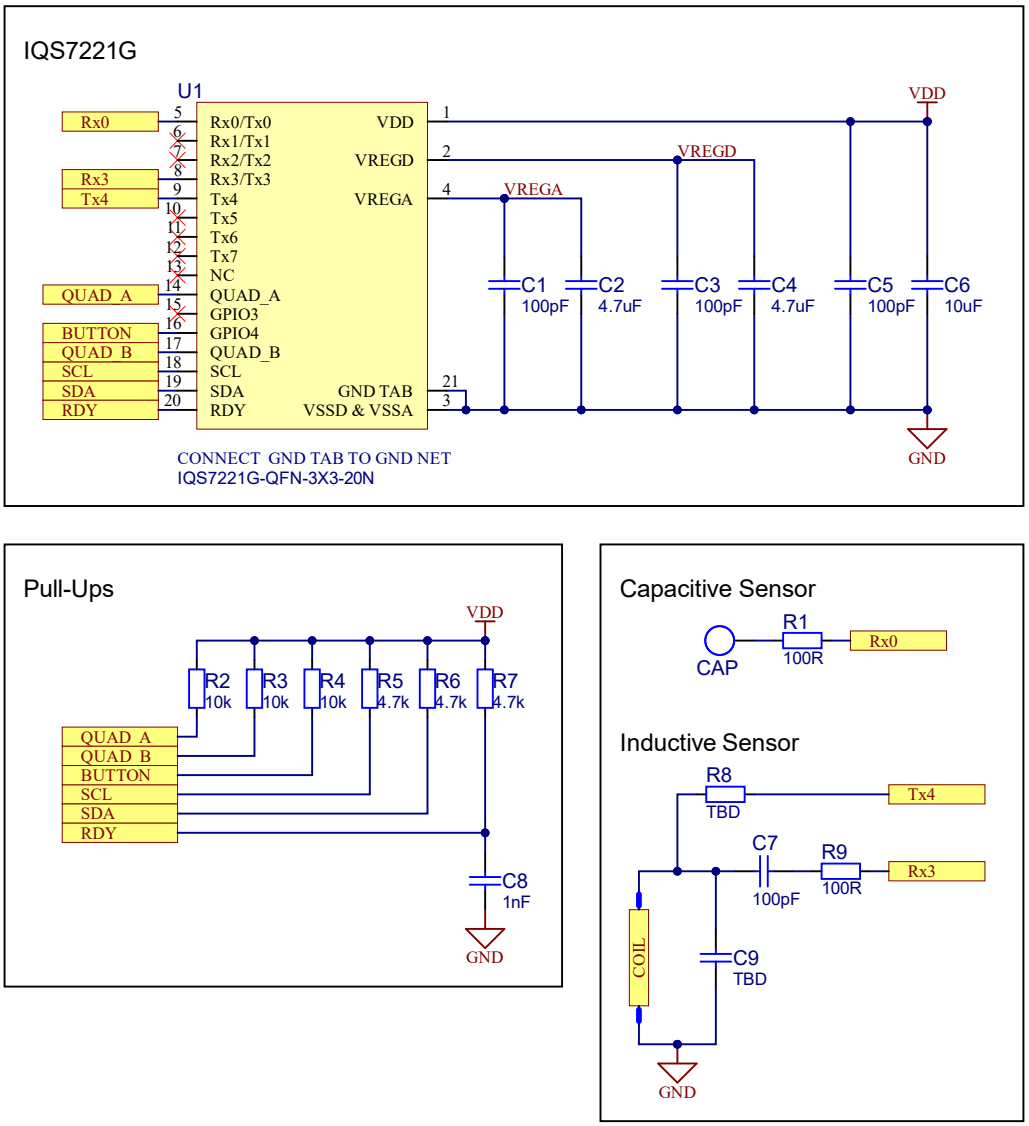


Figure 3.2: IQS7221G Reference Schematic with Self-Capacitive and Inductive Sensing

3.5 Hall Plate Positions

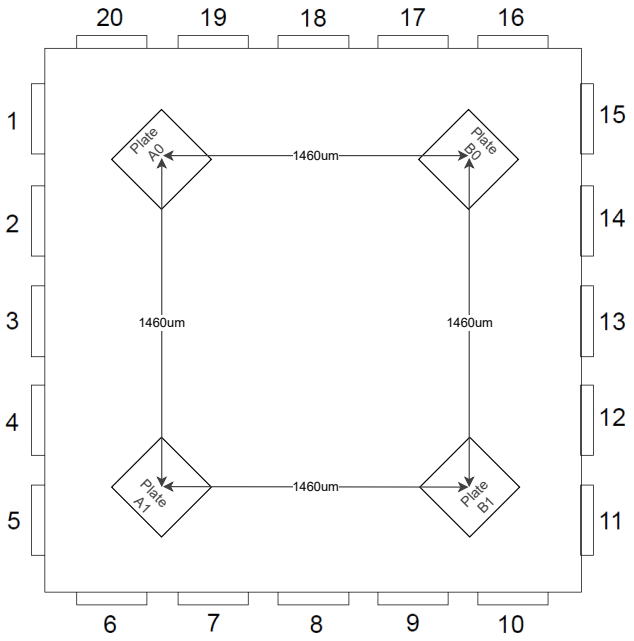


Figure 3.3: Plate Layout QFN (Top View)

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.8	3.6	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	–40	85	°C

4.2 Recommended Operating Conditions

Table 4.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 14 MHz F_{OSC} = 18 MHz	 1.8 2.2		 3.6 3.6	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 14 MHz F_{OSC} = 18 MHz	 1.49 1.7	 1.53 1.75	 1.57 1.79	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 14 MHz F_{OSC} = 18 MHz	 1.56 1.75	 1.59 1.8	 1.64 1.85	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREGA}$	$3\times C_{VREGA}$		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR ≤ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{Tx–Rx}$	Capacitance between receiving and transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{Rx–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, F_{xfer} = 1 MHz Mutual-capacitance mode, F_{xfer} = 4 MHz			 100[ii] 25[ii]	pF
$\frac{Cp_{Rx–VSS}}{Cm_{Tx–Rx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{Rx/Tx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.

4.3 ESD Rating

Table 4.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

[ii] RCx = 0 Ω.
[iii] Please note that the maximum values for Cp and Cm are subject to this ratio.
[iv] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.
[v] Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times F_{xfer})}$ where C is the pin capacitance to VSS.
[vi] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

4.4 Current Consumption

The current consumption of the IQS7221G is highly dependent on the specific parameters configured during initialisation, as well as on the frequency and duration of I^2C communications. Therefore, the following tables serve as an illustration of the expected power consumption for similar configurations[vii]. All measurements are taken with *Event Mode* enabled, without any sensor activations, without any I^2C communications, and with quadrature disabled. As a result, current consumption values shown here may be slightly lower than in practical applications.

All other settings, unless stated otherwise, are kept default.

Current consumption values are provided for both 14 MHz and 18 MHz F_{OSC} configurations. For more information, please refer to Section 11.2.

Table 4.4: IQS7221G Typical Current Consumption at 14 MHz F_{OSC}

Power Mode	Report Rate [ms]	Current Consumption [µA]				
		Hall & Self-Cap	Hall & Inductive	Hall	Self-Cap	Inductive
High-Accuracy	5	460	620	350	230	360
Normal	40	75	98	60	36	55
Low	200	18	22	15	10	13
Ultra-Low	500	6.7	8.5	5.5	3.5	4.9
Halt	3000	1.3				

Table 4.5: IQS7221G Typical Current Consumption at 18 MHz F_{OSC}

Power Mode	Report Rate [ms]	Current Consumption [µA]				
		Hall & Self-Cap	Hall & Inductive	Hall	Self-Cap	Inductive
High-Accuracy	5	530	650	387	233	315
Normal	40	80	97	63	40	53
Low	200	19	22	16	11	13
Ultra-Low	500	7.3	8.6	5.9	4.0	5.0
Halt	3000	1.3				

[vii] These measurements are based on bench testing and have not been characterised over large volumes.

5 Timing and Switching Characteristics

5.1 Reset Levels

Table 5.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

5.2 Miscellaneous Timings

Table 5.2: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
F_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
F_{OSC}	Master CLK frequency tolerance 18 MHz	17.1	18	19.54	MHz
F_{xfer}	Charge transfer frequency (derived from F_{OSC})	42	500 – 1500	4500	kHz

5.3 Digital I/O Characteristics

Table 5.3: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA		0.3	V
V_{OL}	GPIO[i] Output low voltage	I_{sink} = 10 mA		0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2		V
V_{IL}	Input low voltage			VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7		V
C_{b_max}	SDA & SCL maximum bus capacitance			550	pF

5.4 I²C Characteristics

Table 5.4: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

[i] Refers to QUAD_A, GPIO3, GPIO4, and QUAD_B pins.

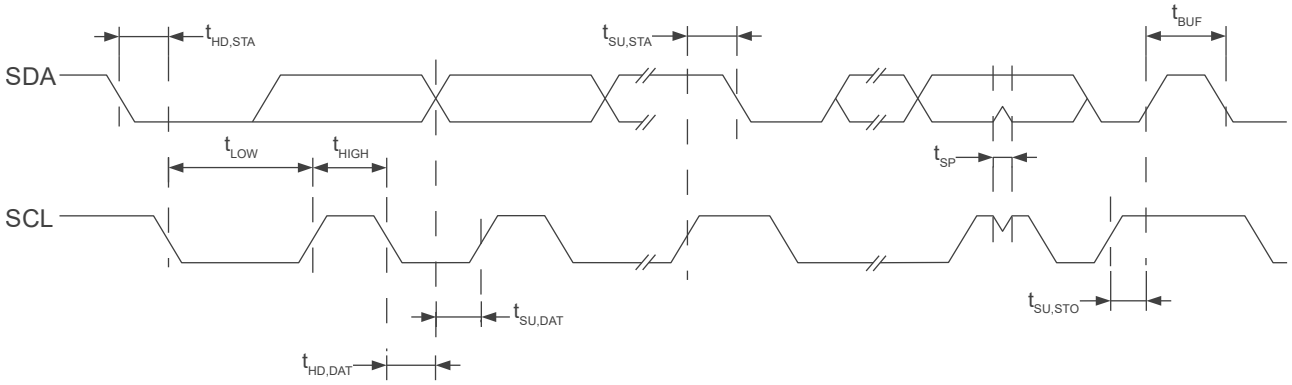


Figure 5.1: I²C Mode Timing Diagram

5.5 Power-On I²C Timing

5.5.1 Power-On Communication Timing with No I²C

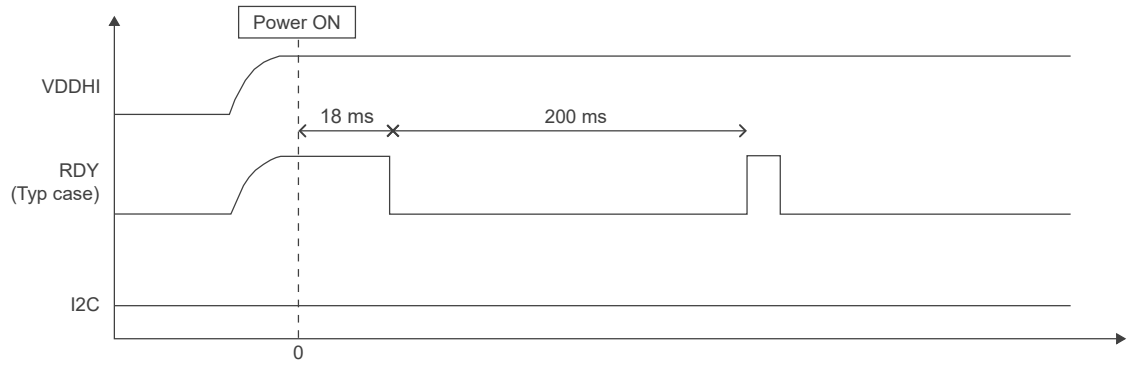


Figure 5.2: Power-On Communications Window Timing With No I²C Initiated

5.5.2 Power-On Communication Timing with I²C

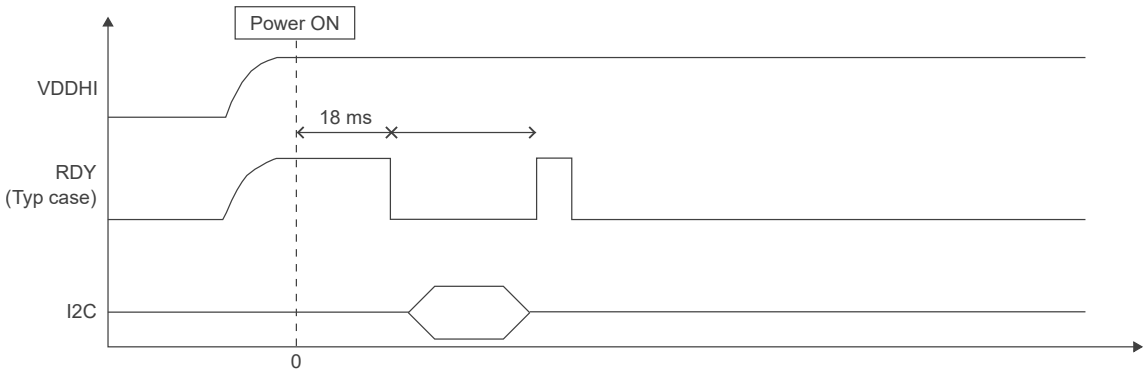


Figure 5.3: Power-On Communications Window Timing With I²C Initiated and Closed

6 ProxFusion® Hall Sensor Module

The IQS7221G contains four equally-spaced Hall plates that measure the magnetic field strength and orientation of a nearby diametrically-polarised magnet. These Hall plates are used to calculate the relative angle of a magnet with regards to the IC, in an on-axis orientation. The angle can be divided into discrete intervals using the Interval UI, providing a convenient interface for scroll wheel applications.

Two ProxFusion® modules allow for simultaneous sampling of two Hall plates at a time, improving the responsiveness of the system. The Hall sensor provides an interval UI to track the current angle of the magnet. The I^2C interface can be used to track the absolute angle of the magnet. The quadrature outputs provide an interface for relative angle tracking in low-power systems and can act as a drop-in replacement for existing digital rotational encoders.

6.1 Magnet Orientation

The IQS7221G is designed to be used in an on-axis orientation with regard to the magnet, as shown in Figure 6.1.

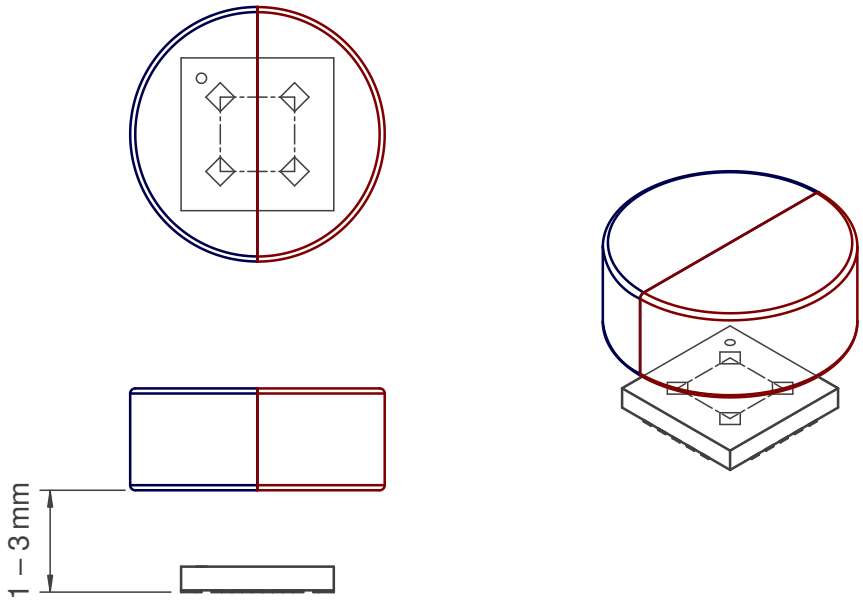


Figure 6.1: Magnet Orientation of an On-axis Angle Measurement Application

Please refer to AZD127 for more information regarding on-axis design guidelines.

6.2 Hall Rotation Measurements

The IQS7221G provides the angle measurement as three different values:

- *Absolute Angle*: Raw angle measurement, provided as an unsigned 16-bit value, where the range [0, 65536) maps to [0°, 360°). This represents the angle of the magnet relative to the IC.
- *Processed Angle*: Angle measurement after post-processing, also an unsigned 16-bit value. This output is filtered and includes an angular offset. This output can be used for applications requiring high-resolution measurements.

- *Interval*: The output of the interval UI, which divides the unsigned 16-bit processed angle into several sections, or intervals. This output is recommended for applications with mechanical ratchets and is supplemented by the hysteresis, auto-zero, and quadrature features.

6.3 Hall Rotation Channels

The Hall-effect rotation measurement on the IQS7221G relies on two measurements on each of the four Hall plates, where the second measurement is inverted to the first. These two measurements allow for the calculation of a reference value and a differential value, from which the relative strength of the magnetic field can be inferred. The reference value is calculated as the average of the two measurements, and the differential value is calculated as the difference between the measurements.

As a result, the IQS7221G performs eight Hall-effect measurements, four of which are inverted to the others. These measurement values (channels) are available in the *Hall Plate Counts* and *Hall Reference* registers.

6.4 Automatic Tuning Implementation (ATI)

ATI is an automatic sensor calibration algorithm that configures the *Hall Plate Offsets* to ensure accurate Hall-effect sensing for a range of different magnet sizes and strengths. The ATI aims to modify the Hall plate settings such that the Hall channel reference values are within the range defined by the *Target* and *ATI Band* parameters. Recommended value for the target is between 8000 and 14000.

The *Hall Gain* value is a constant parameter that must be chosen at design time. This can be done with the aid of the IQS7221G GUI. Typically, the Hall Gain value can be chosen such that the Hall channels swing around ±2000 to ±4000 counts from the reference over a full rotation of the magnet. Once this Gain value is chosen, it can be fixed for all modules across production. The ATI feature will then compensate for any variation across production.

6.4.1 Runtime ATI

ATI is performed automatically at start-up, as well as when all the following criteria are met:

- The Stationary flag is set; see Section 6.8.
- The *Hall Reference* of a channel is outside the threshold defined by Equation (1).

$$|\text{Hall Target} - \text{Hall Reference}| > \text{Hall ATI Band} \quad (1)$$

- Runtime ATI is enabled in *Hall UI Settings*.

6.5 Filtering

The IQS7221G includes a dynamic angle filter that increases its bandwidth based on the magnet's current speed. This allows the filter to remove most of the high-frequency noise while the magnet is stationary, and prevents the filter from aliasing during high-speed rotations. The overall strength of the filter can be adjusted with the *Angle Filter Beta* value in the *Hall Angle Betas* register.

In Low and Ultra Low power modes, the *Low Power Beta* is used instead. This should be set to a *larger* value than the normal beta value, to reduce measured jitter at lower report rates.

6.6 Interval UI

The interval UI divides the 16-bit processed angle into a value between 0 and the *Number of Intervals*, where the size of each interval is defined as:

$$\text{Interval Size} = \frac{2^{16}}{\text{Number of Intervals}}. \tag{2}$$

This is especially useful for applications that do not require a high measurement resolution, or that use mechanical ratchets.

The interval UI is also used for the quadrature UI. On interval change, the IQS7221G will output a quadrature event on the quadrature pins. The device can also open an I²C communications window on interval change if *I²C* is enabled and *Hall Events* are enabled.

6.6.1 Interval Hysteresis

The Interval Hysteresis prevents the interval output from jittering between two intervals, causing unnecessary interval change events. The behaviour of the hysteresis is shown in Figure 6.2.

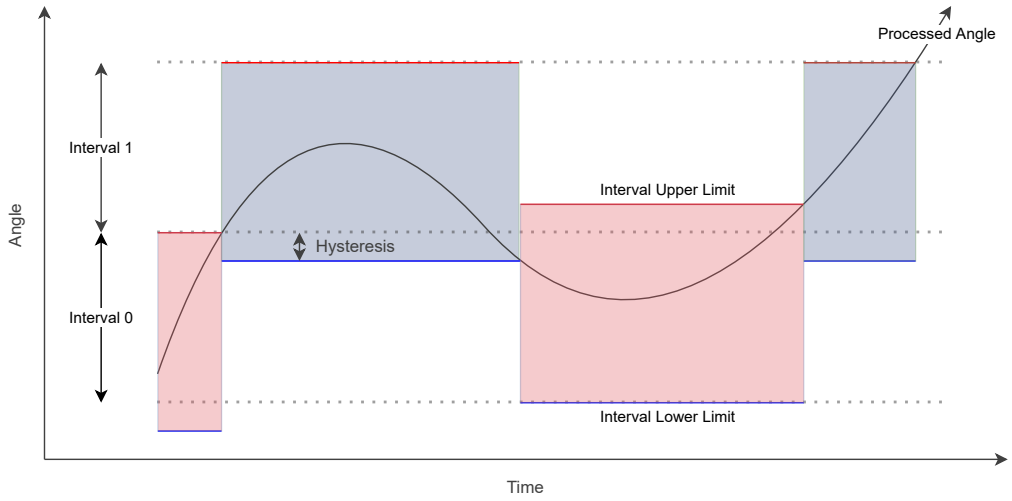


Figure 6.2: Illustration of the Interval Size and Interval Hysteresis

The amount of hysteresis applied can be modified by changing the *Interval Hysteresis* value. Hysteresis is a 16-bit value, in the same unit as the Processed Angle. Hysteresis should therefore be chosen based on the interval size calculated in the previous section, and on the amplitude of the noise on the Processed Angle.

6.7 High-accuracy Mode

The High-Accuracy mode of the IQS7221G will increase the report rate of the device to sample Hall rotation measurements more accurately and to reduce aliasing during high rotation rates.

The IQS7221G will enter High-Accuracy mode in the event of:

- An interval change,
- Freewheeling, if the “Force High-Accuracy” bit is set under the *Hall UI Settings* register.

The *High-Accuracy* flag will remain set for the duration of the *High-Accuracy Timeout*. This flag is used to identify whether to transition into the High-Accuracy power mode, and can be configured to signal an automatic interval centering event when High-Accuracy mode is exited.

6.8 Stationary Detection

The IQS7221G will set a *Stationary* flag if no movement is detected during the period defined by the *Stationary Timeout* value. This Stationary flag is used to identify whether to go into a lower power mode. Runtime ATI for the Hall channels is also only executed when the Stationary flag is set.

6.9 Angle Offset Compensation

Angle offset compensation is applied to ensure the output angle corresponds to the angle of the wheel, rather than the raw angle of the magnet, as shown in Figure 6.3. This is especially important for ratchet applications, where the intervals generated by the IC must match the mechanically-defined intervals of the wheel.

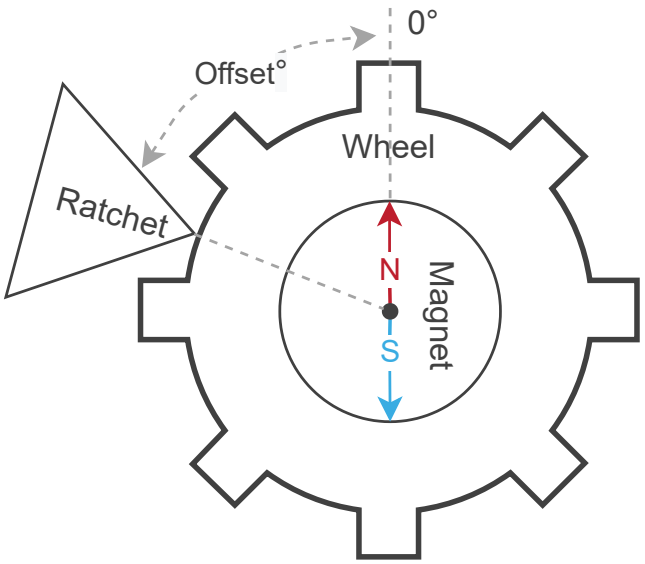


Figure 6.3: Illustration of the Absolute Angle Offset

The angle offset is updated when the *Zero* command in the *System Settings 2* register is set. This sets the Processed Angle to the centre of interval 0, and thus adjusts the angle offset accordingly. The *Zero* command is also set automatically on start-up.

The angle offset is also modified by the automatic interval centering functionality, to align the intervals with a mechanical ratchet automatically.

Finally, the angle offset can be manually changed via the *Angle Offset* register.

6.10 Automatic Interval Centering

The interval centering functionality (or “auto-zero”) of the IQS7221G allows the device to modify the absolute angle offset of the Processed Angle such that the Processed Angle is at the centre of the current interval. This dynamically adjusts the absolute angle offset until the Processed Angle aligns with the physical intervals of a ratchet device.

The auto-zero functionality can be set to one of four different modes in the *Hall UI Settings*:

- **Off**: The device will never allow an automatic interval zero action to happen, and the master device will have to send an instruction over I^2C to set the *Zero* bit.
- **Stationary**: An auto-zero event will occur when the High-Accuracy timeout event occurs. A single adjustment is made to the absolute angle offset each time the device exits High-Accuracy mode. The *Auto-Zero Beta* parameter defines the size of the adjustment, with an auto-zero beta value of 0 resulting in a jump to the exact center of the interval. This behaviour can be seen in Figure 6.4.
- **Continuous**: The auto-zero filter will cause the Processed Angle to move continuously towards the centre of the current interval. It is recommended to use an auto-zero beta value of 10 or higher to allow the Processed Angle to move between intervals during slower rotations. This mode is recommended for devices without a mechanical ratchet. This behaviour can be viewed in Figure 6.5.
- **Release**: An auto-zero event will occur on a Movement Exit event on ProxFusion Channel 0. If Channel 0 is configured as a capacitive touch channel, this exit event could indicate that the user released the device.

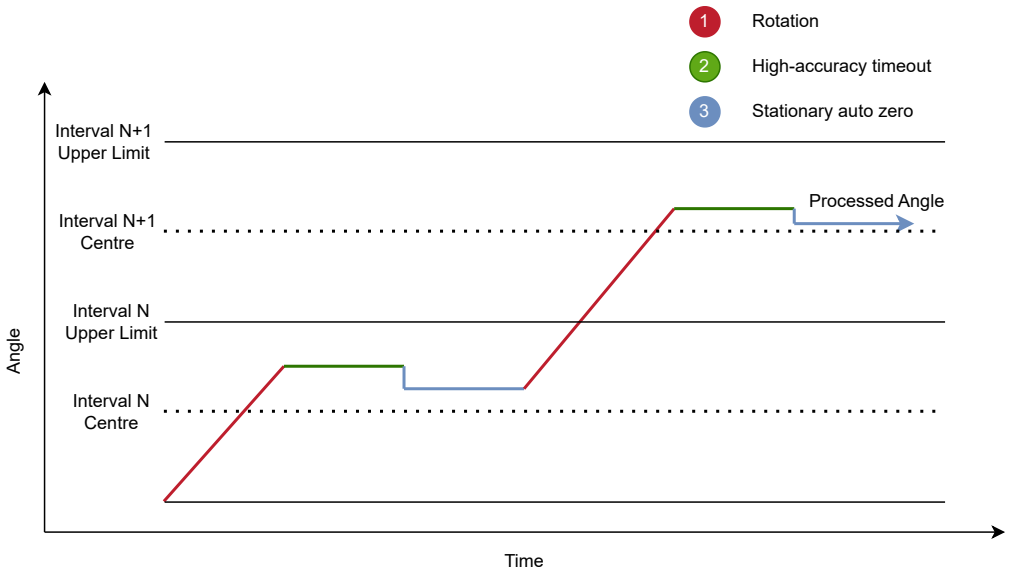


Figure 6.4: Stationary Auto-zero Behaviour

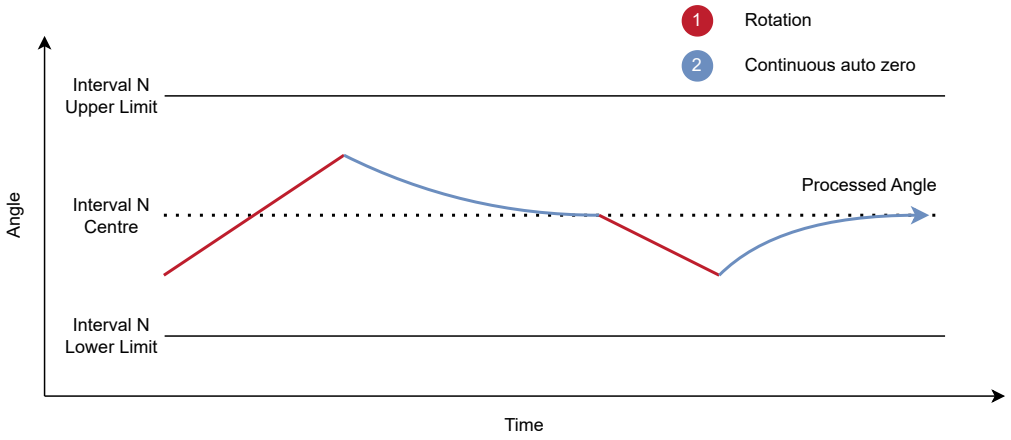


Figure 6.5: Continuous Auto-zero Behaviour

6.11 Quadrature Output

The quadrature output provides feedback over two GPIOs (QUAD_A and QUAD_B) when the value of the current interval changes. This functionality can be used for standalone applications where the master device would not need to poll the current interval value over I^2C but would rather monitor the state of the two quadrature outputs. A visual example of the quadrature output is displayed in Figure 6.6.

A single interval change is represented by a rising or falling edge on both quadrature pins. The direction of the interval change is defined by which pin changes state first. For a positive rotation, the state of QUAD_A changes first, and for a negative rotation, the state of QUAD_B changes first. The period between the change in states of each quadrature output is defined by the *Quadrature Flank Delay* parameter. The quadrature flank delay parameter will also define the maximum report rate of the quadrature output.

The quadrature output pins can be configured as either push-pull or open-drain by setting the *Quadrature Mode* parameter. If open-drain mode is used, pull-up resistors must be added to the quadrature lines as shown in the reference schematic in Section 3.4.1.

Note: The quadrature output can be fed directly into a standard quadrature decoder. Please note that, since some quadrature decoders expect only one GPIO edge per interval (instead of two), they will record twice the number of intervals.

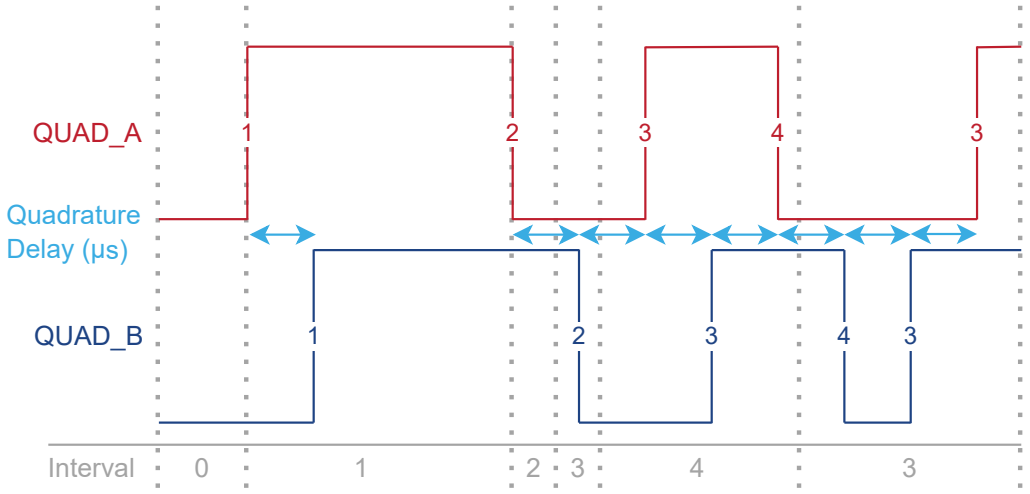


Figure 6.6: Quadrature IO Timing with Respect to Current Interval

Note the rapid change from interval 2 to 4 in Figure 6.6 resulting in a delayed output of the corresponding flanks, so as not to overwhelm the receiving IC.

6.12 Buffered Intervals

During fast rotation, the rate at which intervals are processed may exceed the rate at which quadrature pulses are clocked out. These intervals are buffered in the missed intervals register, and are processed by the quadrature output peripheral at a later time. The buffered intervals can automatically be discarded when the device becomes stationary by setting the *Discard Intervals* bit in the *Hall UI Settings* register.

7 ProxFusion® Channels

The IQS7221G features two ProxFusion® sensing channels that use Azoteq's patented on-chip ProxFusion® modules to measure and process relative changes in capacitive and inductive sensors.

Each channel provides two primary Event types – *Button* and *Movement* events. The Button event attempts to track slow changes and long term activations, whereas the Movement event detects smaller, fast changes. Each of these events store their own reference and delta values.

The Movement event on Channel 0 integrates with the Hall-Rotation UI, providing activation triggers for starting and stopping freewheeling.

7.1 Sensing Modes

Each ProxFusion® channel independently supports the following sensing modes:

- Self-capacitive sensing
- Mutual-capacitive sensing
- Resonated inductive sensing

The sensing mode of each channel can be modified with the CH0 and CH1 *Sensor Settings 1* registers.

Please refer to the following application notes for more information:

- AZD004: Overview of Azoteq's ProxFusion® Sensing
- AZD115: Design Guidelines for Inductive Sensing
- AZD125: Design Guidelines for Capacitive Touch Sensing
- AZD144: Inductive Freewheel and Haptics Design Guide (available upon request)

7.2 Counts

Each ProxFusion® module reports a capacitance or inductance measurement as a relative, unit-less value referred to as "Raw Counts". These raw counts are related to the number of charge transfer cycles necessary to charge an internal sampling capacitor, and are typically inversely proportional to the signal measured on the external sensor.

7.2.1 Counts Linearisation

The IQS7221G does not directly use the "Raw Counts" obtained from the sensing module, but uses "Linearised Counts", which is calculated as

$$\text{Linearised Counts} = \frac{3276750}{\text{Raw Counts}}. \tag{3}$$

All references to "Counts" in this datasheet, and in the I^2C memory map, use these Linearised Counts values.

After linearisation, counts are filtered using a low-pass IIR filter to reduce the high-frequency noise in the measurement. The response of the filter can be adjusted with the *Counts Filter Beta* value in the *CH0 Betas 1* and *CH1 Betas 1* registers. Higher beta values result in a slower filter response, with less noise on the channel.

7.3 Button Event Detection

The Button Event attempts to emulate the behaviour of a typical button, which stays in activation for as long as it is pressed.

7.3.1 Long-Term Average

Button events are detected by comparing the filtered counts value to a reference value, known as the Long-Term Average (LTA). While the channel is not in activation, the LTA is slowly updated to track changes in the environment using a low-pass filter.

The difference between the filtered counts and the LTA is stored as the *Delta* value.

$$\text{Delta} = \text{LTA} - \text{Counts} \tag{4}$$

The delta is used to detect user interaction by comparing it to the *Button Threshold*. The channel enters the active state when the delta exceeds the threshold, and the *Button Active* bit in the *Channel Events* register will be set.

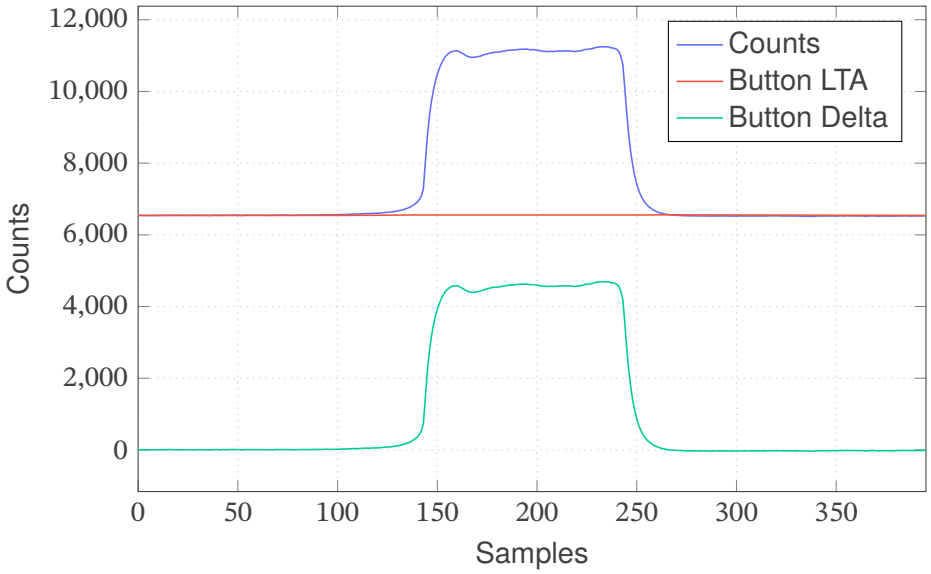


Figure 7.1: Button UI Activation

The LTA is then halted (kept constant) while the Button event is active, or while the delta exceeds the *LTA Halt Threshold*, as shown in Figure 7.1. The LTA Halt Threshold can typically be made smaller than the Button Threshold. This may help increase the sensitivity of the event detection during slower activations, preventing the LTA from drifting during user interaction.

The response of the LTA filter is controlled by the LTA beta values stored in the Channel *Betas 1* and *Betas 2* registers. The *LTA Beta* value sets the response of the filter during High-Accuracy and Normal power modes, whereas the *Low Power LTA Beta* is used during Low and Ultra-Low power modes. The Low Power Beta value should be set to a *larger* value than the Normal Beta value, to maintain adequate sensitivity at lower sampling rates.

7.3.2 Direction

Negative delta values are typically ignored, as they typically indicate an unexpected decrease in signal. If a negative delta value exceeds the *Fast LTA Bound* threshold, the LTA will be updated using the *Fast LTA Beta* filter. This behaviour can be disabled by setting the *Bi-Directional* bit, or the sign of the delta can be inverted by setting the *Inverse* bit in the *Sensor Settings 1* register.

7.3.3 LTA Reseeding

The reseed function of the device will replace the filtered counts and the long-term average value of the channel with the latest sampled counts value to reset the environmental reference of the channel. This may be necessary in certain instances when the Button event gets incorrectly stuck in an activation. Detection of stuck states is controlled by the *Button Timeout* parameter. If the Button event remains active for this timeout duration, the LTA is reseeded automatically. This behaviour can be disabled by setting the timeout parameter to 0.

A *Reseed* command can also be given manually by setting the corresponding bit in *System Settings 2*.

7.4 Movement Event Detection

The Movement Event detects small, rapid changes or movements on the ProxFusion channels. This may be used to trigger freewheeling in Hall-rotation applications, or as a simple wake-up event, triggered as the user approaches the sensor.

7.4.1 Long-Term Average

The movement event tracks its own LTA and delta values, separately from the Button event. In contrast to the Button event, the Movement event does not halt its LTA. Instead, it filters using the regular LTA Beta value while not in activation, and filters with the Fast LTA Beta while the event is active (while the delta is larger than the *Movement Threshold*).

The purpose of this is to track increases in the rate of change of counts. This typically occurs as a user is approaching or releasing a proximity sensor. Outside of activations, the LTA is updated slowly to maximise sensitivity to changes in counts. As soon as the delta exceeds the threshold, the fast LTA is used to exit the movement event as quickly as possible, to be ready to detect the next change in counts. This allows for detection of quick flicks typically performed when attempting to activate freewheeling on scroll wheels. An example of the Movement's response to a flick is shown in Figure 7.2.

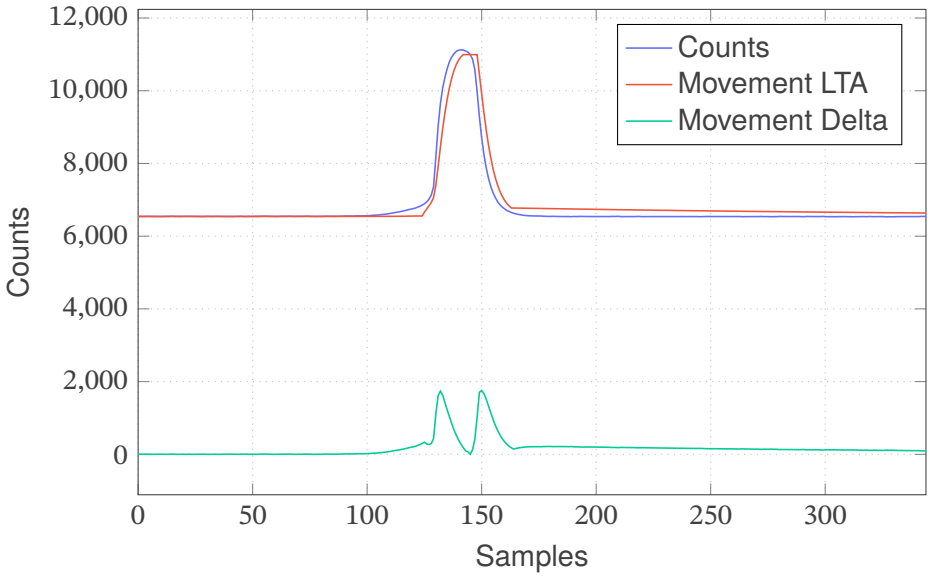


Figure 7.2: Movement UI Activation

7.4.2 Movement Flags

The primary outputs of the Movement Event are the *Movement Entered* and *Movement Exited* flags in the *Channel Events* registers. The Movement Entered flag is set while the delta exceeds the threshold with a positive sign, and indicates that a user approached the sensor, or entered touch. The Movement Exited flag is set while the delta exceeds the threshold with a negative sign, indicating that the user released the sensor. These flags can be flipped by setting the *Inverse* bit.

Note that the Movement event is not affected by the *Bi-Directional* setting.

During slower movements, the same flag may be set multiple times consecutively. For example, an Enter event may occur repeatedly as the user approaches the sensor.

7.5 Dormancy

The touch dormancy flag will be set if the dormancy timeout event occurs after no touch input is received for the period defined in the *Dormancy Timeout* parameter. The IQS7221G is only allowed to enter lower power states once the dormancy flag is set for both channels.

Note that the dormancy timer also acts as a timeout for the LTA Halt flag, if the channel's delta exceeds the LTA Halt Threshold while not in any active state. When dormancy is set, the LTA is reseeded, and will then continue to track environmental changes normally.

7.6 Automatic Tuning Implementation

The ATI is a sophisticated technology implemented in ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode designs, without modification to external components.

The ATI functions by using the *Base* and *Target* parameters to calculate appropriate *Multiplier* and *Compensation* values to achieve an LTA approximately equal to the ATI target value. Note that the base and target values are specified in terms of Linearised Counts, and the base value should always be larger than the target. Typically, a base value of 10000 to 30000 can be used, while a target value between 3500 and 10000 is recommended.

The Coarse Gain parameter in the *ProxFusion Multipliers* registers can be tuned in the GUI. The ATI will then adjust the Fine Multiplier parameter until the counts reach the base value. The Coarse Gain should be manually adjusted at design time until the Fine Divider reaches a value between '4' and '26' after ATI. It can then be fixed across production.

If the ATI algorithm cannot achieve a counts value within the ATI Band, the IQS7221G will set the channel's ATI Error flag.

7.7 Automatic Re-ATI

One of the most important features of the automatic Re-ATI functionality of the IQS7221G is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. It is always recommended to have the automatic Re-ATI functionality enabled. When a Re-ATI is performed on the IQS7221G, the *ATI Event* status bit in the *System Flags* register will be momentarily set to indicate that this has occurred.

An automatic Re-ATI operation is performed when the reference of a channel drifts outside the acceptable range around the ATI Target, which is defined by the *ATI Band* parameter. Automatic Re-ATI is also triggered on ATI Error states.

7.8 Debouncing and Hysteresis

Each of the Button and Movement events provides two mechanisms to prevent jitter: debouncing and hysteresis.

Debouncing occurs when the Button or Movement delta initially crosses the threshold. It forces the IQS7221G to perform a number of quick measurements (at High-Accuracy report rate), checking that all measurements exceed the threshold. The event's *Debouncing* flag is set as long as debouncing is active. Once debouncing is complete, the event's *Active* flag is set.

The number of high-frequency measurements to execute can be configured independently for entering or exiting the event's active state in the *Debounce* register. Setting the debounce values to '0' or '1' will disable debouncing.

Hysteresis allows the channel to use different enter and exit thresholds for an event. Once the event has entered the active state by exceeding the normal threshold value, the exit threshold is calculated as

$$\text{Exit Threshold} = \text{Threshold} \times \left(1 - \frac{\text{Hysteresis Value}}{256}\right) \tag{5}$$

For example, with a Button threshold of 100 counts, and a hysteresis value of 50, the Button event will enter the Active state when the delta exceeds 100 counts, and will exit the Active state when the delta drops down to $100 \times (1 - 50/256) = 80$ counts.

A larger hysteresis value is recommended for the Movement Event, as this allows the delta value to return to 0 more quickly after a movement activation.

7.9 Button GPIO

GPIO4 may be configured to echo the state of the Button Event of either Channel 0 or 1. GPIO4 provides an open-drain active-low signal. As long as the Button Event is active (delta is above the threshold), GPIO4 is pulled low, until the Prox sensor is released or the Button timeout is reached. A pull-up resistor between GPIO4 and VDD is required.

The Button output may be assigned to either Channel 0 or Channel 1 with the *GPIO Button Channel* setting in the *System Settings 1* register. Note that the Button GPIO output is not compatible with the Haptic UI, as the same pin is required for both features.

8 Freewheel UI

The freewheeling UI of the IQS7221G allows the device to continue emulating rotational input when no physical rotation is detected by the Hall-effect sensor. Freewheeling integrates the Hall-rotation sensing and ProxFusion Channel 0 to detect deliberate flicks of a scroll wheel. On a flick, the Freewheel UI measures the rotational speed of the magnet, then continuously increments the Processed Angle at the measured rotational speed, as though the magnet was freely spinning. This speed will eventually decay until the freewheeling event has ended.

A freewheeling event can occur when the freewheeling UI is enabled, and a Movement Exit event occurs while the rotational speed of the physical input is greater than the *Freewheel Start Speed*. Freewheeling continues until the freewheeling speed decays below the value defined in the *Freewheel Stop Speed* parameter.

The movement release delta required to start a freewheeling event is defined by the *Forward Movement Threshold* and *Reverse Movement Threshold* parameters. These parameters are used to set different touch release sensitivity values for freewheeling in different directions.

Freewheeling can be manually stopped during the emulated rotation by triggering a touch event. The *Movement Stop Threshold* parameter will determine the delta of the Movement event required to stop freewheeling.

8.1 Effects of Freewheel Parameters

A simplified equation of the freewheeling angular velocity over time is displayed in Equation (6).

$$\omega_{n+1} = \omega_n - \frac{\text{Friction} + (\text{Damping} \times \omega_n)}{\text{Inertia}}. \tag{6}$$

Figure 8.1 displays the change in angular velocity as the freewheeling friction parameter changes. Freewheeling damping remains constant with a value of 5000, and freewheeling inertia remains constant at 150.

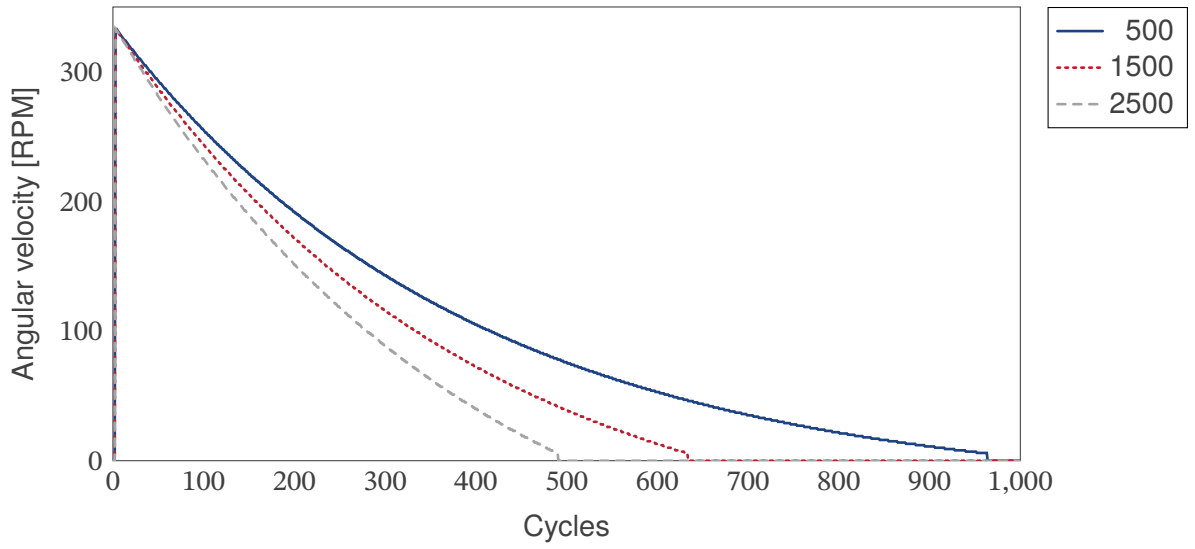


Figure 8.1: Freewheel Response as Friction Changes

Figure 8.2 displays the change in angular velocity as the freewheeling damping parameter changes. Freewheeling friction remains constant with a value of 1000, and freewheeling inertia remains constant at 150.

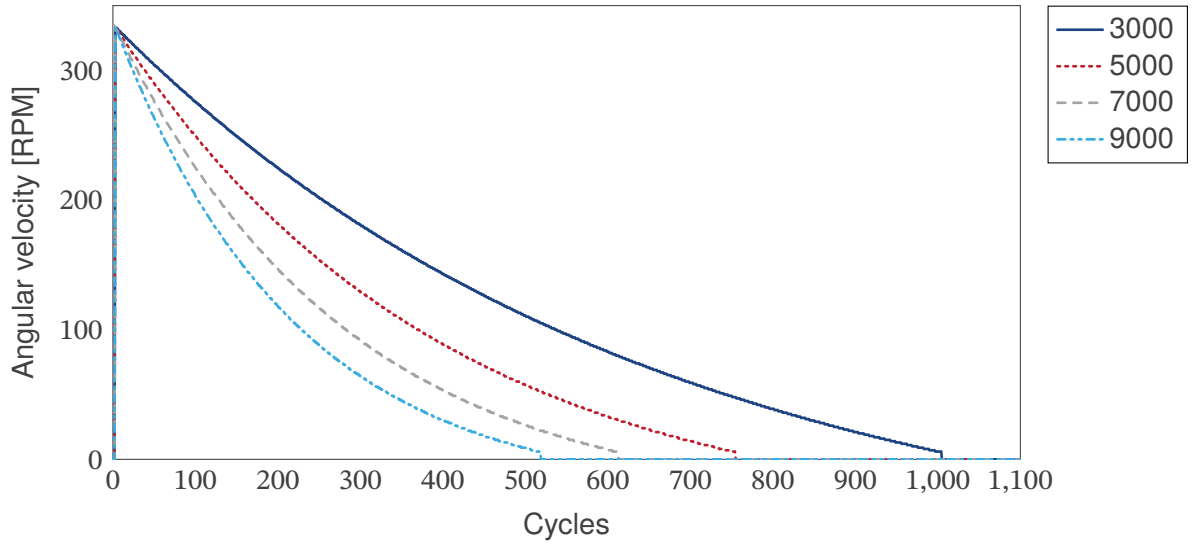


Figure 8.2: Freewheel Response as Damping Changes

Figure 8.3 displays the change in angular velocity as the freewheeling inertia parameter changes. Freewheeling damping remains constant with a value of 5000, and freewheeling friction remains constant at 1000.

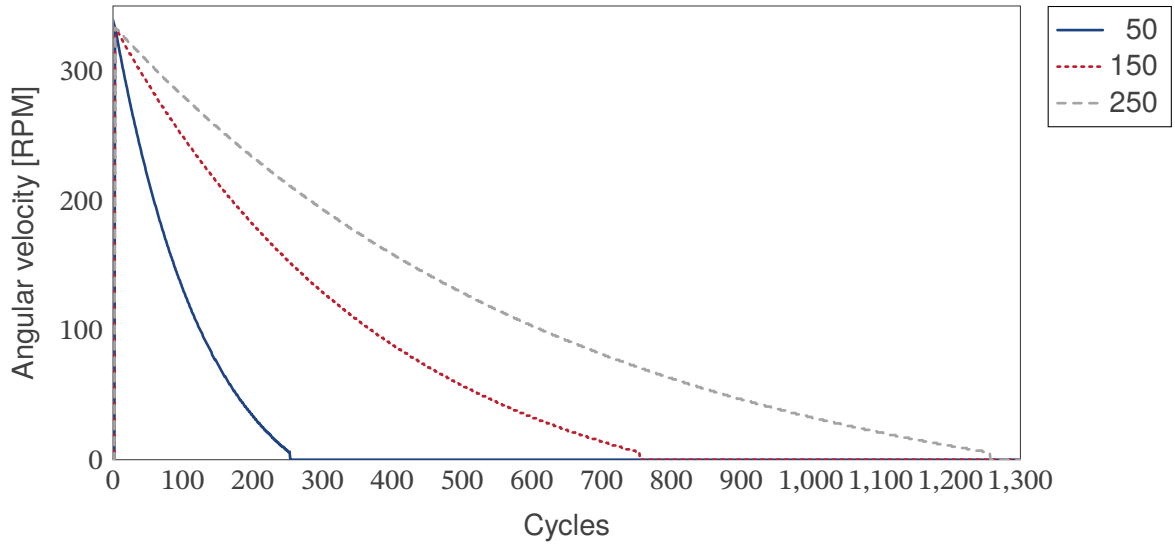


Figure 8.3: Freewheeling Response as Inertia Changes

8.2 Recommended Parameters

The freewheeling settings on the device all default to 0. The Table 8.1 provides recommended parameters to use as a starting point:

Table 8.1: Freewheeling Recommended Settings

Parameter	Value
Decay Beta	4
Follow Beta	2
Freewheel Friction	20
Freewheel Damping	5000
Freewheel Inertia	180
Freewheel Minimum Start Speed	40
Freewheel Stop Speed	20
CH0 Movement Stop Threshold	200
CH0 Movement Forward Threshold	200
CH0 Movement Reverse Threshold	200
Hall Movement Stop Threshold	2500
Stationary Detect Speed	40

9 Haptic UI

The IQS7221G provides two GPIOs to interact with an external H-Bridge device to drive a linear resonant actuator (LRA) and provide haptic feedback on specific events. This allows the IQS7221G to create its own haptic clicks on rotation events or ProxFusion button events, emulating the sensation of either a rotational ratchet or button click. This feature is aimed at supporting wide-band LRAs that do not require auto-resonance (resonant frequency tracking).

9.1 Supported H-Bridge Devices

The IQS7221G primarily supports two interfaces to control external LRA drivers: PWM1/PWM2 and PWM/DIR. Table 9.1 provides the pin mapping of the two interfaces.

Table 9.1: Haptics Pin Mapping

Pin	PWM1/PWM2	PWM/DIR
GPIO3	PWM2	DIR
GPIO4	PWM1	PWM

The H-bridge interface mode can be selected by modifying the *Driver Interface* bit of the *Haptic Global Settings* register.

9.1.1 PWM1/PWM2

The PWM1/PWM2 mode provides two PWM signals, where one drives the motor in a forward direction, and the other in the reverse direction. This mode may be referred to as “IN1/IN2” by some manufacturers. These PWM signals run at a carrier frequency of 20 kHz. To create the triangular waveform to drive the LRA, the PWM duty cycle is modulated linearly from 0% to 100%, at the LRA resonant frequency. The positive half-cycle of the triangular waveform is generated on PWM1, while the negative half-cycle is output on PWM2. This is shown in Figure 9.1.

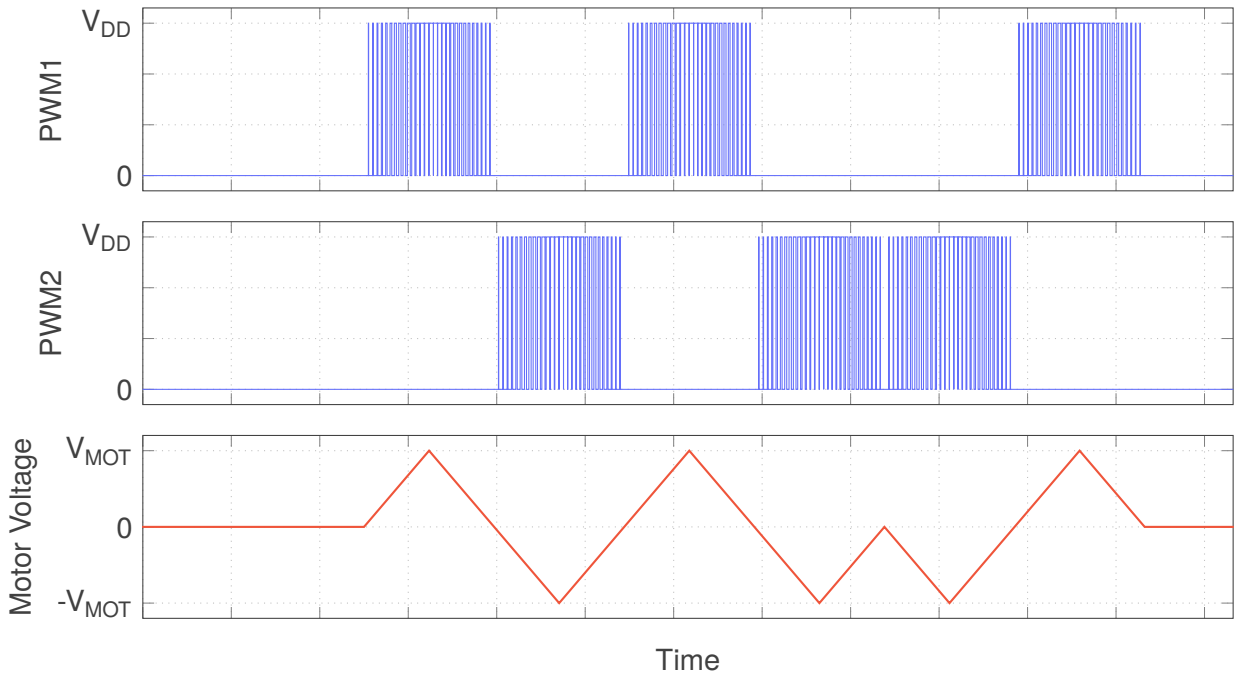


Figure 9.1: PWM1/PWM2 Interface Signals

This interface may be used with certain monolithic H-bridge integrated circuits that only require two PWM inputs. Alternatively, an H-bridge circuit may be created using discrete components. Figure 9.2 provides a reference schematic for such an LRA driver circuit. Resistor sizing and design will be required to take into account the transient effects of the gate capacitance of the selected transistors.

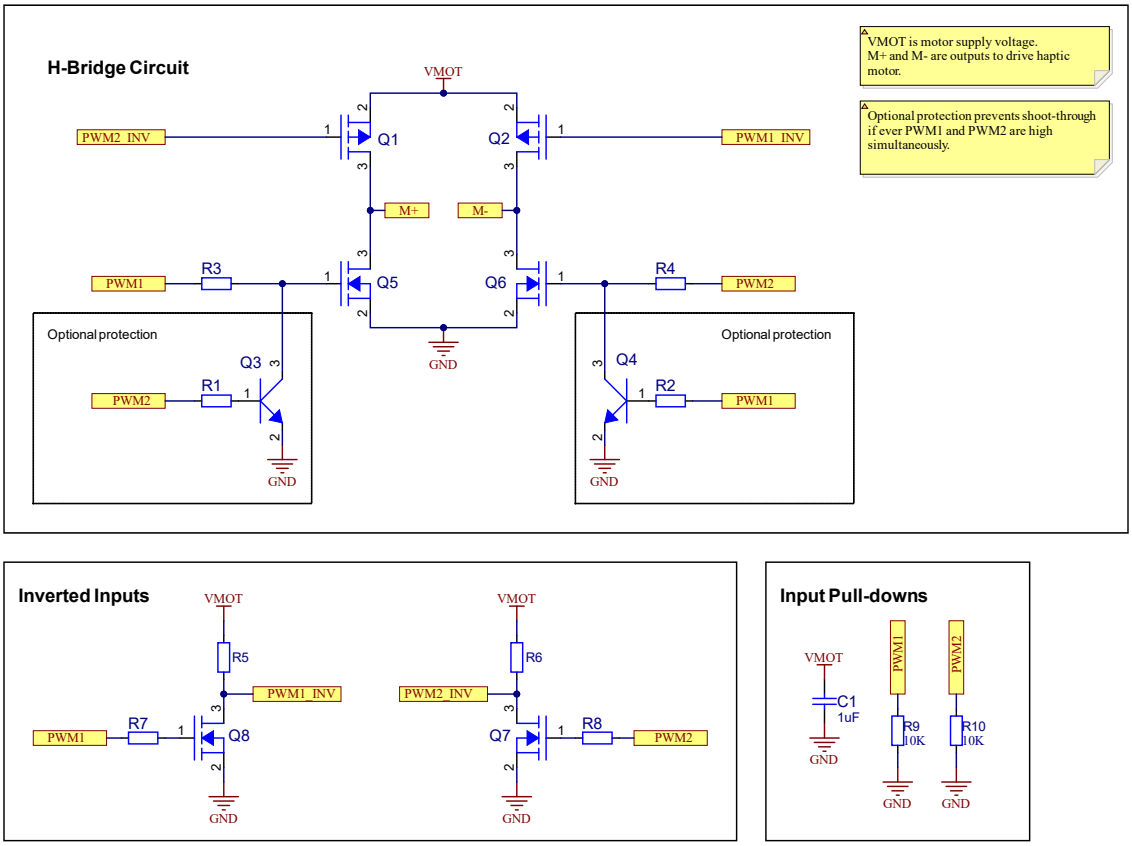


Figure 9.2: Example H-Bridge with Two PWM Inputs

The above circuit may be susceptible to shoot-through if the PWM1 and PWM2 signals are both high simultaneously. Two BJTs are used to ensure that all four H-bridge transistors may never be active simultaneously. Note that this circuit will not provide short-circuit protection on the M+ and M- outputs, nor does it provide any over-temperature protection.

9.1.2 PWM/DIR

The PWM/DIR provides a PWM and Direction signal. Similar to the PWM1/PWM2 interface, the IQS7221G drives the LRA with a 20 kHz PWM signal, with a triangular waveform modulated at the LRA resonant frequency. However, the PWM pin now controls the absolute amplitude of the haptic drive signal, while the Direction pin alternates with each half-cycle to set the sign of the signal. This is shown in Figure 9.3.

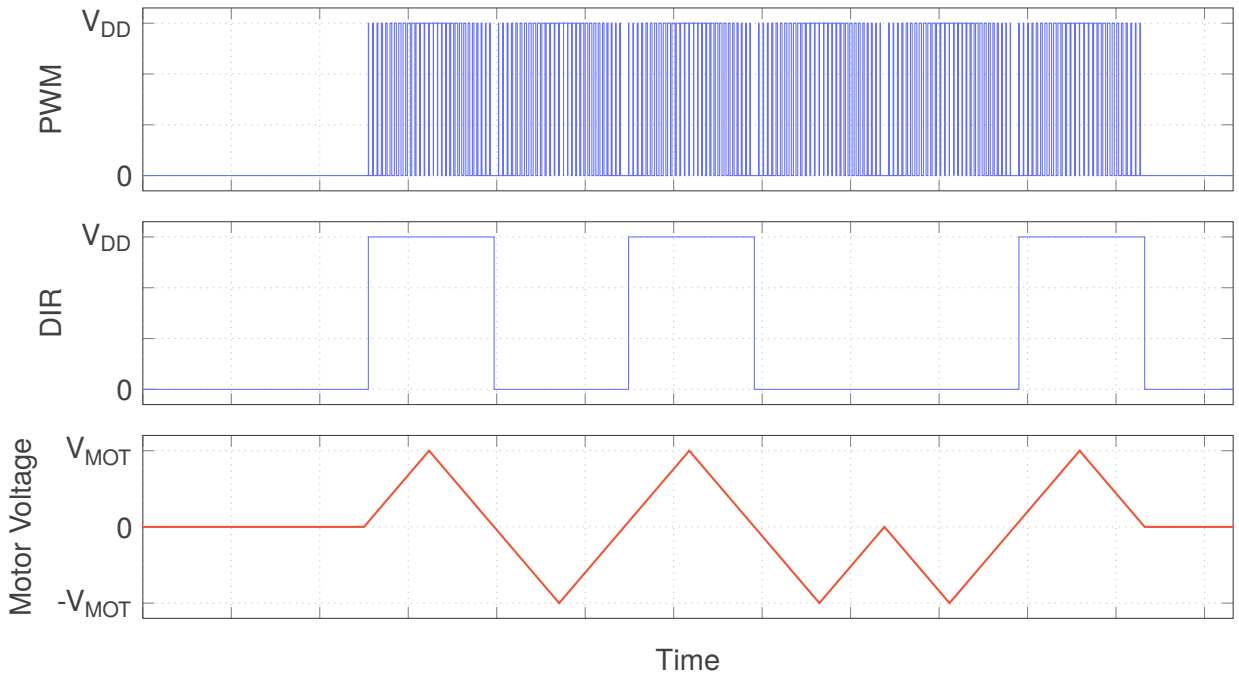


Figure 9.3: PWM/DIR Interface Signals

This interface is primarily aimed at supporting the IQS390 haptic driver. Figure 9.4 shows the recommended schematic for an IQS390-based haptic circuit.

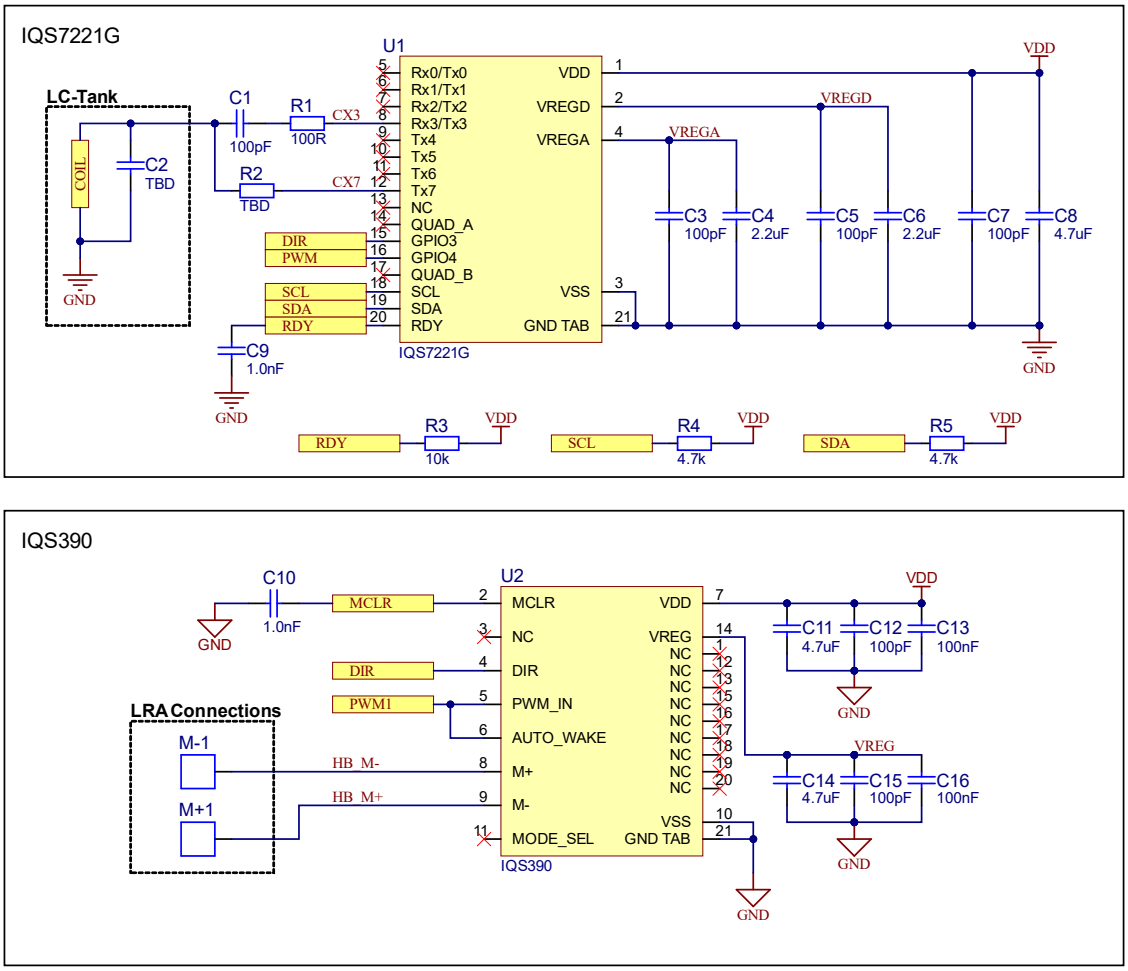


Figure 9.4: IQS7221G Reference Schematic with IQS390 Haptic Driver

This mode may be compatible with other devices that offer a “PWM/DIR” interface or “Phase/Enable” interface. Please contact Azoteq for more information regarding compatibility with such devices.

9.2 Enabling Haptics

Haptics is disabled by default. Haptics can be enabled by setting the global *Haptics Enable* bit in the *System Settings 1* register.

9.3 LRA Frequency

The resonant frequency of the LRA can be set in the *LRA Frequency* register. The frequency is specified in hertz. Typical values for LRAs range between 160 Hz and 350 Hz.

9.4 Haptic Triggers

Haptics can be triggered on an interval change, on the ProxFusion Button Enter and Exit events, or on request over I^2C.

10 Power Options

The IQS7221G offers 5 power modes:

- **High-Accuracy (HA)**
  - Highest current consumption.
  - High-accuracy mode is always entered during Channel 0 or Channel 1 debouncing.
  - When in automatic power mode, high-accuracy mode is entered when:
    - The *Interval* value has changed.
    - A freewheeling event occurs with the *Force High-Accuracy Freewheeling* option enabled in *Hall UI Settings*.
- **Normal Power Mode (NP)**
  - The default operating power mode.
  - When in automatic power mode, normal power mode is entered when:
    - Exiting high-accuracy mode after the high-accuracy timeout.
    - Button UI event occurs.
    - Movement UI event occurs.
- **Low Power Mode (LP)**
  - Typically configured with a slower report rate to reduce current consumption.
  - When in automatic power mode, low power mode is entered when all the following conditions are met:
    - Hall stationary flag is set.
    - CH0 and CH1 dormancy flags are set.
- **Ultra-Low Power Mode (ULP)**
  - Recommended being configured for the slowest report rate.
  - Sampling on Channel 0, Channel 1, and Hall can be individually enabled or disabled from the *System Settings 1* register.
  - The device will not enter ULP if there are missed intervals that need to be processed.
  - The device will enter ULP mode if the *ULP timeout event* occurs. The ULP timer is started when the device enters LP mode.
- **Halt Mode**
  - Is entered and exited by an I^2C command, by setting or clearing the *Halt* bit.
  - Places device in standby mode.
  - Periodically wakes at the ULP report rate. Set the report rate to maximum (3 seconds) to minimise current consumption.
  - No analog sampling events occur during halt mode.
  - To exit halt mode the master device must open a forced communications window and clear the *Halt* bit.

Figure 10.1 shows a block diagram of the automatic power mode switching.

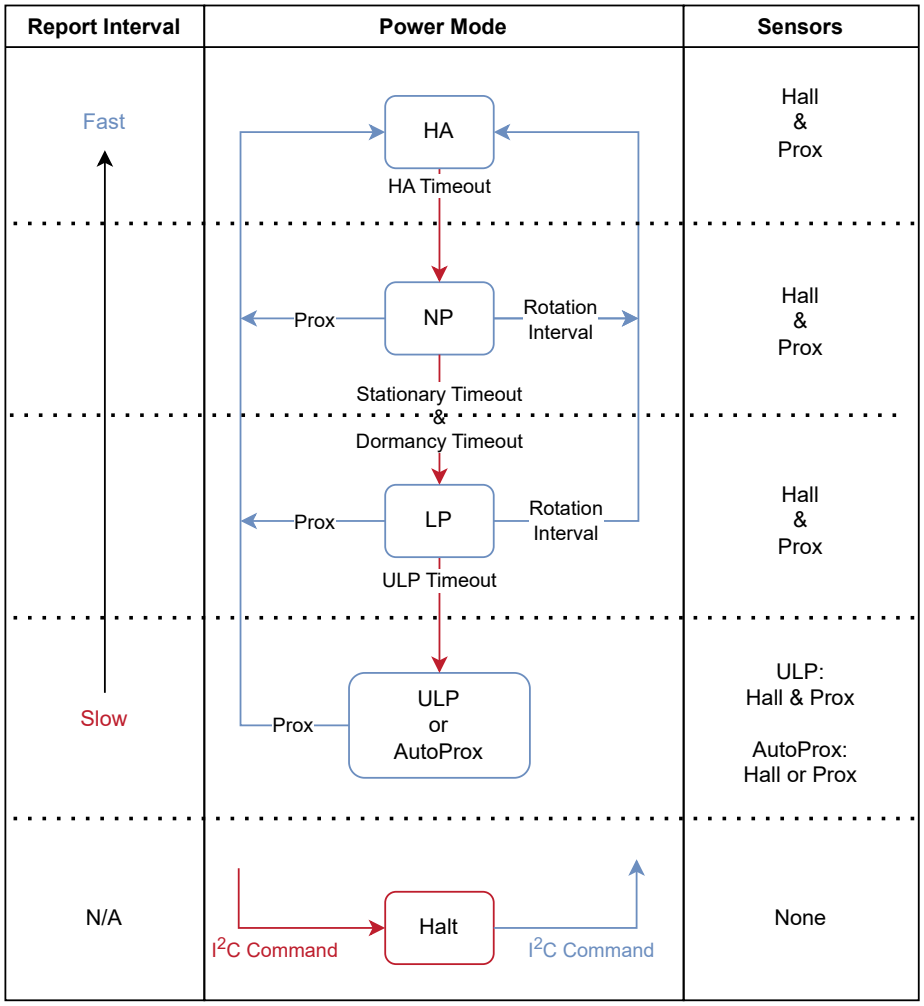


Figure 10.1: Power Modes

11 Additional Features

11.1 Debug and Display Software (GUI)

The Azoteq IQS7221G GUI can be utilised to configure the optimal settings required for a specific hardware setup or application. The device performance can be easily monitored and evaluated in the graphical environment until the optimal device configuration is obtained.

Once the IQS7221G is configured in the GUI as desired, a C header file (*.h* file) can be exported that stores the values of all the read-write registers of the IQS7221G. The *.h* file displays the start address of each block of data, with each address containing two bytes in little endian order. An example of the *.h* file exported by the GUI is shown below.

```
/* Global Device Settings */
/* Memory Map Position 0x60 - 0x6D */
#define SYSTEM_SETTINGS                    0x01 // Least-significant byte
#define POWER_SETTINGS                     0x70 // Most-significant byte
...
```

11.2 Main Oscillator

The main oscillator frequency can be configured for 14 MHz or 18 MHz. This is configured in the *System Settings 1* register. The lower-frequency configuration reduces the requirements on VDD, as shown in Section 4.2.

The higher-frequency configuration allows for larger amplification of the Hall plate signals, reducing noise in situations with low magnetic fields. This can be achieved by setting the *Hall Plate Bias* register to a higher value. The following table provides recommended values:

Table 11.1: Recommended Hall Bias Values for Different F_{OSC} Values

F_{OSC} [MHz]	Hall Bias Value
14	52
18	67

11.3 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability. The watchdog timer is reset at the start of the main loop before any measurements take place. If the timer expires, the device is reset, performing a soft reboot. The *Watchdog Period* register determines the period of the timer in milliseconds before the device will reset.

Note: Ensure that the watchdog timeout period is greater than the I^2C timeout period.

11.4 Reset

11.4.1 Reset Indication

After a reset, the *Show Reset* bit in the *System Flags* register will be set by the system to indicate that the reset event occurred. This device reset bit will clear when the master sets the *Ack Reset* bit in the *System Settings 2* register. If the Show Reset bit becomes set again, the master will know a reset has occurred and can react appropriately.

11.4.2 Software Reset

The IQS7221G can be reset by means of an I²C command, by setting the *Soft Reset* bit in the *System Settings 2* register.

12 I²C Interface

12.1 I²C Module Specification

The device features a standard two-wire I²C interface, complemented by a RDY (ready interrupt) line, supporting a maximum bit rate of up to 1 Mbit/s. The IQS7221G implements 8-bit addressing with 2 data bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes, stored at each address in little-endian order, will be referred to as “byte 0” (least significant byte) and “byte 1” (most significant byte).

- Standard two-wire interface with RDY interrupt line
- *Fast-Mode Plus* I²C with up to 1 Mbit/s bit rate
- 7-bit device address
- 8-bit register addressing
- Two data bytes stored per register address, in little-endian order

12.2 I²C Address

The IQS7221G has a default I²C address of 0x50 (0b1010000). The full address byte will thus be 0xA0 (write) or 0xA1 (read).

12.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

12.4 I²C Starting Behaviour

The device will default to streaming mode as long as *Show Reset* bit is set in the *System Flags* register. For the device to enter either Event mode or Standalone Mode, the Show Reset bit needs to be cleared by setting the *Acknowledge Reset* bit in the *System Settings 2* .

12.5 Memory Map Data

Data is stored in 16-bit words, meaning that each address contains two bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11. The 16-bit data is sent in little endian byte order (least significant byte first).

12.6 RDY/IRQ

The IQS7221G has an open-drain active low RDY signal to inform the master that updated data is available. The IQS7221G will pull the RDY line low to indicate that it has opened a communications window, or “RDY window”, for the master to read the new updated data. While the master can communicate with the device at any time according to the *Force Comms Method*, it is recommended to use the RDY signal for optimal power consumption. Integrating the RDY signal as an interrupt input allows the master MCU to read and write data efficiently.

The device provides three communication modes:

- Streaming Mode
- Event Mode
- Standalone Mode

In streaming mode, the RDY line toggles continuously, with each sensing cycle, whereas in event mode the RDY toggles only when specific events occurs. The types of events that trigger the RDY window are configurable in the *Event Mask* register. Standalone mode never toggles the RDY pin, and never opens a communications window (unless the Force Comms command is given, as described in Section 12.11.2). The master must rely on the quadrature and Button outputs.

12.7 Read and Write Operations

12.7.1 I²C Read From Specific Address

A typical read operation is displayed in Figure 12.1. The master device waits for the RDY line of the IQS7221G to go low, indicating the availability of new data and an available communication window. Once the RDY interrupt is triggered, the master initiates communication by sending a start condition followed by the device address and a write command. The IQS7221G responds with an acknowledgement, after which the master device will transmit one byte defining the register address. The master then sends a repeated start condition, followed by the device address with a read command. The IQS7221G transmits data from the requested address and will continue to do so while the master acknowledges each byte. The read operation is ended when the master does not acknowledge the last byte received and produces a stop condition.

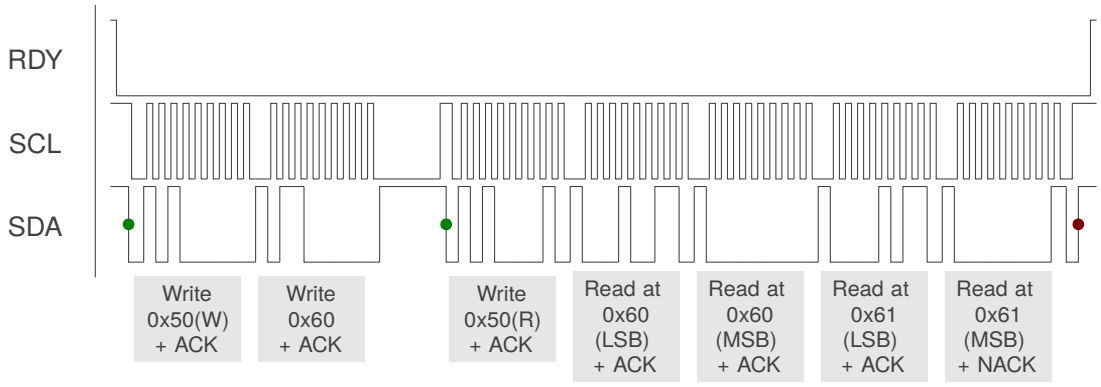


Figure 12.1: I²C Read Example — Read Status Registers 0x10 and 0x11

12.7.2 I²C Write To Specific Address

The write operation is displayed in Figure 12.2. Similar to the read transaction, when the RDY interrupt is triggered, the master initiates communication by sending a start condition followed by the device address and a write command. The IQS7221G responds with an acknowledgement, after which the master device transmits one byte defining the register address. The slave acknowledges the register address byte. The master may then write a series of bytes to the register address and the addresses that follow, with each byte being acknowledged by the slave. The write operation is ended when the master produces a stop condition.

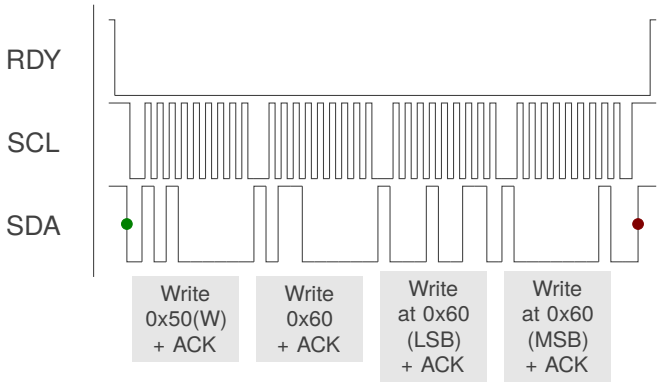


Figure 12.2: I²C Write Example — Write Two Bytes to System Settings 1 Register 0x60

12.7.3 Modifying Bits Over I²C

When modifying individual bits in a register, it is recommended to read the register first, make the necessary modifications, and then write the updated value back to the IQS7221G register to prevent unintentional bit changes.

For example, setting the *I²C Enable* bit and *Power Mode* setting would involve:

- Read the *System Settings 1* Register (0x60) as illustrated in Figure 12.1.
- Set the *I²C Enable* bit using the bitwise OR operator. For example:

  READ_VALUE OR 0x0001

- Set the *Power Mode* setting by clearing the bit field using a bitwise AND operation, then setting the bit field value with an OR operation. For example, to set the *Power Mode* to 'Normal':

  (READ_VALUE AND 0xFCFF) OR 0x0100

- Write the new values back over I²C, as shown in Figure 12.2.

Read-modify-write transactions should be done in a single communication window, using I²C restart conditions. Please refer to Section 12.9 for more information regarding multiple I²C transactions in a single communication window.

12.8 I²C Timeout

If the communication window is not serviced within the *I²C Timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be lost, so this should be avoided. The default I²C timeout period is set to 200 ms.

12.9 Terminate Communication

With the *Stop End Comms Disable* setting disabled in the *System Settings 2* register, a standard I²C STOP ends the current communication window. If multiple I²C transactions need to be done, then they should be strung together using repeated-start conditions instead of giving a STOP. Allowing an I²C STOP to terminate the communication window is the recommended method, as illustrated in Figures 12.1 and 12.2.

This behaviour can be temporarily disabled by clearing the *Stop End Comms Disable* setting. In this case, an I²C STOP will NOT terminate the communication window. Instead, the communication window can be closed manually, as desired, by clearing the *Stop End Comms Disable* bit as the final I²C transaction, followed by a STOP.

12.10 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside a communication window (while RDY is high).

12.11 Event Mode Communication

The device can be set up to bypass the communication window when no activity is sensed by setting the *Event Mode* bit in the *System Settings 1* register. This is usually enabled since the master does not need to be interrupted unnecessarily during every cycle if no activity occurs. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

Event mode can only be entered if the following requirements are met:

- Events must be serviced by reading from the *System Flags* register to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every cycle, similar to streaming mode.
- The *Show Reset* bit in the Device Status register has been cleared by setting the *Ack Reset* bit in *System Settings 2*.

12.11.1 Events

Numerous events can be individually enabled in the *Event Mask* register to trigger communication in Event Mode:

- Power mode changes
- ATI events
- Touch/button events
- Movement detection
- Hall rotation event

12.11.2 Force Communication

In streaming mode, the IQS7221G I²C will provide RDY windows at regular intervals specified by the relevant power mode report rate. This will provide the master with regular opportunities to perform I²C communication as necessary.

If the device is placed in Event Mode or Halt Mode, the IQS7221G will not open RDY windows unless certain conditions are met. A new RDY window can be requested by writing 0xFF over I²C, followed by a stop condition. After a short delay, the IQS7221G will pull the RDY line low and open a new communication window. This is shown in Figure 12.3.

Figure 12.3: Force Comms Diagram

After a short delay, a new communication window will be made available, indicated by the RDY signal. The delay between the communication request and the opening of a RDY window (t_{wait}) is application specific, but will typically be under 2 milliseconds.

13 I²C Memory Map

Refer to Appendix A for more detailed descriptions of registers and bit definitions.

The IQS7221G uses two's complement to represent signed values.

Table 13.1: I²C Memory Map

Address	Length	Description	Default	Notes
Read-Only	**No. Bytes**	**Version Info**		
0x00	2	Product Number	2024	
0x01	2	Major Version	1	
0x02	2	Minor Version	0	
Read-Only	**No. Bytes**	**System Flags**		
0x10	2	System Flags		Appendix A.1
0x11	2	Hall Flags		Appendix A.2
0x12	2	Channel States		Appendix A.3
0x13	2	CH0 Events		Appendix A.4
0x14	2	CH1 Events		Appendix A.5
Read-Only	**No. Bytes**	**Hall UI Data**		
0x20	2	Current Interval		
0x21	2	Interval Upper Limit		Same unit as Processed Angle
0x22	2	Interval Lower Limit		Same unit as Processed Angle
0x23	2	Processed Angle		0 – 65536 → 0° – 360°
0x24	2	Absolute Angle		0 – 65536 → 0° – 360°
0x25	2	Filtered Magnet Speed		Signed 16-bit value
0x26	2	Reserved		
0x27	2	Freewheel Speed		Signed 16-bit value
Read-Only	**No. Bytes**	**ProxFusion Counts**		
0x30	2	CH0 Filtered Counts		
0x31	2	CH0 Button LTA		
0x32	2	CH0 Button Delta		Signed 16-bit value
0x33	2	CH0 Movement LTA		
0x34	2	CH0 Movement Delta		Signed 16-bit value
0x35	2	CH1 Filtered Counts		
0x36	2	CH1 Button LTA		
0x37	2	CH1 Button Delta		Signed 16-bit value
0x38	2	CH1 Movement LTA		
0x39	2	CH1 Movement Delta		Signed 16-bit value

Continued on next page...

Table 13.1: I²C Memory Map (Continued)

Read-Only	No. Bytes	Hall Sensor Data		
0x40	2	Reference A0		
0x41	2	Reference B0		
0x42	2	Reference A1		
0x43	2	Reference B1		
0x44	4	Field Buffer A0		Signed 32-bit value
0x45				
0x46	4	Field Buffer B0		Signed 32-bit value
0x47				
0x48	4	Field Buffer A1		Signed 32-bit value
0x49				
0x4A	4	Field Buffer B1		Signed 32-bit value
0x4B				
0x4C	4	Field Differential A		Signed 32-bit value
0x4D				
0x4E	4	Field Differential B		Signed 32-bit value
0x4F				
Read-Only	**No. Bytes**	**Raw Sensor Data**		
0x50	2	Hall Plate A0 Counts		
0x51	2	Hall Plate B0 Counts		
0x52	2	Hall Plate A0 Inv Counts		
0x53	2	Hall Plate B0 Inv Counts		
0x54	2	Hall Plate A1 Counts		
0x55	2	Hall Plate B1 Counts		
0x56	2	Hall Plate A1 Inv Counts		
0x57	2	Hall Plate B1 Inv Counts		
0x58	2	CH0 Counts		
0x59	2	Reserved		
0x5A	2	CH1 Counts		
Read-Write	**No. Bytes**	**System Settings**		
0x60	2	System Settings 1	29707	Appendix A.6
0x61	2	System Settings 2	0	Appendix A.7
0x62	2	Events Mask	29	Appendix A.8
0x63	2	HA Report Rate	5	0 – 3000
0x64	2	NP Report Rate	40	0 – 3000
0x65	2	LP Report Rate	200	0 – 3000
0x66	2	ULP Report Rate	500	0 – 3000
0x67	2	ULP Delay	5000	
0x68	2	Watchdog Period	5000	
0x69	2	Reserved	0	
0x6A	2	I2C Timeout	200	
Read-Write	**No. Bytes**	**Hall UI Settings**		
0x70	2	Rotation UI Settings	1385	Appendix A.9
0x71	2	Angle Offset	35988	
0x72	2	High Accuracy Timeout	300	
0x73	2	Stationary Timeout	5000	

Continued on next page...

Table 13.1: I²C Memory Map (Continued)

0x74	2	Angle Betas	3073	Appendix A.10
0x75	2	Number Of Intervals	24	
0x76	2	Interval Hysteresis	250	Same unit as Processed Angle
0x77	2	Reserved	0	
0x78	2	Hall ATI Band	1000	
0x79	2	Reserved	2	
0x7A	2	Quadrature Settings	10254	Appendix A.11
0x7B	2	LP Angle Filter Beta	20	Appendix A.12
Read-Write	**No. Bytes**	**ATI Settings**		
0x80	2	Hall Target	13000	
0x81	2	CH0 Base	32000	
0x82	2	CH0 Target	6500	
0x83	2	CH1 Base	32000	
0x84	2	CH1 Target	6500	
0x85	2	Hall Gain	8385	
0x86	2	CH0 Multipliers		Appendix A.13
0x87	2	CH1 Multipliers		Appendix A.14
0x88	2	Reserved	0	
0x89	2	CH0 Compensation		
0x8A	2	CH1 Compensation		
0x8B	2	Hall Offset 0		Appendix A.15
0x8C	2	Hall Offset 1		Appendix A.16
0x8D	2	Hall Bias	52	
Read-Write	**No. Bytes**	**Freewheel UI Settings**		
0x90	2	Freewheel Filter Betas	0	Appendix A.17
0x91	2	Freewheel Friction	0	
0x92	2	Freewheel Damping	0	
0x93	2	Freewheel Inertia	0	
0x94	2	Freewheel Minimum Start Speed	0	
0x95	2	Freewheel Stop Speed	0	
0x96	2	CH0 Movement Stop Threshold	0	
0x97	2	CH0 Movement Forward Threshold	0	
0x98	2	CH0 Movement Reverse Threshold	0	
0x99	2	Hall Movement Stop Threshold	0	
0x9A	2	Stationary Detect Speed	0	
Read-Write	**No. Bytes**	**Channel 0 Settings**		
0xB0	2	CH0 Button Timeout	8000	
0xB1	2	CH0 Dormancy Timeout	4000	
0xB2	2	CH0 ATI Retry Delay	1000	
0xB3	2	CH0 Betas 1	2564	Appendix A.18
0xB4	2	CH0 Betas 2	3076	Appendix A.19
0xB5	2	CH0 Fast LTA Bound	50	
0xB6	2	CH0 ATI Band	1000	
0xB7	2	CH0 LTA Halt Threshold	200	

Continued on next page...

Table 13.1: I²C Memory Map (Continued)

0xB8	2	CH0 Button Threshold	500	
0xB9	2	CH0 Button Debounce	5138	Appendix A.20
0xBA	2	CH0 Movement Threshold	250	
0xBB	2	CH0 Movement Debounce	25618	Appendix A.21
0xBC	2	CH0 Sensor Settings 1	292	Appendix A.22
0xBD	2	CH0 Sensor Settings 2	1798	Appendix A.23
Read-Write	**No. Bytes**	**Channel 1 Settings**		
0xC0	2	CH1 Button Timeout	8000	
0xC1	2	CH1 Dormancy Timeout	4000	
0xC2	2	CH1 ATI Retry Delay	1000	
0xC3	2	CH1 Betas 1	2564	Appendix A.24
0xC4	2	CH1 Betas 2	3076	Appendix A.25
0xC5	2	CH1 Fast LTA Bound	50	
0xC6	2	CH1 ATI Band	1000	
0xC7	2	CH1 LTA Halt Threshold	200	
0xC8	2	CH1 Button Threshold	500	
0xC9	2	CH1 Button Debounce	5138	Appendix A.26
0xCA	2	CH1 Movement Threshold	250	
0xCB	2	CH1 Movement Debounce	25618	Appendix A.27
0xCC	2	CH1 Sensor Settings 1	2084	Appendix A.28
0xCD	2	CH1 Sensor Settings 2	1826	Appendix A.29
Read-Write	**No. Bytes**	**Haptic Settings**		
0xD0	2	Haptic Global Settings	4	Appendix A.30
0xD1	2	LRA Frequency	0	
0xD2	2	Reserved	0	

14 Ordering Information

14.1 Ordering Code

Table 14.1: Order Code Description

IQS7221G zzz ppb

IC NAME				IQS7221G
CONFIGURATION	zzz	=	001	I^2C address: 0x50
		=	002	I^2C address: 0x56
PACKAGE TYPE	pp	=	QF	QFN-20 Package
BULK PACKAGING	b	=	R	QFN-20 Reel (2000 pcs/reel)

14.2 Top Marking

14.2.1 QFN20 Package Marking (IQS7221GzzzQFR)

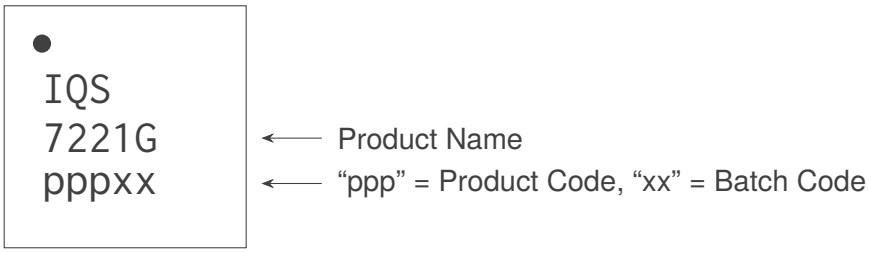


Figure 14.1: IQS7221G-QFN20 Package Top Marking

14.2.2 QFN20 Alternative Package Marking (IQS7221GzzzQFR)

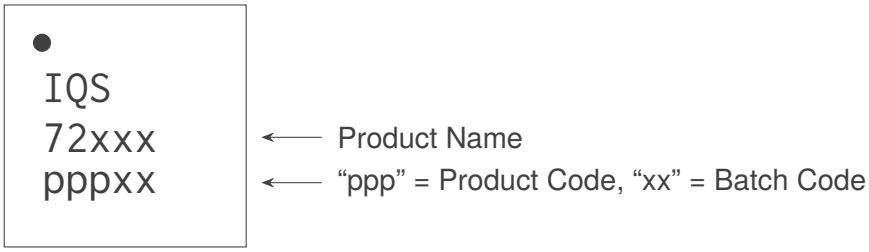


Figure 14.2: IQS72xxx-QFN20 Package Top Marking

15 Package Information

15.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

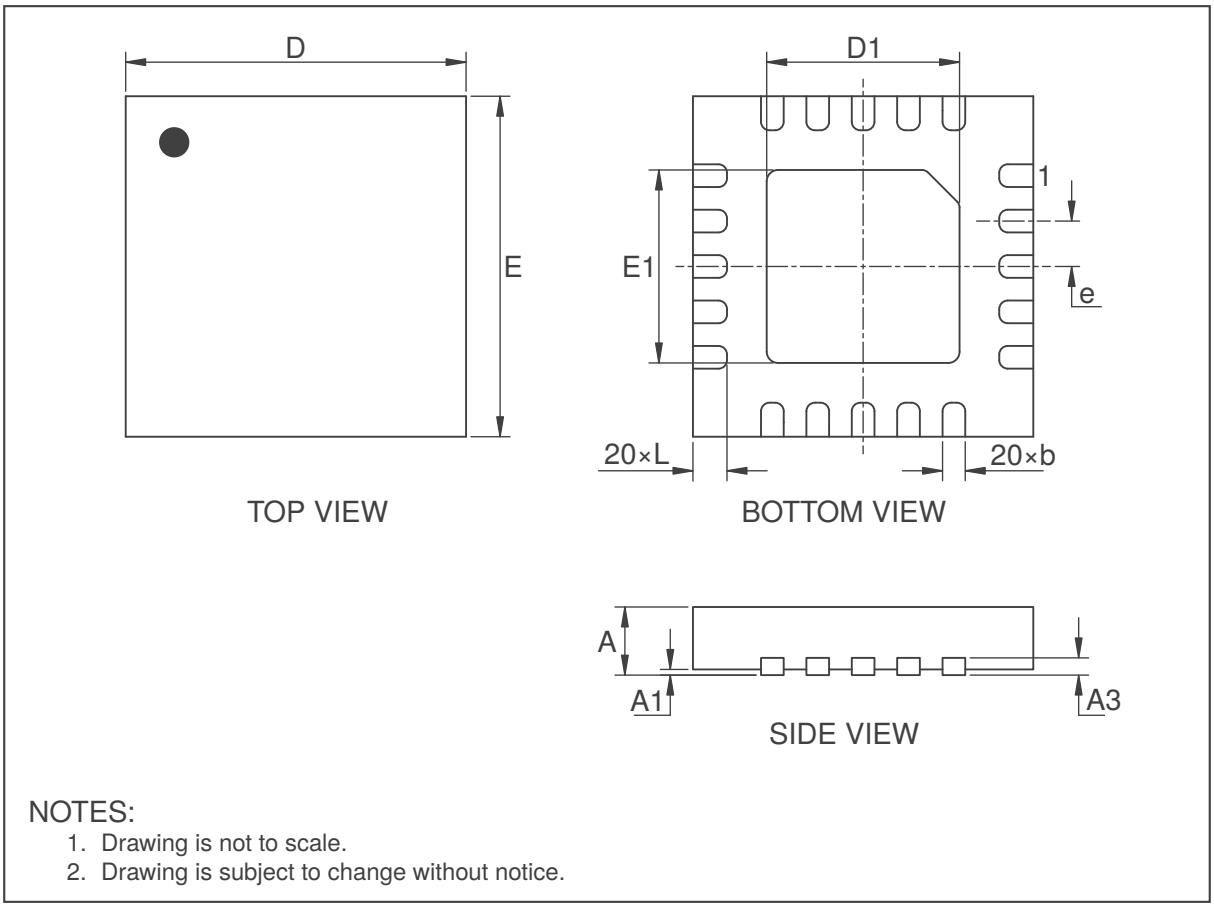
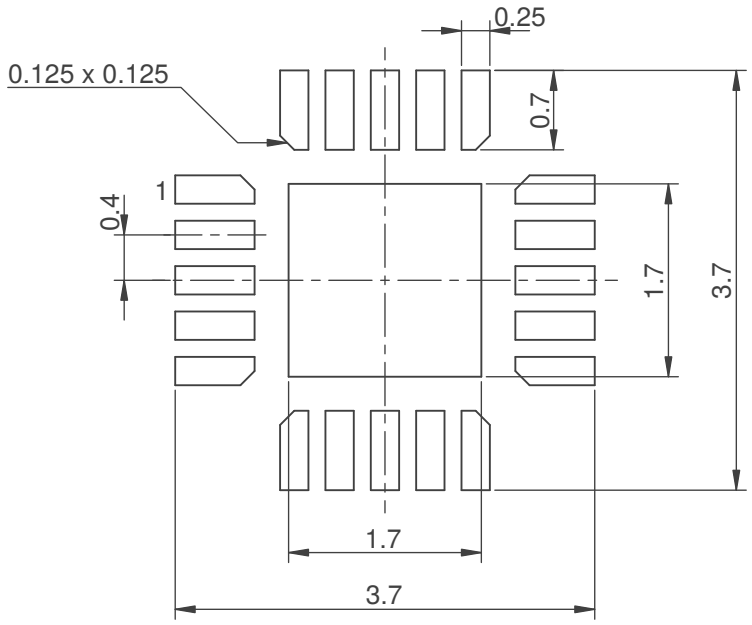


Figure 15.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

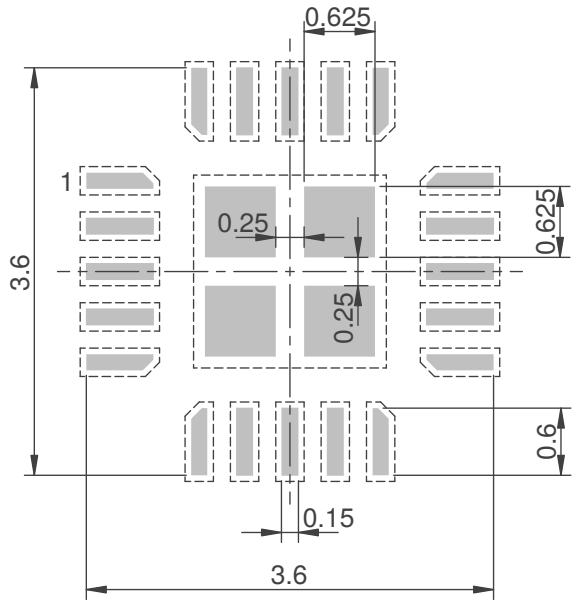
Table 15.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

15.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



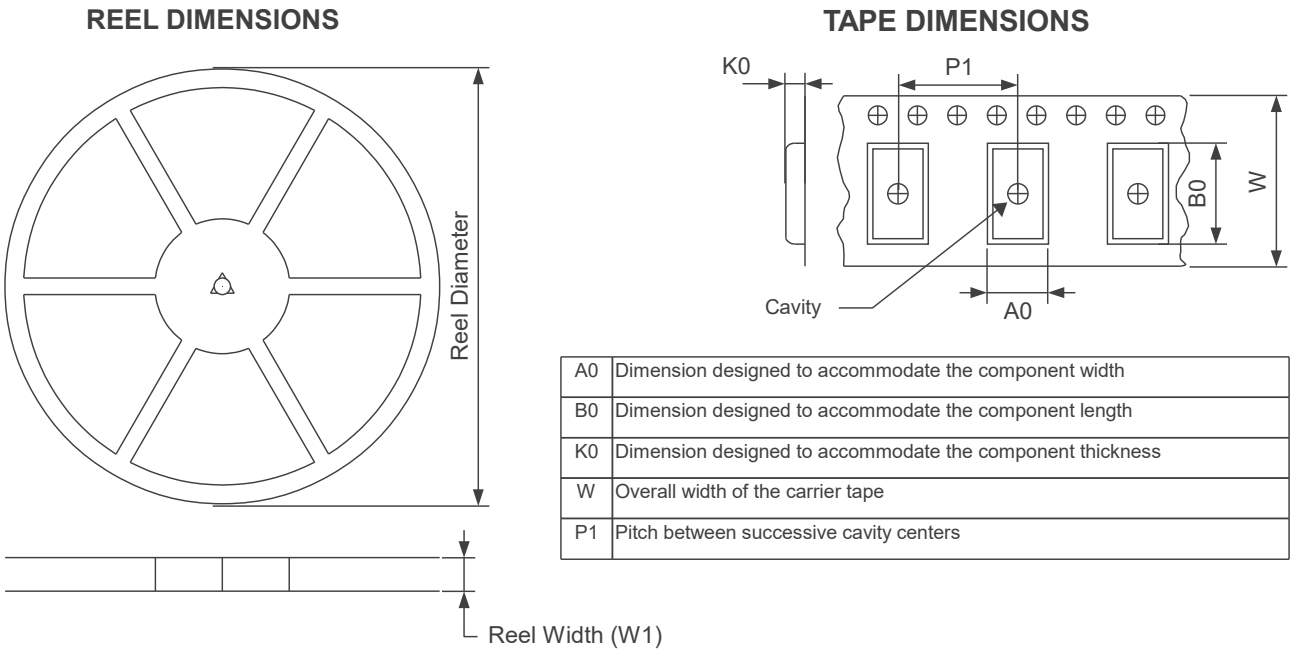
RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 15.2: QFN (3x3)-20 (QFR) Recommended Footprint

15.3 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 15.3: Tape and Reel Specification

Table 15.2: Tape and Reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

15.4 Moisture Sensitivity Levels

Table 15.3: Moisture Sensitivity Levels

Package	MSL
QFN20	1

15.5 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

A.1 System Flags (0x10)

Bit	15	14	13	12	11	10	9	8
Description	Reserved			Hall Interval Event	Channel 1 Event	Channel 0 Event	ATI Event	Power Mode Event

Bit	7	6	5	4	3	2	1	0
Description	Reserved					Power Mode		Show Reset

- Bit 12: **Hall Interval Event**
  - 0: No event
  - 1: Interval change occurred
  - Cleared on read
- Bit 11: **Channel 1 Event**
  - 0: No event
  - 1: Button or Movement event occurred on CH1
  - Cleared on read
- Bit 10: **Channel 0 Event**
  - 0: No event
  - 1: Button or Movement event occurred on CH0
  - Cleared on read
- Bit 9: **ATI Event**
  - 0: No event
  - 1: ATI event occurred
  - Cleared on read
- Bit 8: **Power Mode Event**
  - 0: No event
  - 1: Power mode change occurred
  - Cleared on read
- Bit 1-2: **Current Power Mode**
  - 0: High Accuracy
  - 1: Normal
  - 2: Low
  - 3: Ultra-Low
- Bit 0: **Show Reset**
  - 0: No event
  - 1: System reset event occurred

A.2 Hall Flags (0x11)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						Magnet Stationary	Free-wheeling

Bit	7	6	5	4	3	2	1	0
Description	Reserved				High-Accuracy	Stationary	Direction	Interval Change

- Bit 9: **Magnet Stationary**
  - Only used when freewheeling is active
  - 0: Magnet currently moving
  - 1: Magnet stopped moving since freewheeling started. Any new movement of the magnet will stop freewheeling.

- Bit 8: **Freewheeling**
  - 0: Virtual freewheeling is inactive
  - 1: Virtual freewheeling currently active
- Bit 3: **High-Accuracy**
  - 0: Device not in high-accuracy mode
  - 1: IQS7221G sampling at high-accuracy report rate to avoid aliasing
- Bit 2: **Stationary**
  - 0: Magnet moved recently. IQS7221G samples at normal or high-accuracy report rate.
  - 1: Magnet is considered stationary when interval has not changed for some time. IQS7221G may transition to lower power mode.
- Bit 1: **Direction**
  - 0: Interval change in negative direction
  - 1: Interval change in positive direction
- Bit 0: **Interval Change**
  - 0: No interval change occurred
  - 1: Interval change occurred

A.3 Channel States (0x12)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						CH1 ATI Error	CH1 Dormant

Bit	7	6	5	4	3	2	1	0
Description	Reserved						CH0 ATI Error	CH0 Dormant

- Bit 9: **CH1 ATI Error**
  - 0: No error
  - 1: CH1 failed to calibrate correctly
- Bit 8: **CH1 Dormant**
  - 0: Recent activity on CH1 occurred
  - 1: Channel is considered dormant after some period of inactivity. Allows IQS7221G to transition to a lower power mode.
- Bit 1: **CH0 ATI Error**
  - 0: No error
  - 1: CH0 failed to calibrate correctly
- Bit 0: **CH0 Dormant**
  - 0: Recent activity on CH0 occurred
  - 1: Channel is considered dormant after some period of inactivity. Allows IQS7221G to transition to a lower power mode.

A.4 CH0 Events (0x13)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Movement Event Exited	Movement Event Entered	Reserved	Movement Debouncing	Movement Direction	Movement Active

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Button Event Exited	Button Event Entered	Button LTA Halted	Button Debouncing	Reserved	Button Active

- Bit 13: **Movement Event Exited**
  - 0: No event
  - 1: “Release” event. *Movement Active* state transitioned from ‘0’ to ‘1’ with a negative delta.
- Bit 12: **Movement Event Entered**
  - 0: No event
  - 1: “Touch” event. *Movement Active* state transitioned from ‘0’ to ‘1’ with a positive delta.
- Bit 10: **Movement Debouncing**
  - 0: CH0 not currently debouncing
  - 1: CH0 currently debouncing by sampling at high-accuracy report rate
- Bit 9: **Movement Direction**
  - 0: Movement delta is less than 0
  - 1: Movement delta is greater than 0
- Bit 8: **Movement Active**
  - 0: No movement detected
  - 1: Movement occurring on CH0. The movement UI delta is currently above the threshold.
- Bit 5: **Button Event Exited**
  - 0: No event
  - 1: “Button release” event. *Button Active* state transitioned from ‘1’ to ‘0’.
- Bit 4: **Button Event Entered**
  - 0: No event
  - 1: “Button press” event. *Button Active* state transitioned from ‘0’ to ‘1’.
- Bit 3: **Button LTA Halted**
  - 0: CH0 LTA is filtering normally
  - 1: CH0 LTA filter is halted to improve channel sensitivity
- Bit 2: **Button Debouncing**
  - 0: CH0 not currently debouncing
  - 1: CH0 currently debouncing by sampling at high-accuracy report rate
- Bit 0: **Button Active**
  - 0: Button UI delta currently below threshold
  - 1: Button UI delta currently above threshold. Button is considered “pressed”.

A.5 CH1 Events (0x14)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Movement Event Exited	Movement Event Entered	Reserved	Movement Debouncing	Movement Direction	Movement Active

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Button Event Exited	Button Event Entered	Button LTA Halted	Button Debouncing	Reserved	Button Active

- Bit 13: **Movement Event Exited**
  - 0: No event
  - 1: “Release” event. *Movement Active* state transitioned from ‘0’ to ‘1’ with a negative delta.
- Bit 12: **Movement Event Entered**
  - 0: No event
  - 1: “Touch” event. *Movement Active* state transitioned from ‘0’ to ‘1’ with a positive delta.
- Bit 10: **Movement Debouncing**
  - 0: CH0 not currently debouncing
  - 1: CH0 currently debouncing by sampling at high-accuracy report rate
- Bit 9: **Movement Direction**
  - 0: Movement delta is less than 0
  - 1: Movement delta is greater than 0

- Bit 8: **Movement Active**
  - 0: No movement detected
  - 1: Movement occurring on CH0. The movement UI delta is currently above the threshold.
- Bit 5: **Button Event Exited**
  - 0: No event
  - 1: “Button release” event. *Button Active* state transitioned from ‘1’ to ‘0’.
- Bit 4: **Button Event Entered**
  - 0: No event
  - 1: “Button press” event. *Button Active* state transitioned from ‘0’ to ‘1’.
- Bit 3: **Button LTA Halted**
  - 0: CH0 LTA is filtering normally
  - 1: CH0 LTA filter is halted to improve channel sensitivity
- Bit 2: **Button Debouncing**
  - 0: CH0 not currently debouncing
  - 1: CH0 currently debouncing by sampling at high-accuracy report rate
- Bit 0: **Button Active**
  - 0: Button UI delta currently below threshold
  - 1: Button UI delta currently below threshold. Button is considered “pressed”.

A.6 System Settings 1 (0x60)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	CH1 in ULP	CH0 in ULP	Hall in ULP	Halt	Auto Power Modes	Power Mode	

Bit	7	6	5	4	3	2	1	0
Description	Reserved		GPIO Button Channel		FOSC Selection	Haptics Enable	Event Mode	I2C Enable

- Bit 14: **CH1 in ULP**
  - 0: Disable CH1 during ULP
  - 1: CH1 may sample during ULP
- Bit 13: **CH0 in ULP**
  - 0: Disable CH0 during ULP
  - 1: CH0 may sample during ULP
- Bit 12: **Hall in ULP**
  - 0: No Hall angle measurements in ULP
  - 1: Allow Hall angle measurements in ULP
- Bit 11: **Halt**
  - 0: Halt mode disabled
  - 1: Halt mode enabled
- Bit 10: **Auto Power Modes**
  - 0: Automatic power mode switching disabled
  - 1: Automatic power mode switching enabled
- Bit 8-9: **Power Mode**
  - 0: High Accuracy
  - 1: Normal
  - 2: Low
  - 3: Ultra-Low
- Bit 4-5: **GPIO Button Channel**
  - 0: None
  - 1: Echo CH0 button state on GPIO4 (open-drain active low)
  - 2: Echo CH1 button state on GPIO4 (open-drain active low)
  - This setting is incompatible with haptics

- Bit 3: **FOSC Selection**
  - 0: 18 MHz
  - 1: 14 MHz
  - This selection affects the electrical operating conditions. Please refer to Section 4.2 and Section 11.2.
- Bit 2: **Haptics Enable**
  - 0: Haptics PWM generation disabled
  - 1: Haptics PWM generation enabled (Disables the GPIO button output)
- Bit 1: **Event Mode**
  - 0: Streaming mode enabled. An I²C communications window is opened every cycle.
  - 1: Event mode enabled. An I²C communications window is opened only if an enabled event occurs.
- Bit 0: **I2C Enable**
  - 0: Standalone mode
  - 1: I²C enabled

A.7 System Settings 2 (0x61)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						Read-write Check Disable	Stop End Comms Disable

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Reseed CH1	Reseed CH0	Zero	Force ATI	Soft Reset	Ack Reset

- Bit 9: **Read-Write Check Disable**
  - 0: Read-write check enabled
  - 1: Read-only registers may be overwritten over I²C
- Bit 8: **Stop End Comms Disable**
  - 0: Close I²C communications window on I²C stop condition
  - 1: Keep I²C communications window open until a `0xFF` command is received
- Bit 5: **Reseed CH1**
  - 0: No action
  - 1: Reseed CH1 LTA
  - Bit automatically cleared
- Bit 4: **Reseed CH0**
  - 0: No action
  - 1: Reseed CH0 LTA
  - Bit automatically cleared
- Bit 3: **Zero**
  - 0: No action
  - 1: Set the processed Hall angle to the centre of interval 0
  - Bit automatically cleared
- Bit 2: **Force ATI**
  - 0: No action
  - 1: Perform ATI calibration on all channels
  - Bit automatically cleared
- Bit 1: **Soft Reset**
  - 0: No action
  - 1: Soft reset the device
  - Bit automatically cleared
- Bit 0: **Ack Reset**
  - 0: No action
  - 1: Acknowledge a device reset
  - Bit automatically cleared

A.8 Events Mask and Haptic Request (0x62)

Bit	15	14	13	12	11	10	9	8
Description	Reserved				Run Selected Waveform	Waveform Selection		

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Hall	Channel 1	Channel 0	ATI	Power Mode

- Bit 11: **Run Selected Waveform**
  - 0: No action
  - 1: Manually run a specific waveform. Specific waveform is selected in the *Waveform Selection* bit field.
  - Bit automatically cleared
- Bit 8-10: **Waveform Selection**
  - Select a waveform index to run when the *Run Selected Waveform* bit is set.
  - 1: Waveform 1
  - 2: Waveform 2
  - 3: Waveform 3
  - 4: Waveform 4
- Bit 4: **Hall**
  - 0: Hall interval event disabled
  - 1: Open an I^2C communications window on interval events
- Bit 3: **Channel 1**
  - 0: Channel 1 events disabled
  - 1: Open an I^2C communications window on any button or movement events on CH1
- Bit 2: **Channel 0**
  - 0: Channel 0 events disabled
  - 1: Open an I^2C communications window on any button or movement events on CH0
- Bit 1: **ATI**
  - 0: ATI events disabled
  - 1: Open an I^2C communications window on ATI events
- Bit 0: **Power Mode**
  - 0: Power mode events disabled
  - 1: Open an I^2C communications window on power mode changes

A.9 Hall UI Settings (0x70)

Bit	15	14	13	12	11	10	9	8
Description	Reserved				Quadrature Mode		Auto Zero Mode	

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Hall Sampling Enabled	Hall Runtime ATI	Discard Intervals	HA Free-wheeling	Reverse	Freewheel UI Enabled	Hall UI Enabled

- Bit 10-11: **Quadrature Mode**
  - 0: Off
  - 1: Open Drain
  - 2: Push Pull
- Bit 8-9: **Auto Zero Mode**
  - 0: Off
  - 1: Stationary
  - 2: Continuous
  - 3: Release

- Bit 6: **Hall Sampling Enabled**
  - 0: Sampling on Hall channels disabled
  - 1: Sampling on Hall channels enabled
- Bit 5: **Hall Runtime ATI**
  - 0: Disabled
  - 1: Enabled
- Bit 4: **Discard Intervals**
  - 0: Disabled
  - 1: Discards queued quadrature intervals when exiting high-accuracy power mode
- Bit 3: **Freewheeling in High Accuracy**
  - 0: Device may run at lower power modes during freewheeling
  - 1: Device runs at high-accuracy report rate during freewheeling
- Bit 2: **Reverse**
  - 0: Disabled
  - 1: Reverse direction of sampled rotation
- Bit 1: **Freewheel UI Enabled**
  - 0: Disabled
  - 1: Freewheel UI enabled
- Bit 0: **Hall UI Enabled**
  - 0: Disabled
  - 1: Angle calculations on Hall measurements enabled

A.10 Angle Betas (0x74)

Bit	15	14	13	12	11	10	9	8
Description	Angle Filter Beta							

Bit	7	6	5	4	3	2	1	0
Description	Auto-Zero Beta							

- Bit 8-15: **Angle Filter Beta**
  - 8-bit value
  - Range: 0 – 31
  - Sets the bandwidth of the Hall angle filter. Higher values filter with a lower bandwidth.
- Bit 0-7: **Auto-Zero Beta**
  - 8-bit value
  - Range: 0 – 15
  - Correction factor for automatic interval centering
  - Higher beta values result in smaller corrections

A.11 Quadrature Settings (0x7A)

Bit	15	14	13	12	11	10	9	8
Description	Quadrature Flank Delay							

Bit	7	6	5	4	3	2	1	0
Description	Reserved							

- Bit 8-15: **Quadrature Flank Delay**
  - 8-bit value
  - Set the minimum delay between quadrature pin state changes
  - delay = value × 50 µs

A.12 LP Angle Filter Beta (0x7B)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	LP Angle Filter Beta							

- Bit 0-7: **LP Angle Filter Beta**
  - 8-bit value
  - Range: 0 – 31
  - Sets the bandwidth of the Hall angle filter. Higher values filter with a lower bandwidth.

A.13 CH0 Multipliers (0x86)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Fine Multiplier					Coarse Gain

Bit	7	6	5	4	3	2	1	0
Description	Coarse Gain							

- Bit 9-13: **Fine Multiplier**
  - 5-bit value
- Bit 0-8: **Coarse Multiplier**
  - 9-bit value

A.14 CH1 Multipliers (0x87)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Fine Multiplier					Coarse Gain

Bit	7	6	5	4	3	2	1	0
Description	Coarse Gain							

- Bit 9-13: **Fine Multiplier**
  - 5-bit value
- Bit 0-8: **Coarse Multiplier**
  - 9-bit value

A.15 Hall Offset 0 (0x8B)

Bit	15	14	13	12	11	10	9	8
Description	Plate B0							

Bit	7	6	5	4	3	2	1	0
Description	Plate A0							

- Bit 8-15: **Plate B0**
  - 8-bit value
- Bit 0-7: **Plate A0**
  - 8-bit value

A.16 Hall Offset 1 (0x8C)

Bit	15	14	13	12	11	10	9	8
Description	Plate B1							

Bit	7	6	5	4	3	2	1	0
Description	Plate A1							

- Bit 8-15: **Plate B1**
  - 8-bit value
- Bit 0-7: **Plate A1**
  - 8-bit value

A.17 Freewheel Filter Betas (0x90)

Bit	15	14	13	12	11	10	9	8
Description	Follow Beta							

Bit	7	6	5	4	3	2	1	0
Description	Decay Beta							

- Bit 8-15: **Follow Beta**
  - 8-bit value
  - Range: 0 – 15
- Bit 0-7: **Decay Beta**
  - 8-bit value
  - Range: 0 – 15

A.18 CH0 Betas 1 (0xB3)

Bit	15	14	13	12	11	10	9	8
Description	LTA Beta							

Bit	7	6	5	4	3	2	1	0
Description	Counts Filter Beta							

- Bit 8-15: **LTA Beta**
  - 8-bit value
  - Range: 0 – 15
  - LTA filter beta value
- Bit 0-7: **Counts Filter Beta**
  - 8-bit value
  - Range: 0 – 15
  - Counts filter beta value

A.19 CH0 Betas 2 (0xB4)

Bit	15	14	13	12	11	10	9	8
Description	Low Power LTA Beta							

Bit	7	6	5	4	3	2	1	0
Description	LTA Fast Beta							

- Bit 8-15: **Low Power LTA Beta**
  - 8-bit value
  - Range: 0 – 15
  - LTA filter beta value during low power mode
- Bit 0-7: **LTA Fast Beta**
  - 8-bit value
  - Range: 0 – 15
  - LTA filter beta value when delta is negative

A.20 CH0 Button Debounce (0xB9)

Bit	15	14	13	12	11	10	9	8
Description	Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Debounce on Exit				Debounce on Enter			

- Bit 8-15: **Hysteresis**
  - 8-bit value
  - Hysteresis on Button UI threshold, calculated as

$$\text{Hysteresis} = \frac{\text{Button Threshold} \times \text{value}}{256}$$

- Bit 4-7: **Debounce on Exit**
  - 4-bit value
  - Number of high-frequency samples while exiting button state
- Bit 0-3: **Debounce on Enter**
  - 4-bit value
  - Number of high-frequency samples while entering button state

A.21 CH0 Movement Debounce (0xBB)

Bit	15	14	13	12	11	10	9	8
Description	Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Debounce on Exit				Debounce on Enter			

- Bit 8-15: **Hysteresis**
  - 8-bit value
  - Hysteresis on Movement UI threshold, calculated as

$$\text{Hysteresis} = \frac{\text{Movement Threshold} \times \text{value}}{256}$$

- Bit 4-7: **Debounce on Exit**
  - 4-bit value
  - Number of high-frequency samples while exiting movement state

- Bit 0-3: **Debounce on Enter**
  - 4-bit value
  - Number of high-frequency samples while entering movement state

A.22 CH0 Sensor Settings 1 (0xBC)

Bit	15	14	13	12	11	10	9	8
Description	Tx Pin Select							

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Enable FOSC TX	Enable 80 pF Cs	Bi-Directional	Inverse	Enabled	Mode	

- Bit 8-15: **Tx Pin Select**
  - 8-bit value
- Bit 6: **Enable FOSC TX**
  - 0: Disabled
  - 1: Run sensor at FOSC frequency
- Bit 5: **Enable 80 pF Cs**
  - 0: 40 pF internal reference capacitor (half resolution)
  - 1: 80 pF internal reference capacitor (full resolution)
- Bit 4: **Bi-Directional**
  - Allow button events to trigger for both positive and negative delta values
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Inverse**
  - Set button events to trigger for negative deltas. May be necessary for inductive sensing or mutual-capacitance sensing.
  - 0: Disabled
  - 1: Enabled
- Bit 2: **Enabled**
  - 0: Channel 0 disabled
  - 1: Channel 0 enabled
- Bit 0-1: **Sensor Mode**
  - 0: Self-Capacitance
  - 1: Mutual-Capacitance
  - 2: Inductive

A.23 CH0 Sensor Settings 2 (0xBD)

Bit	15	14	13	12	11	10	9	8
Description	Conversion Frequency							

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Rx Pin Select				ATI Mode	

- Bit 8-15: **Conversion Frequency**
  - 8-bit value
  - The following are recommended example values:

Value	Conversion Frequency (F_{xfer})	
	18 MHz F_{OSC}	14 MHz F_{OSC}
15	0.563 MHz	0.438 MHz
7	1.125 MHz	0.875 MHz
3*	2.250 MHz	1.750 MHz
1*	4.500 MHz	3.500 MHz
0*	9.000 MHz	7.000 MHz

** Please note: The maximum recommended conversion frequency for capacitive sensing is 1 MHz.*

- Bit 2-5: **Rx Pin Select**
  - 4-bit value
- Bit 0-1: **ATI Mode**
  - 0: Disabled
  - 1: Compensation Only
  - 2: Compensation and Multipliers

A.24 CH1 Betas 1 (0xC3)

Bit	15	14	13	12	11	10	9	8
Description	LTA Beta							

Bit	7	6	5	4	3	2	1	0
Description	Counts Filter Beta							

- Bit 8-15: **LTA Beta**
  - 8-bit value
  - Range: 0 – 15
  - LTA filter beta value
- Bit 0-7: **Counts Filter Beta**
  - 8-bit value
  - Range: 0 – 15
  - Counts filter beta value

A.25 CH1 Betas 2 (0xC4)

Bit	15	14	13	12	11	10	9	8
Description	Low Power LTA Beta							

Bit	7	6	5	4	3	2	1	0
Description	LTA Fast Beta							

- Bit 8-15: **Low Power LTA Beta**
  - 8-bit value
  - Range: 0 – 15
  - LTA filter beta value during low power mode
- Bit 0-7: **LTA Fast Beta**
  - 8-bit value
  - Range: 0 – 15
  - LTA filter beta value when delta is negative

A.26 CH1 Button Debounce (0xC9)

Bit	15	14	13	12	11	10	9	8
Description	Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Debounce on Exit				Debounce on Enter			

- Bit 8-15: **Hysteresis**
  - 8-bit value
  - Hysteresis on Button UI threshold, calculated as

$$\text{Hysteresis} = \frac{\text{Button Threshold} \times \text{value}}{256}$$

- Bit 4-7: **Debounce on Exit**
  - 4-bit value
  - Number of high-frequency samples while exiting button state
- Bit 0-3: **Debounce on Enter**
  - 4-bit value
  - Number of high-frequency samples while entering button state

A.27 CH1 Movement Debounce (0xCB)

Bit	15	14	13	12	11	10	9	8
Description	Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Debounce on Exit				Debounce on Enter			

- Bit 8-15: **Hysteresis**
  - 8-bit value
  - Hysteresis on Movement UI threshold, calculated as

$$\text{Hysteresis} = \frac{\text{Movement Threshold} \times \text{value}}{256}$$

- Bit 4-7: **Debounce on Exit**
  - 4-bit value
  - Number of high-frequency samples while exiting movement state
- Bit 0-3: **Debounce on Enter**
  - 4-bit value
  - Number of high-frequency samples while entering movement state

A.28 CH1 Sensor Settings 1 (0xCC)

Bit	15	14	13	12	11	10	9	8
Description	Tx Pin Select							

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Enable FOSC TX	Enable 80 pF Cs	Bi-Directional	Inverse	Enabled	Mode	

- Bit 8-15: **Tx Pin Select**
  - 8-bit value

- Bit 6: **Enable FOSC TX**
  - 0: Disabled
  - 1: Run sensor at FOSC frequency
- Bit 5: **Enable 80 pF Cs**
  - 0: 40 pF internal reference capacitor (half resolution)
  - 1: 80 pF internal reference capacitor (full resolution)
- Bit 4: **Bi-Directional**
  - Allow button events to trigger for both positive and negative delta values.
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Inverse**
  - Set button events to trigger for negative deltas. May be necessary for inductive sensing or mutual-capacitance sensing.
  - 0: Disabled
  - 1: Enabled
- Bit 2: **Enabled**
  - 0: Channel 1 disabled
  - 1: Channel 1 enabled
- Bit 0-1: **Sensor Mode**
  - 0: Self-Capacitance
  - 1: Mutual-Capacitance
  - 2: Inductive

A.29 CH1 Sensor Settings 2 (0xCD)

Bit	15	14	13	12	11	10	9	8
Description	Conversion Frequency							

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Rx Pin Select				ATI Mode	

- Bit 8-15: **Conversion Frequency**
- Example values:
  - 8-bit value

Value	Conversion Frequency (F_{xfer})	
	18 MHz F_{OSC}	14 MHz F_{OSC}
15	0.563 MHz	0.438 MHz
7	1.125 MHz	0.875 MHz
3*	2.250 MHz	1.750 MHz
1*	4.500 MHz	3.500 MHz
0*	9.000 MHz	7.000 MHz

** Please note: The maximum recommended conversion frequency for capacitive sensing is 1 MHz.*

- Bit 2-5: **Rx Pin Select**
  - 4-bit value
- Bit 0-1: **ATI Mode**
  - 0: Disabled
  - 1: Compensation Only
  - 2: Compensation and Multipliers

A.30 Haptic Global Settings (0xD0)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved					Reconfigure	Reserved	Driver Interface

- Bit 2: **Reconfigure**
  - 0: No action
  - 1: Recalculate all haptic parameters
  - Bit cleared automatically
- Bit 0: **Driver Interface**
  - 0: PWM1/PWM2
  - 1: PWM/DIR

B Revision History

Release	Date	Comments
v1.0	October 2024	Initial document released
v1.1	February 2025	Added Usage Disclaimer section. Updated haptics guidelines and memory map.

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