



IQS370 Datasheet

Quadrature mutual-inductive I²C sensing controller. Computes a temperature-stable position or angle. Resistant to external common-mode interferences.

1 Device Overview

The IQS370 ProxFusion® IC is a two-channel I²C mutual-inductive sensing device. An absolute position or angle is calculated on chip. Measurements are stable against temperature drifts and external common-mode interferences following correct design procedures. Built-in routines are provided for the simple calibration of a sensor in factory. Error correction and/or custom response curves with a lookup table are provided. Noise filtering with fast movement responses and movement detection is configurable.

Typical sensor designs allow for 8-bit measurement resolution at 1 kHz report rates. Signal processing options are available to increase the resolution up to 11-bit at slower report rates. The sensor is fully I²C compatible, and the IQS370 responds effectively even when in a low-power mode.

1.1 Main Features

- > External sensor options:
 - One absolute linear position sensor, or
 - One absolute angle sensor
- > Built-in basic functions:
 - Calibration routines for in-factory calibration (external non-volatile memory required)
 - Design-time internal gain calibration
- > Built-in signal processing options:
 - Slider or encoder position from sine/cosine sensors
 - Movement indication
 - Noise filtering with fast response to movement
 - Lookup table calibration, and/or
 - Lookup table custom functions (log, exponential, etc.)
- > Low-power mode:
 - Automatic switching when no movement detected
 - Reduced functionality in lower power mode for ultra-low-power consumption
 - Automatic wake-up to normal operation on movement
 - Less than 15 µA at report rates of 250 ms for typical sensor designs when in low-power mode.
- > Design simplicity:
 - Compatible with sensors of sizes ranging from 5–300 mm in length or diameter.
- > Supply voltage range:
 - 1.71 V to 3.6 V
- > Small package:
 - QFN20 (3 × 3 × 0.55 mm) – 0.4 mm pitch



QFN20 Package

1.2 Applications

- > Waterproof absolute position or angle sensing
- > Sound or music equipment
- > Low-power position or angle sensor applications
- > Potentiometer replacement with I²C for digital UI systems



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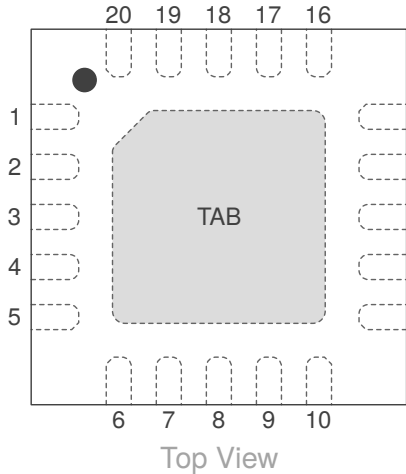
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2 Hardware Connection

2.1 QFN20 Pin Diagram

Table 2.1: 20-pin QFN Package (Top View)



Pin no.	Signal	Pin no.	Signal
1	TxC	11	NC
2	RxB	12	NC
3	RxA	13	NC
4	NC	14	NC
5	NC	15	NC
6	VREG	16	NC
7	TxB	17	MCLR/RDY
8	VDD	18	TxA
9	VSS	19	SDA
10	NC	20	SCL

Area name	Signal
TAB ⁱ	Thermal pad (floating)

2.2 Signal Descriptions

Table 2.2: Signal Descriptions

Function	Signal Name	Signal Type	Pin Type ⁱⁱ	Description
ProxFusion®	RxB	Analog	I	ProxFusion® measurement input.
	RxA	Analog	I	
	TxA	Analog	O	ProxFusion® excitation signal output.
	TxB	Analog	O	
	TxC	Analog	O	
GPIO	MCLR/RDY	Digital	IO	Active pull-up — 200k resistor to VDD. Pulled low during Power-on Reset (POR ⁱⁱⁱ), and MCLR function enabled by default.
I²C	SDA	Digital	IO	I²C Data
	SCL	Digital	IO	I²C Clock
Power	VDD	Power	P	Input supply voltage.
	VREG	Power	P	Internal regulated supply output.
	VSS	Power	P	Analog and digital ground.

ⁱ It is recommended to connect the thermal pad (TAB) to VSS.

ⁱⁱ Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

ⁱⁱⁱ POR is used to reference a clean reset state after power-on.



2.3 Reference Schematic

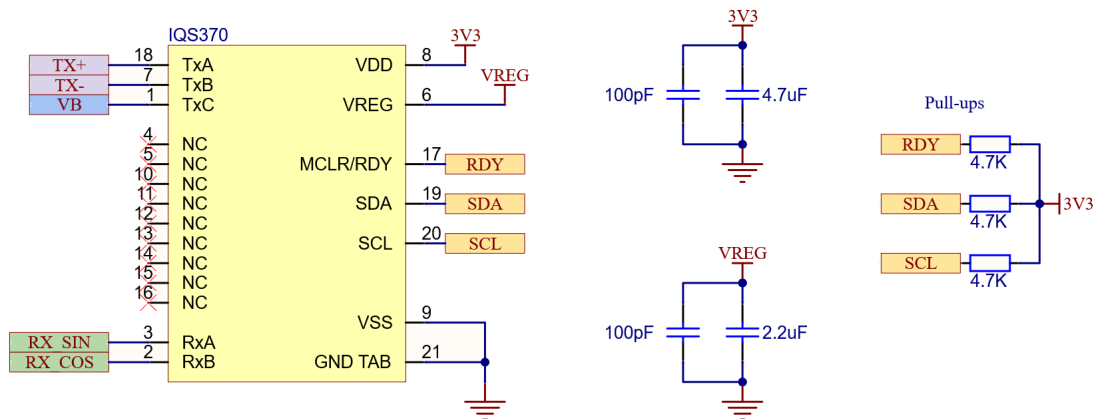


Figure 2.1: IQS370 Connections, Communication and Power Decoupling Reference Schematic

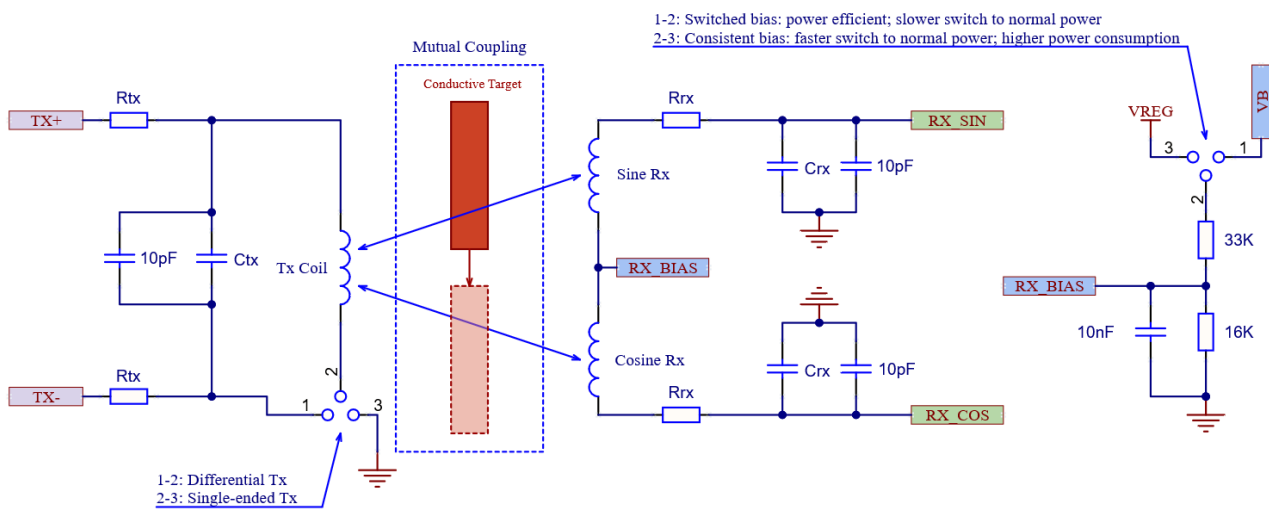


Figure 2.2: Sensor Reference Schematic



3 Block Diagram

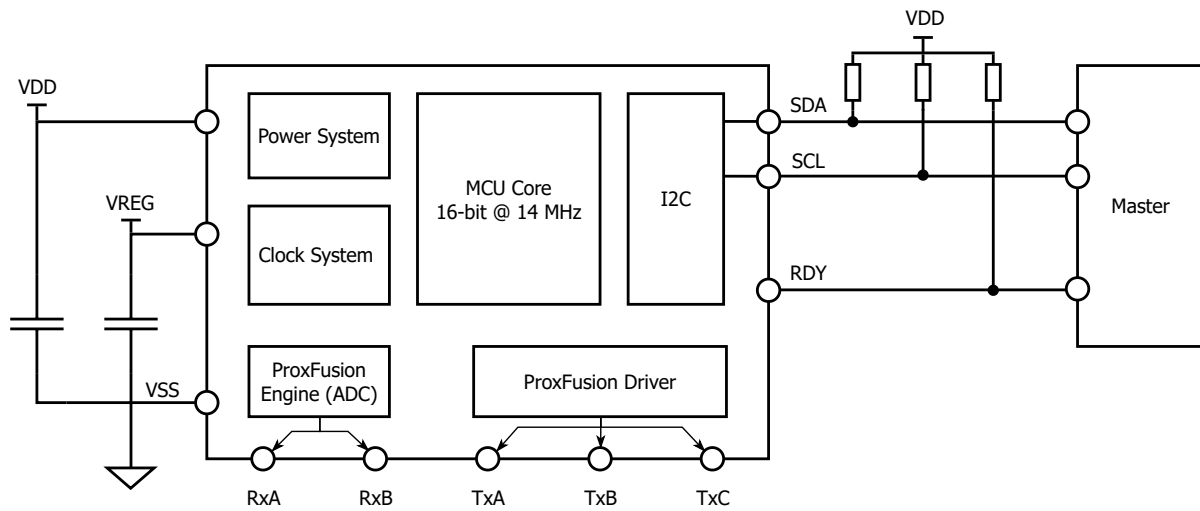
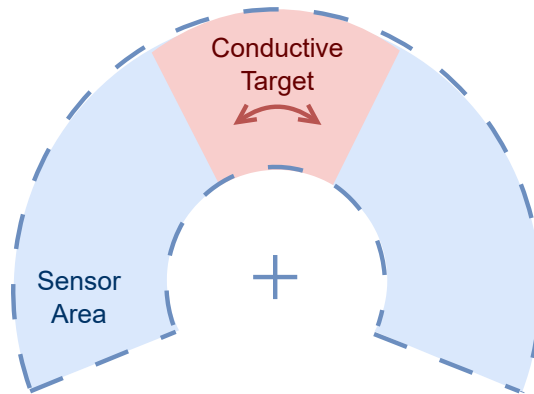


Figure 3.1: Functional Block Diagram

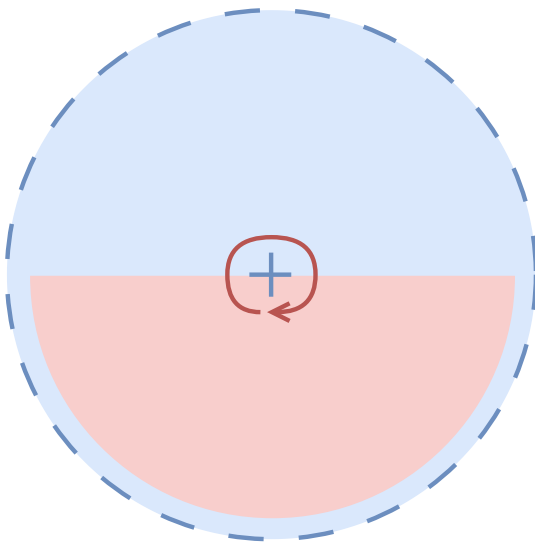


4 Supported Sensors

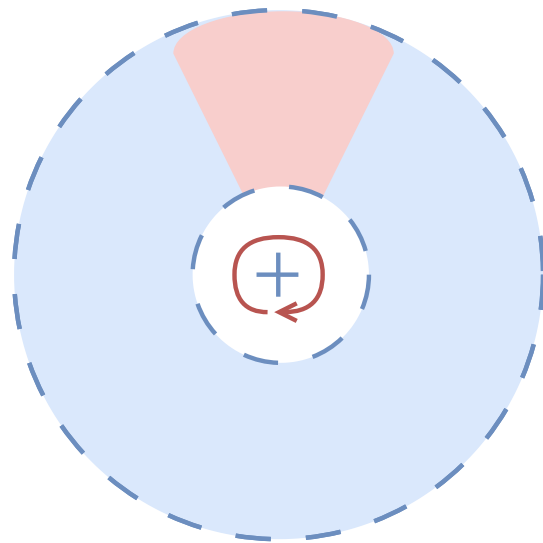
Arc Slider Sensor



Full Area Encoder Sensor



Partial Area Encoder Sensor



Linear Slider Sensor





5 Electrical Characteristics

5.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T _{stg}	-40	85	°C

5.2 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.6	V
VREG	Internal regulated supply output for analog domain		1.53		V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T _A	Operating free-air temperature	-40	25	85	°C
C _{VDD}	Recommended capacitor at VDD	2×C _{VREG}	3×C _{VREG}		μF
C _{VREG}	Recommended external buffer capacitor at VREG, ESR ≤ 200 mΩ	2 ⁱ	4.7	13	μF

5.3 ESD Rating

			Value	Unit
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁱⁱ	± 2000	V

ⁱ Absolute minimum allowed capacitance value is 1 μF, after taking derating, temperature, and worst-case tolerance into account. Please refer to the [AZD004](#) application note for more information regarding capacitor derating.

ⁱⁱ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.



5.4 Current Consumption

5.4.1 I²C Inductive Slider

- > General Test Conditions:
 - Current consumption measurements are performed in I²C event mode with no slider motion.
 - Reported current consumption does not take into account I²C communication and I²C pull-up resistors.
 - All tests report the consumption on the nominal target counts. Power consumption may change depending on target position.
 - Low-power current consumption is measured in forced low power mode (conversions enabled).
 - Power consumption is sensitive to the sensor circuit - different sensor inductances and excitation frequencies may result in higher or lower current draw.
- > NP/LP Test Conditions:
 - Mimics a typical sensor setup, optimised for resolution and linearity.
 - Target counts: 600
 - Bias stabilisation time of 10 ms.
 - Differentially driven Tx coil.
- > LP Optimised Test Conditions:
 - Mimics a more power-optimised sensor setup, preferring smaller power consumption over high resolution and linearity.
 - Target counts: 400
 - Bias stabilisation time of 3 ms.
 - Single-endedly driven Tx coil.

Report Rate [ms]	Normal Power [µA]	Low Power [µA]	Low Power Optimised [µA]
1	5200	-	-
5	1777	674	442
10	1047	250	245
15	806	238	169
25	610	147	104
50	461	75	54
100	390	40	30
150	320	25	20
200	320	19	15
250	-	16	12



6 Timing and Switching Characteristics

6.1 Reset Levels

Table 6.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < -100 V/s	0.9		

6.2 MCLR Pin Levels and Characteristics

Table 6.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS - 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

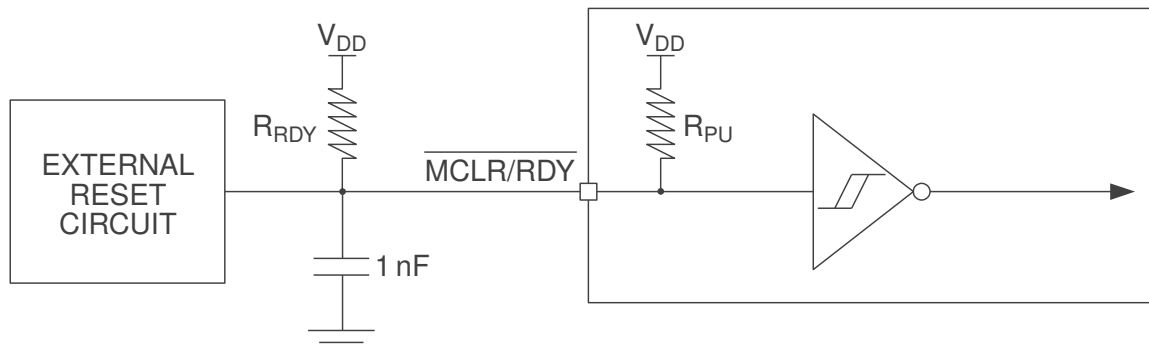


Figure 6.1: MCLR Pin Diagram

6.3 Miscellaneous Timings

Table 6.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	55	500-1500	7000	kHz
f_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz



6.4 Digital I/O Characteristics

Table 6.4: Digital I/O Characteristics

Parameter	Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL Output low voltage	$I_{sink} = 20 \text{ mA}$	0.3	V
V_{OL}	TxA Output low voltage TxB Output low voltage	$I_{sink} = 10 \text{ mA}$	0.15	V
V_{OH}	Output high voltage	$I_{source} = 20 \text{ mA}$	$VDD - 0.2$	V
V_{IL}	Input low voltage		$VDD \times 0.3$	V
V_{IH}	Input high voltage	$VDD \times 0.7$		V
C_{b_max}	SDA & SCL maximum bus capacitance		550	pF

6.5 I²C Characteristics

Table 6.5: I²C Characteristics

Parameter	Min	Max	Unit
f_{SCL}		1000	kHz
$t_{HD,STA}$	0.26		μs
$t_{SU,STA}$	0.26		μs
$t_{HD,DAT}$	0		ns
$t_{SU,DAT}$	50		ns
$t_{SU,STO}$	0.26		μs
t_{BUF}	0.5		μs
t_{SP}	0	50	ns

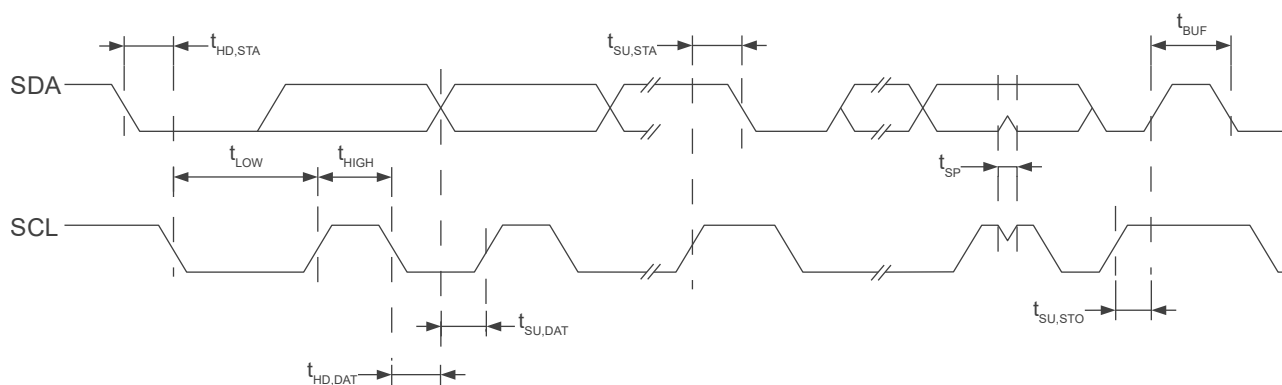


Figure 6.2: I²C Mode Timing Diagram



7 Detailed Summary of Operation

The IQS370 uses four measurement conversions from sense coils to ensure robustness against environmental changes. Various processing methods are applied to these measurements to provide a calibrated position output.

A single ProxFusion® module interfaces with the measurement pins (TxA, TxB, TxC; RxA, RxB) to facilitate conversions by exciting reception (Rx) coils via a mutually coupled transmission (Tx) coil. The excitation induced by the Tx coil onto the Rx coils appears as voltage.

The excitation induced on the Rx coils by the mutually coupled Tx coil is a positive or negative amplitude modulation. The IQS370 measures the magnitude and sign of the amplitude modulation. The Rx coils are wound in such a way that a conductive target produces an amplitude modulation having sine and cosine shapes as a function of target position. The ratio of the sine and cosine measurements is used to approximate the position of the conductive target.

Measurements are referred to as “counts” due to the internal counter used in the ProxFusion® module to perform the analogue-to-digital conversion. “Raw counts” describe the measurements directly obtained from the ProxFusion® module. The summary below omits some implementation details, which are available in further sections.

During normal power operation, the following procedures are used to provide a stable position measurement:

- > Tx excitation signals:
 - A single Tx coil is driven to excite the Rx coils.
 - The Tx coil may be driven single-endedly or differentially.
 - TxA, TxB and TxC may be configured as either single-ended or differential drivers for the Tx coil, referred to as the “Tx+”, “Tx-” or “Inactive” configurations.
 - A single-endedly driven Tx coil must be grounded on one coil side or connected to an “Inactive” Tx. The other coil side must be connected to either “Tx+” or “Tx-”.
 - A Tx coil must connect one coil terminal to “Tx+” and the other to “Tx-”.
- > Rx biasing:
 - A biasing voltage must be applied to the Rx coils.
 - This is easily achieved with a resistive voltage divider with a stabilisation capacitor.
 - TxA, TxB and TxC may also be configured as a switchable biasing pin, referred to as “Vb”.
 - The biasing point may be fed from VREG to reduce startup delays when switching from normal power, or connected to a switchable “Vb” pin to save power in a lower power mode.
- > Conversion order:
 1. The sine coil is measured. This is referred to as the $\sin^+$ (0x20) measurement.
 2. The sine coil is measured again, differentially. This is the $\sin^-$ (0x21) measurement.
 3. The cosine coil is measured. This is the $\cos^+$ (0x22) measurement.
 4. The cosine coil is measured again, differentially. This is the $\cos^-$ (0x23) measurement.
- > Conversion ordering:
 - Sine and cosine coils are arbitrarily configured on RxA and RxB.
 - $\sin^+$ and $\sin^-$ may be optionally swapped.
 - $\cos^+$ and $\cos^-$ may be optionally swapped.
 - The ordering of the $\sin^{+/-}$ and $\cos^{+/-}$ measurements influences the movement direction and starting point of the position output.
 - Oversampling is configurable, allowing multiple conversions to be accumulated for higher resolution, but slower, measurements.



- > Measurement linearisation:
 - The raw conversion counts are optionally linearised.
 - The linearisation function used is $f(x) = \frac{1}{x}$, since the counts are inversely proportional to measurement amplitude.
 - This is referred to as “linearised counts”, notated as $\sin_{lin}^{+/-}$ (0x24; 0x25) and $\cos_{lin}^{+/-}$ (0x26; 0x27).
- > Differential computation:
 - The differential measurements are computed from linearised counts.
 - The sine differential is computed as $\sin_{diff} = \sin_{lin}^{+} - \sin_{lin}^{-}$.
 - The cosine differential is computed as $\cos_{diff} = \cos_{lin}^{+} - \cos_{lin}^{-}$.
- > Calibrated differentials:
 - The differential measurements are normalised according to configurable calibration values.
 - The normalised sine differential is computed as $\sin_{norm}$ (0x14) = $(\sin_{diff} - B_{sin}) / A_{sin}$.
 - The normalised cosine differential is computed as $\cos_{norm}$ (0x15) = $(\cos_{diff} - B_{cos}) / A_{cos}$.
 - The normalising constants $A_{sin/cos}$ and $B_{sin/cos}$ are computed from the calibration values.
- > Angle computation:
 - The angle is computed from the normalised differentials.
 - A quadrant-sensitive arctangent is used: $Angle$ (0x13) = $\arctan2(\sin_{norm}, \cos_{norm})$.
 - The arctan2 function is sensitive to the polarity and order of its inputs. The conversion order of $\sin_{lin}^{+/-}$ and $\cos_{lin}^{+/-}$ must be properly configured to ensure sensible *Angle* output.
 - The computed *Angle* is filtered with a configurable IIR low-pass filter. The IIR filter may be configured to respond faster when large changes are observed.
 - When sensing boundaries are exceeded, arctan2 will “wrap around” to the beginning as a natural part of sensor behaviour.
- > Lookup table (LUT):
 - Optional and configurable.
 - 2, 3, 5, 9 or 17 points in the lookup table may be used. Values in between the points are linearly interpolated.
 - The lookup table is applied to the *Angle*, and its output is $Angle_{LUT}$ (0x12).
 - Allows for finer calibration to increase linearity.
 - Allows for custom response curve approximations, such as logarithmic or exponential responses.
 - When the LUT is disabled, $Angle_{LUT} = Angle$.
- > Range calibration:
 - Due to the “wrapping” effect of the arctan2 function, linear and arced slider sensors must have a tolerance specified at their boundaries. As such, the full range of $Angle_{LUT}$ output is not always used.
 - The used range of $Angle_{LUT}$ can optionally be calibrated in a separate calibration step.
 - Calibration values are used to convert $Angle_{LUT}$ into a calibrated position output.
 - The position has a programmable maximum value, referred to as the position *Resolution* (0x67). Position output ranges from zero to the configured *Resolution* value. The measurement resolution of the position measurement is determined by the conversion settings and sensor design.
 - $Position$ (0x11) = $\text{clamp}((Angle_{LUT} - B_{range}) / A_{range}, 0, Resolution)$.
 - The normalising constants A_{range} and B_{range} are computed from the calibration values and the position resolution.
 - Outputs outside the *Resolution* bounds are clamped. This allows “dead zones” to be specified at the boundaries of sensors. Note that this does not protect against arctan2 “wrapping” (see Section 8.3).



The IQS370 has three power modes available: normal power, automatic power switching, and forced low-power mode. Automatic power switching places the device in low-power mode when no movement has been detected for a specified time. Once movement is detected, the device will switch into normal power mode again.

During low-power operation, the following procedures are followed:

- > Fewer conversions to save power:
 - A lower report rate may be configured for low-power mode.
 - The raw counts of either $\sin^+$ or $\cos^+$ are monitored.
 - A reference conversion is also performed.
 - Position and angles are not reported in low-power mode.
- > Optimal wake-up monitoring:
 - The IQS370 automatically chooses to monitor either $\sin^+$ or $\cos^+$ conversions, depending on which conversion will be the most sensitive to change based on the current position.
 - When a change in the raw counts is detected (configurable), the device enters the normal power mode if automatic power switching is enabled.
- > Reference conversion:
 - A reference conversion allows environmental changes to be monitored in low-power mode.
 - Slow drifts in raw counts will not wake up the device.
 - The reference conversion only happens after every n 'th $\sin^+/\cos^+$ conversion (configurable) to save power.
- > Halt mode:
 - The device may be forced into low-power mode when position measurements are not required.
 - All conversions may be disabled during this time.
 - The device will not wake up from low-power until it is configured to do so.



8 Sensor Configuration

The IQS370 drives one Tx coil and measures the induced voltages on two Rx coils, as detailed in the reference schematics of Figures 2.1 and 2.2. Pinout selection is performed using the [Pin Selection \(0x43\)](#) register.

Sensor measurements are configured using the registers in the [Conversion Settings \(0x40 – 0x4A\)](#) memory block.

The pins TxA, TxB and TxC may be configured to perform any one of the following functions:

Configuration	Description
Tx+	Positive coil driving excitation.
Tx-	Negative coil driving excitation.
Vb	Switchable bias voltage, switched between VREG and floating depending on the power mode. Used to disable the biasing voltage during low-power mode.
Inactive	Inactive coil driving excitation. This pin may still experience voltage switching but does not excite the coil.

TxA, TxB and TxC may not be connected to GND. If unused, these pins must remain unconnected.

The pins RxA and RxB may be configured as the measurement points of either the sine or cosine coil. Sine and cosine must be correctly selected to ensure that the built-in calibration procedures perform as intended.

8.1 Tx Coil Configuration

Various pin configurations are possible for driving the Tx coil. Figures 8.1, 8.2 and 8.3 illustrate these configurations.

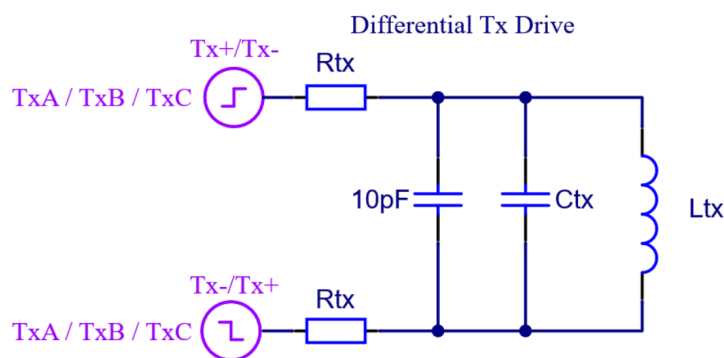


Figure 8.1: Differential Tx Coil Driving

The differential drive, as shown in Figure 8.1, is the recommended configuration, where one Tx+ and one Tx- are connected to arbitrary sides of the Tx coil. This configuration provides the most driving power and can increase measurement resolution.

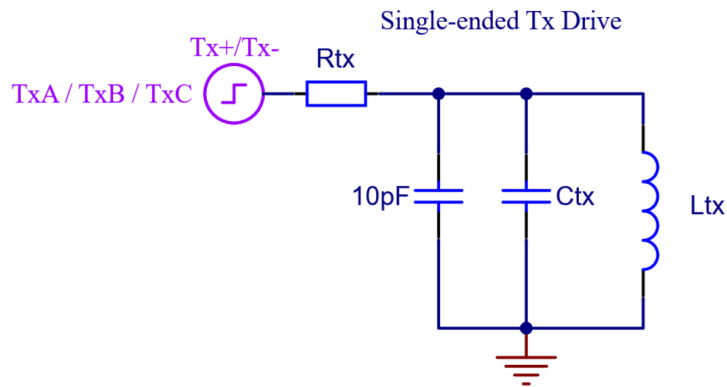


Figure 8.2: Single-Ended Tx Coil Driving

The single-ended drive, as shown in Figure 8.2, is achieved by connecting one Tx coil end to GND and another to the Tx+/Tx- pin. While this configuration may reduce the power consumption of conversions, it will also decrease the signal strength on the Rx coil side. This configuration may also be necessary if the received signals are too large. A large series capacitor may also be used to reduce power consumption further.

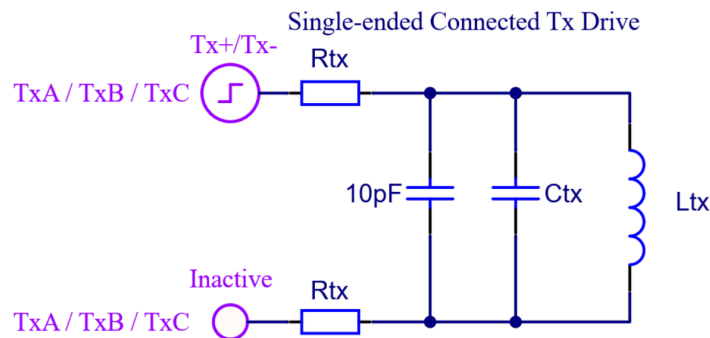


Figure 8.3: Single-Ended Tx Coil Driving, With Both Pins Connected to the IQS370. Not Recommended for Final Designs

Single-ended drive is also possible while connected to the IQS370. This is achieved by connecting one Tx coil end to an inactive pin and another to a Tx+/Tx- pin. This mode of operation adds additional series resistance to the Tx coil circuit, thereby increasing the quality factor (Q) of the resonator. This mode of operation is only recommended for testing purposes. A final design should utilise the circuit topologies of either Figure 8.1 or Figure 8.2.

It is recommended to use the TxA and/or TxB pins to act as “Tx+”, “Tx-” or “Inactive” pins. The frequency of the Tx+ and Tx- excitations is configured using the [Excitation Frequency \(0x40\)](#) register. An excitation frequency of 2.33 MHz is recommended.

8.2 Biasing Configuration

Rx coils must be biased with a constant voltage of approximately 500 mV to ensure linear operation. The biasing voltage must be decoupled with a capacitor of at least 1 nF. A value of 10 nF is recom-

mended. This is achieved by connecting a voltage divider either directly to VREG or a Vb-configured pin. It is recommended to configure TxC as Vb. Refer to Figure 8.4 for an illustration.

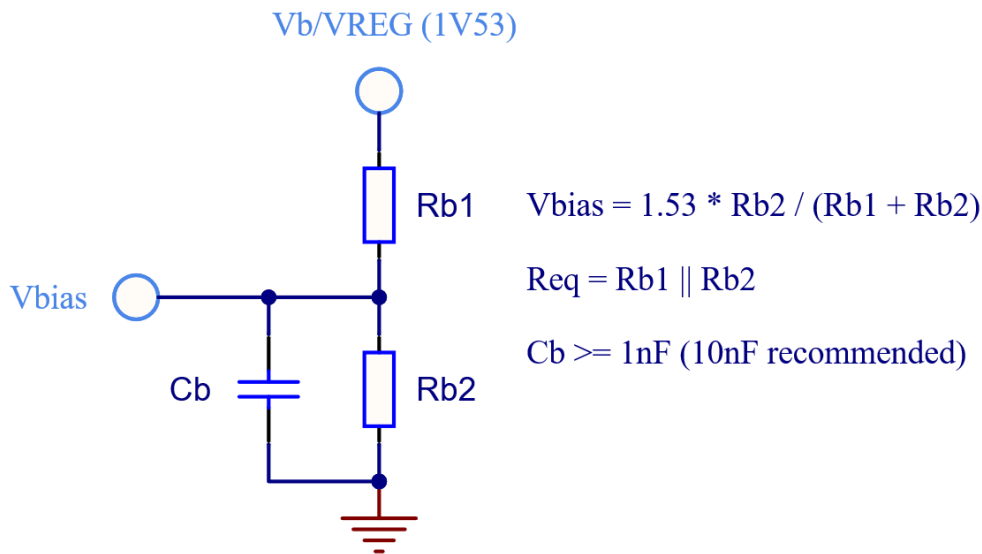


Figure 8.4: Rx Coil Biasing Divider

For ultra-low-power applications, it is recommended to utilise a Vb pin to reduce current consumption through the biasing resistor divider. For applications where a higher power consumption may be tolerated, it is best to connect the voltage divider to VREG to ensure fast response times when transitioning from power modes.

A Vb-configured pin switches its output from VREG to disconnected (floating), depending on the power mode. In normal power operation, Vb is always on, allowing for the maximum sampling rate to be achieved. In low-power, Vb is floating and only connected to VREG when a low-power conversion must take place, before being disconnected again. Refer to Figure 8.5 for a visualisation of Vb operation.

The minimum required stabilisation time depends on the RC time constant ($\tau = R_{eq}C$) of the biasing network. The *Stabilisation Times (0x45)* register may be used to define the time required before the biasing voltage has stabilised. The *Stabilisation Times* register includes *Fine* (in microseconds) and *Coarse* (in milliseconds) values, which are added together to form the stabilisation time indicated in Figure 8.5. A larger *Fine* stabilisation will increase power consumption.

Applications that connect the biasing divider network to VREG may set the stabilisation times to 0, since the biasing voltage will remain constant as long as the IQS370 is powered on.

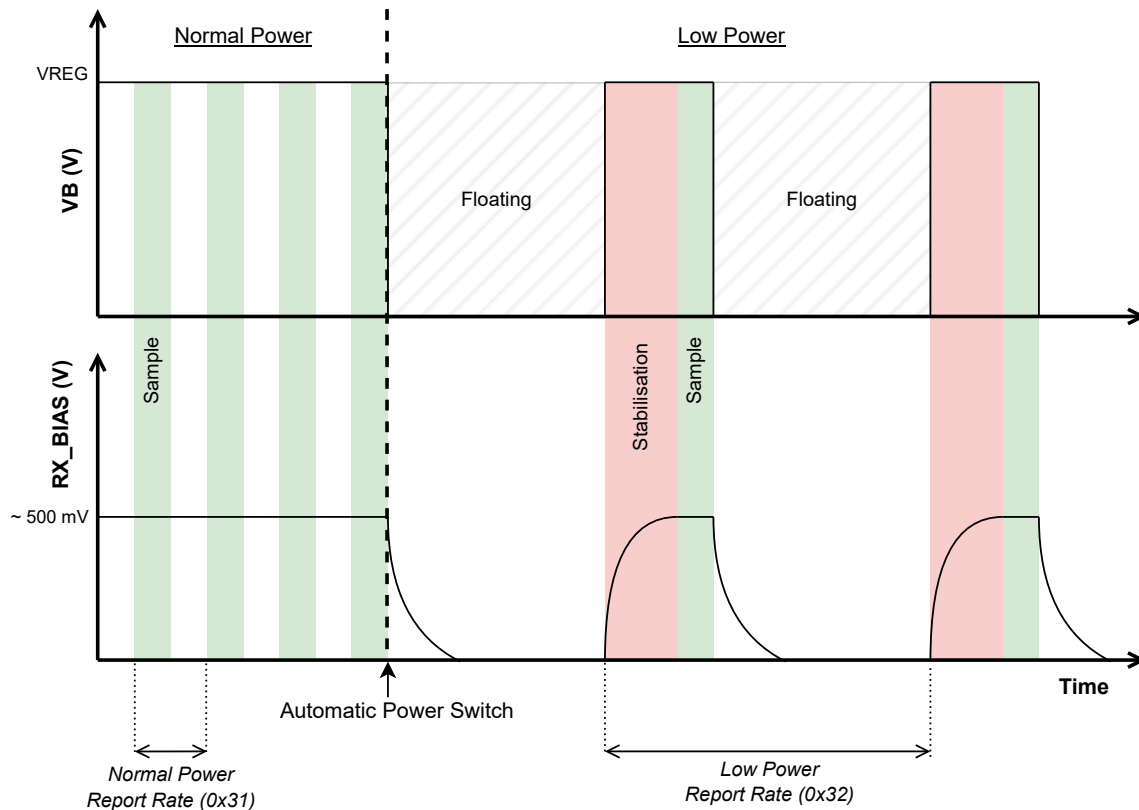


Figure 8.5: Operation of a Vb-Configured Pin, With Reference to the Node Names in the Example Biasing Network in Figure 8.4

8.3 Rx Coil Configuration

The ordering of the sine and cosine measurements is important to configure correctly to ensure that the final *Position* (0x11) output behaves as expected. This is due to the application of the arctangent function to the normalised *sin_{norm}* (0x14) and *cos_{norm}* (0x15) values, which are computed from the *Raw measurements* (0x20 – 0x23). If the *sin_{norm}* and *cos_{norm}* measurements are swapped or have the wrong polarity, then the arctangent output will be offset, and the calibration procedures will not be applied correctly.

An example of the position output for correct and incorrect polarity and sine/cosine selection is shown in Figure 8.6. Note that Figure 8.6 does not display linearity effects and assumes that the range calibration (see Section 9) is performed for the full sensor motion.

Full encoder sensors will periodically wrap in the *Position* output. Linear/arced slider sensors may “wrap” to the other side of sensing if the target is moved too close to the sensing boundaries. In a linear/arced slider sensor, it is recommended to provide sufficient mechanical tolerance to a constrained moving metal target to avoid this “wrapping” effect.

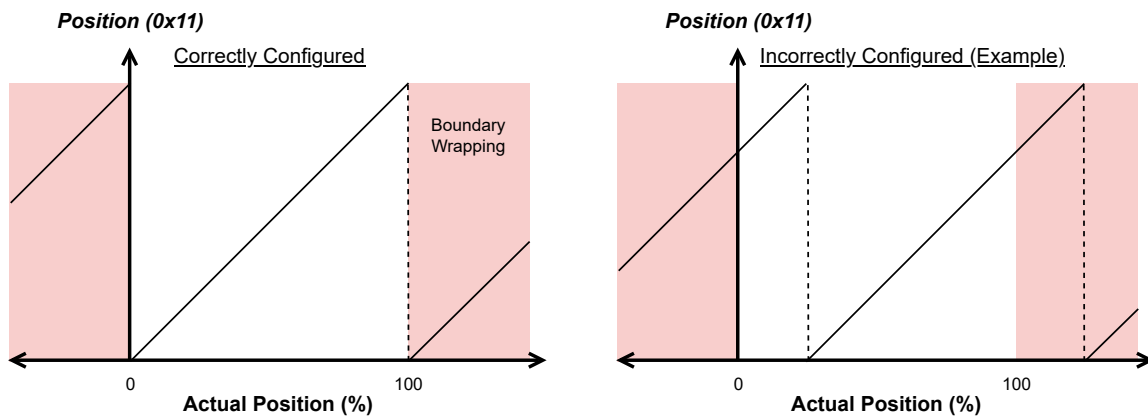


Figure 8.6: Illustration of Expected Position Output for a Correct Sine/Cosine Order and Polarity (Left) and an Example of an Incorrect Configuration (Right)

Various settings may be used to correctly configure the sine/cosine pins and their polarities. *Rx Pin Select* in the *Pin Selection (0x43)* register may be used to select the ordering of *RxA* and *RxB*. This bit will swap the sine and cosine measurements. The correct polarity of $\sin_{\text{norm}}$ and $\cos_{\text{norm}}$ is then configured by utilising the *Differential Polarity (0x44)* register, which can invert the polarity of the sine and cosine measurements individually.

Calibrated values (0x70 – 0x77) are only valid for the sine/cosine ordering and polarity configuration they were measured in.

8.4 Raw Measurement Gain

The ProxFusion® module measuring the Rx coils has a configurable gain via the *Multipliers and Dividers (0x47)* register. The Automatic Tuning Implementation (ATI) procedure may be used to automatically determine the values of the *Multipliers and Dividers* and *Compensation* registers given specific targets. The ATI procedure is triggered by configuring the ATI bit in the *System Control (0x30)* register. The ATI procedure determines the gain value given the *Base (0x49)* and *Target (0x4A)* registers.

Note that higher raw measurement values require more time to perform the conversions. An application must balance resolution with report rate and noise requirements.

The *Base* register controls the nominal counts of the *first raw measurement (0x20)* that is aimed for by the ATI procedure. It is reached by applying the *Multipliers and Dividers* gain only, without any DC subtraction. The *Target* register controls the nominal raw measurement counts after applying DC subtraction via the *Compensation* configuration.

Currently, it is not advised to use *Compensation* during measurements. It is therefore recommended to disable *Compensation* during ATI by setting $\text{Base} \geq \text{Target}$.

The ATI procedure is intended for design-time configuration only and should not be used during the operation of a sensor. *Calibrated values (0x70 – 0x77)* may only be valid for the *Multipliers and Dividers* settings they were determined for on a specific IQS370 IC.



8.5 Power Modes and Events

The IQS370 may be configured to operate in three different power modes: normal, automatic and forced low-power. The configured power mode is selection via the *Power Mode Select* bits in the *System Control (0x30)* register. The device may be active in one of two power states, which is indicated by the *Current Power Mode* bits in the *System Status (0x10)* register.

> Normal Power

- Full measurements, which compute *Position (0x11)* output, are performed, including over-sampling (if configured).
- *Normal Power Report Rate (0x31)* configures the report rate.
- When *Power Mode Select* is “Automatic”, a switch to low-power is performed when no movement event has been detected for *Movement Timeout (0x33)* milliseconds.
- Refer to Section 9.5 for more information on how movement events are detected and reported.

> Low-power

- Very limited measurements are performed to reduce power consumption. The *Position* is not computed and remains frozen as the previously computed value.
- When *Power Mode Select* is “Low-power (Forced)”, reported measurements are not useful and should be disabled. Refer to Section 8.7 for a more detailed description.
- When *Power Mode Select* is “Automatic”, a switch to normal power is performed as soon as any movement is detected in the low-power state.
- Refer to Section 8.6 for more information on low-power measurements.

Any change in power mode when *Power Mode Select* is “Automatic” is reported via the *Power* event bit in the *System Status* register.

8.6 Low-power Measurements

Fewer measurements are performed in the low-power mode to reduce current consumption. Unlike normal power, which performs four measurements, low-power only performs two measurements. No processing is performed in low-power mode, and the *Position (0x11)* is not updated. The current power state can be monitored by the master by reading the *System Status (0x10)* register. In low-power, the *Output data (0x11 – 0x15)* is frozen, whereas some *Intermediate data (0x20 – 0x27)* is invalid.

When transitioning from normal power to low-power in automatic power mode, the current *Position* is used to determine whether the $\sin^+$ (*0x20*) or $\cos^+$ (*0x22*) counts should be monitored for a wake-up into normal power operation. This selection is determined automatically by considering which of $\sin^+$ or $\cos^+$ will be most sensitive to movement.

To allow for monitoring temperature and other environmental fluctuations during low-power conversions, an additional reference measurement is performed. The reference measurement is skipped for *Low-power Reference Sample Skip (0x46)* consecutive low-power measurements. This may reduce power consumption in certain applications. The low-power and its reference measurements are stored in the *Low-power Counts (0x29)* and *Low-power Reference (0x28)* registers, respectively. For a slow *Low-power Report Rate (ms) (0x32)*, it is not recommended to skip many reference samples, as it can result in spurious wake-ups.

The difference between the reference measurement and the $\sin^+$ or $\cos^+$ measurement is monitored for movement. If movement is detected, the device will transition into normal power mode (if in automatic power mode). This wake-up movement threshold is defined by the *Wake-up Threshold* bits in the *General Processing Settings (0x60)* register. It is recommended to set the *Wake-up Threshold* as



large as possible for application requirements in order to avoid spurious wake-ups.

8.7 Halt Mode (Standby Mode)

The device can be forced into standby mode to retain device settings while also having a small power consumption. This mode of operation is achieved by forcing the IQS370 into a low-power mode using the *Power Mode Select* bits in the [System Control \(0x30\)](#) register.

In forced low-power mode, no useful measurements are made, since the IQS370 is unable to wake up into normal power operation. As such, the I²C controller must also disable measurements via the *Enable Conversions* bit in the *System Control* register.

To minimise power consumption further, the device may be placed into event mode communication to disable automatic communication windows entirely, thereby only relying on forced communication (see Section 10.13). The I²C controller must clear the event flags in the [System Status \(0x10\)](#) register (via reading) in the same communication window as enabling event mode communication when transitioning to forced low-power mode.

9 Processing

Various signal processing procedures are applied to the *Raw measurements (0x20 – 0x23)* to transform towards a position output. Calibration is typically required on a per-device basis for applications requiring high resolution and linearity. Once-off calibration shared between devices may be plausible for applications with lower linearity requirements.

9.1 Linearisation and Oversampling

Raw measurements ($\sin^{+/-}$, $\cos^{+/-}$; 0x20 – 0x23), illustrated in Figure 9.1, are linearised utilising the following transformation:

$$\text{Linearised} = \frac{16383 \cdot m}{\text{Raw}},$$

where m is the *Linearisation Multiplier (0x66)* constant. Depending on the amount of oversampling applied, it may be necessary to decrease the *Linearisation Multiplier* to ensure that no integer overflow occurs. *Linearised measurements* ($\sin_{lin}^{+/-}$, $\cos_{lin}^{+/-}$; 0x24 – 0x27) are illustrated in Figure 9.2.

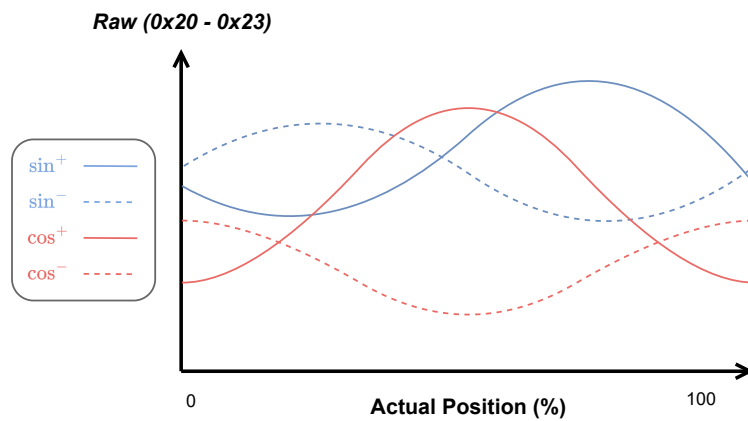


Figure 9.1: Illustration of Raw Measurements (Linearisation Enabled) With Correctly Configured Polarities

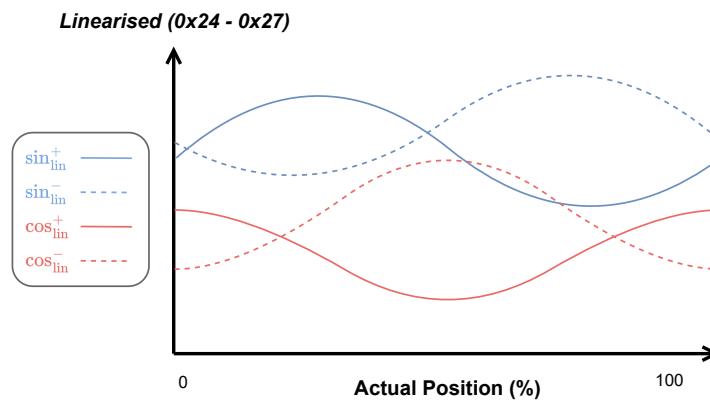


Figure 9.2: Illustration of Linearised Measurements (Linearisation Enabled) With Correctly Configured Polarities

Linearisation may be optionally bypassed using the *Linearise* bit in the *General Processing Settings (0x60)* register, which will copy the raw measurement values to the linearised measurements directly. The IQS370 is capable of software oversampling by accumulating up to 8 linearised samples using the *Oversampling* bits in the *General Processing Settings* register. Oversampling may reduce the maximum sampling rate but could provide more resolution and/or reduce noise. Oversampling will increase the device power consumption.

When oversampling is enabled, the IQS370 will perform multiple back-to-back measurements as quickly as possible while attempting to maintain the requested *Normal Power Report Rate (0x31)*. Oversampling is not applied to low-power measurements.

When linearisation is disabled, the polarity of the measurements must be inverted to obtain the same arctangent behaviour. Calibrated values are only valid for the linearisation setting the *Calibration coefficients (0x70 – 0x77)* were obtained in.

9.2 Normalisation

The linearised measurements are used to compute a differential sine and cosine signal as an intermediate step and are not available in the memory map:

$$\begin{aligned}\sin_{\text{diff}} &= \sin_{\text{lin}}^+ - \sin_{\text{lin}}^-; \\ \cos_{\text{diff}} &= \cos_{\text{lin}}^+ - \cos_{\text{lin}}^-.\end{aligned}$$

The differential signals are then normalised to $\sin_{\text{norm}}$ (0x14) and $\cos_{\text{norm}}$ (0x15) using constants computed from the *Calibration coefficients (0x70 – 0x77)*:

$$\begin{aligned}\sin_{\text{norm}} &= \frac{\sin_{\text{diff}} - B_{\sin}}{A_{\sin}}; \\ \cos_{\text{norm}} &= \frac{\cos_{\text{diff}} - B_{\cos}}{A_{\cos}}.\end{aligned}$$

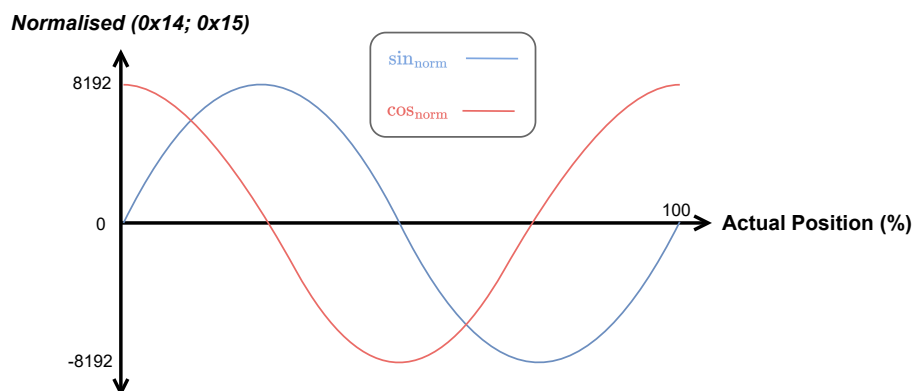


Figure 9.3: Illustration of Normalised Measurements With Correctly Configured Polarities

These constants are determined as follows:

$$A_{\sin} = \frac{1}{2} \left(\text{Sin Max } (0x70) - \text{Sin Min } (0x71) \right);$$

$$B_{\sin} = \frac{1}{2} \left(\text{Sin Max } (0x70) + \text{Sin Min } (0x71) \right);$$

$$A_{\cos} = B_{\cos} - \text{Cos Min } (0x73);$$

$$B_{\cos} = \frac{1}{2} \left(\text{Cos Offset 0 } (0x74) + \text{Cos Offset 1 } (0x75) \right).$$

The *Cos Max (0x72)* coefficient is unused but still available for the user to read. The cosine ($\cos_{\text{diff}}$) is not guaranteed to reach its maximum in a mechanically constrained linear sensor. As such, the calibration coefficients for the cosine are calculated in a manner which only utilises the minimum and offset values.

The outputs $\sin_{\text{norm}}$ and $\cos_{\text{norm}}$ are normalised to a signed 14-bit range (± 8192) and are illustrated in Figure 9.3.

9.3 Angle Computation

Normalised outputs are used to compute the *Angle (0x13)* output via the quadrant-sensitive arctangent:

$$x = \arctan2 \left(\sin_{\text{norm}}, \cos_{\text{norm}} \right).$$

Note that x is not directly stored in the *Angle* output register and must still be filtered.

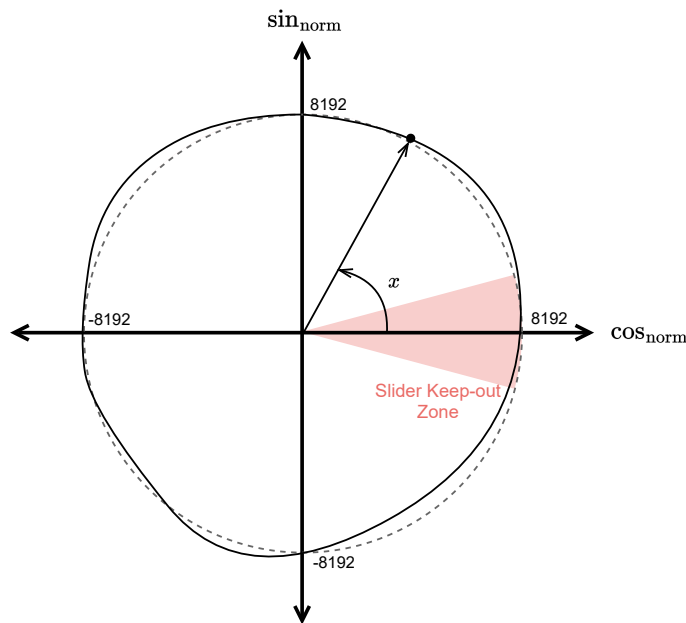


Figure 9.4: Illustration of Angle (0x13) Computation With Respect to $\sin_{\text{norm}}$ (0x14) and $\cos_{\text{norm}}$ (0x15). Example Distortion Resulting From Non-Linearity and a Keep-Out Zone for Slider Operation is Also Indicated



A 360-degree rotation (2π radians) is mapped to the 15-bit unsigned range $[0, 32767]$, which is the value stored in x . It is recommended to mechanically constrain linear sensors to operate away from the boundaries (close to 0 or 32767) due to the “wrapping” effect illustrated in Figure 8.6.

The relationship between $\sin_{\text{norm}}$ and $\cos_{\text{norm}}$ and *Angle* is illustrated in Figure 9.4, where an example of sensor non-linearity is also shown as well as a deadzone resulting from the constrained movement of a linear sensor. A full rotational sensor does not require a deadzone.

An IIR low-pass filter is available to compute the *Angle* output. This filter response may be simplified as the recursive relation:

$$\text{Angle}[n] = 2^{-\beta} \cdot x[n] + (1 - 2^{-\beta}) \cdot \text{Angle}[n - 1].$$

The filter is also modified to be circular in nature to allow for smooth rotational encoder sensing operation. For example, the filter will transition smoothly when the *Angle* transitions from 32767 to 0 via “wrapping” to the other side. I.e., the filter operates on an integer ring (modulo 32768) instead of on the integers directly.

The value of β is chosen from the *Betas (0x63)* register depending on the rate of change of x and the threshold defined in the *Fast Angle Beta Threshold (0x65)*. In particular, *Fast Beta* is used when:

$$\min(|x[n] - \text{Angle}[n - 1]|, 32768 - |x[n] - \text{Angle}[n - 1]|) > \text{Fast Angle Beta Threshold},$$

otherwise, *Slow Beta* is used. The minimum between the distance and the “wrapped” distance is selected so that “wrapping” effects from encoders’ angle sensors are not interpreted as a large change in movement. This behaviour does not influence slider sensors, since sliders are recommended to not operate in the area where wrapping may occur.

The cut-off frequency introduced by the slow and fast filter parameter (β) allows noise to be more effectively suppressed when there is no movement while also updating quickly when there are large changes in movement. A higher value of β applies more filtering. Applications are recommended to test different values in the *Betas* register in order to best suit their needs.

The 3 dB cut-off frequency for a specific value of β expressed as a fraction of the sampling frequency is tabulated below:

β	f_c/f_s
0	No Filtering
1	.42
2	.25
3	.17
4	.12
5	.080
6	.056
7	.040
8	.028

9.4 Look-Up Table

Custom response functions, such as an approximated logarithmic or exponential response, and/or error correction may be performed via the built-in lookup table (LUT). The *LUT Size (0x80)* register allows for a selection of 2, 3, 5, 9 or 17 points in the LUT table. LUT table entries are stored in the *LUT (0x81 – 0x91)* registers. Values in between LUT points are linearly interpolated.

Depending on the value in the *LUT Size* register, LUT points are equally distributed along the 0 – 32767 range of the *Angle (0x13)* output. This is illustrated in Figure 9.5.

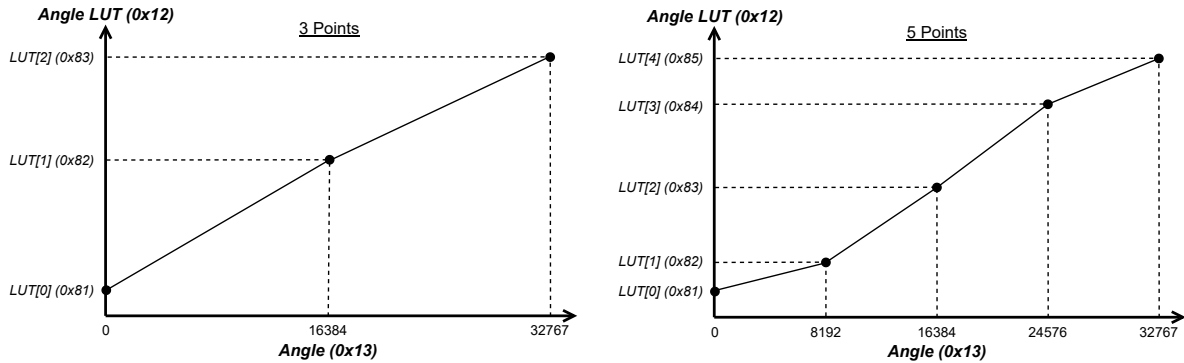


Figure 9.5: Example Lookup-Table (LUT) Configurations for a LUT Size (0x80) of 3 (Left) and 5 (Right) Points

Angle is processed with the lookup table, and its output is stored in *Angle_{LUT} (0x12)*. The lookup table may be optionally disabled with the *Enable Lookup Table* bit in the *General Processing Settings (0x60)* register. If disabled, then the value of *Angle* is directly transferred to *Angle_{LUT}*.

All LUT entries (0x81 – 0x91) should remain in the 15-bit unsigned integer range of 0 – 32767.

9.5 Position

Immediate position output prior to jitter filtering output is calculated from *Angle_{LUT} (0x12)* by considering the calibrated movement range and the requested position *Resolution (0x67)*.

Unfiltered position (*y*) is calculated as:

$$y = \text{clamp}((\text{Angle}_{\text{LUT}} - B_{\text{range}})/A_{\text{range}}, 0, \text{Resolution}),$$

where B_{range} and A_{range} are computed with *Angle Min (0x77)* and *Angle Max (0x76)* as:

$$A_{\text{range}} = \frac{\text{Angle Max} - \text{Angle Min}}{\text{Resolution}};$$

$$B_{\text{range}} = \text{Angle Min}.$$

When the immediate position range is uncalibrated, it will default to utilising the full range, and no clamping will occur. When a range is calibrated, as is typical for slider sensors with constrained movement, then clamping will occur, as illustrated in Figure 9.6.

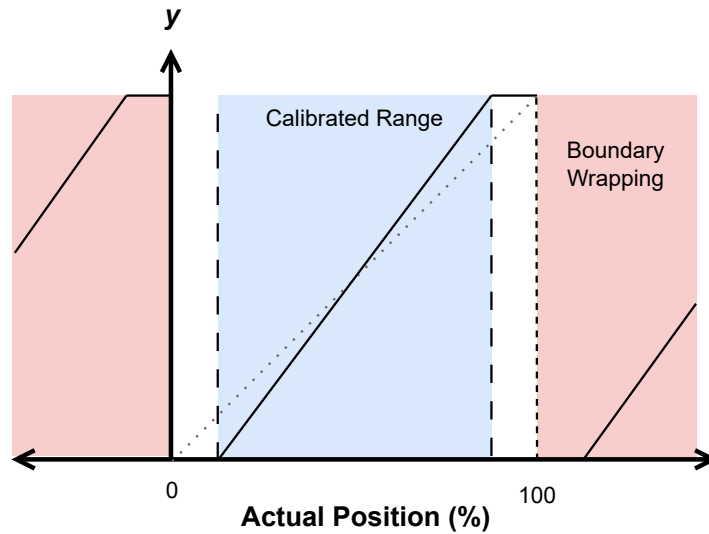


Figure 9.6: Illustration of Position Clamping When the Full Range is Not Utilised. This is the Expected Configuration for Slider Sensors

An application is required to specify the *Movement Threshold* (0x62) that defines a movement in terms of the final *Position* (0x11) output and its defined *Resolution* (0x67).

The *Position* is only updated when the currently computed immediate position (y) exceeds the *Movement Threshold*. The distance on an integer ring determined by configured *Resolution* is used:

$$d = \min(|y - \text{Position}[n - 1]|, \text{Resolution} + 1 - |y - \text{Position}[n - 1]|)$$

The ring distance computed above allows for full rotational sensors to be accommodated in terms of continuous transitions between “wrapped” output. It serves a similar purpose to the calculations performed by filtering operations in Section 9.3. The final *Position* output is calculated using:

$$\text{Position}[n] = \begin{cases} y, & d > \text{Movement Threshold} \\ \text{Position}[n - 1], & \text{otherwise} \end{cases}$$

When $d > \text{Movement Threshold}$, then a movement event is generated. The event is indicated by the *Movement* bit in the *System Status* (0x10) register, which is cleared on read.

This filtering step is referred to as ‘movement hysteresis’ or ‘jitter filtering’. Flickers in the *Position* output due to quantisation noise may be present even on very low-noise sensor designs. To generate a movement event on every change in movement to the finest resolution ($d = 1$), set *Movement Threshold* = 0.



9.6 Basic Calibration Procedures

A total of three mutually exclusive calibration steps per IQS370 device may be applicable to an application. These steps must be performed in order, after correct sine/cosine configuration (see Section 8.3), if applicable, and are enumerated below. The *Power Mode Select* bits in the *System Control (0x30)* register must be set to normal power during calibration procedures. The *Betas (0x63)* register must be set to 0. The calibrated values must be written each time an IQS370 device boots. Typical device operation and calibration procedures are illustrated in the flow diagram of Figure 9.7.

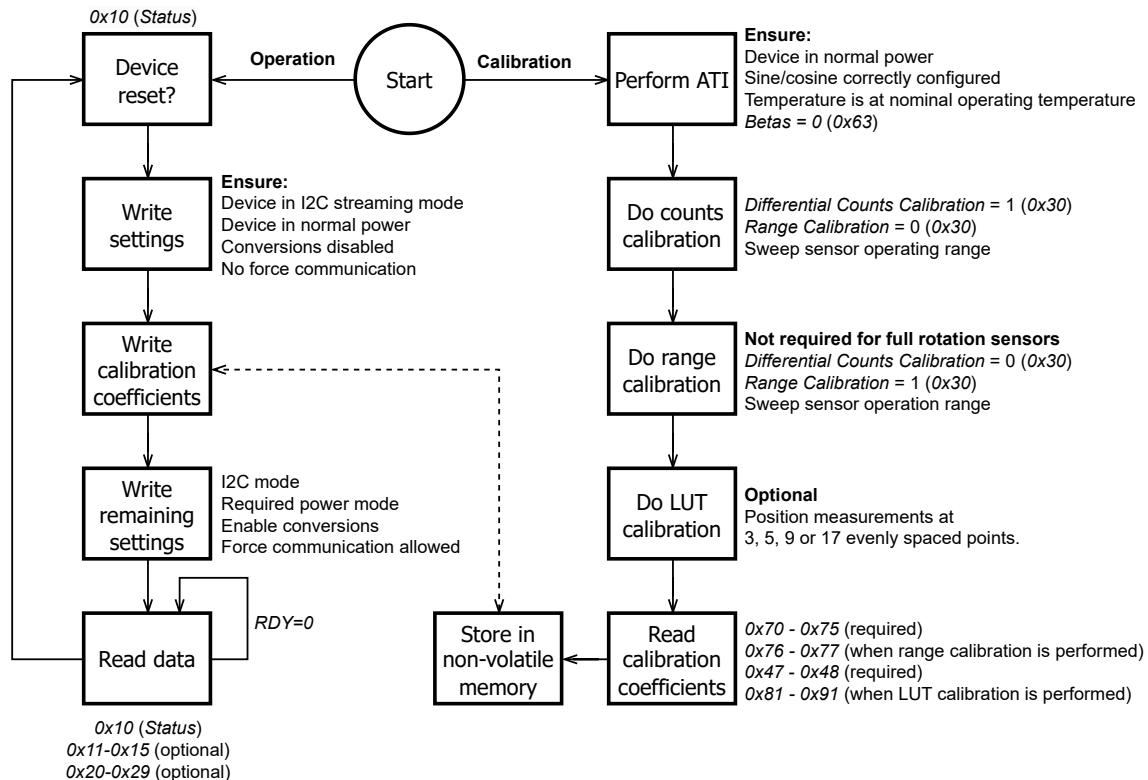


Figure 9.7: Calibration procedures and typical device operation

9.6.1 ATI

An ATI is performed via the *Do ATI* bit in the *System Control* register. This sets the gain for the current device based on the configured *Base (0x49)* and *Target (0x4A)* (see Section 8.4).

The determined gain settings in the *Multipliers and Dividers (0x47)* and *Compensation (0x48)* registers must be read once the *Do ATI* bit is cleared. The read values of *Multipliers and Dividers* and *Compensation* registers must be stored in non-volatile application memory. Depending on the component tolerances of the sensor biasing network, this may not be necessary on a per-device basis.

9.6.2 Normalisation

This step is required to ensure *Position (0x11)* linearity. The *Differential Counts Calibration* bit must be set in the *System Control (0x30)* register. The *Range Calibration* bit must be cleared. A full motion sweep must be performed at least once and must be slow enough that sine/cosine peaks and troughs can be captured with the configured *Normal Power Report Rate (0x31)*.



Once the sweep is completed, the *Differential Counts Calibration* bit must be cleared. Finally, sine and cosine *Calibrated values (0x70 – 0x75)* must be read and stored in non-volatile application memory. Depending on application linearity and resolution requirements, this step may not be necessary on a per-device basis.

9.6.3 Lookup Table Calibration

This step is optional and intended for applications where high linearity is required without requiring sensor modifications. Contact Azoteq for a detailed description of the procedure required to compute a calibrated lookup table. Lookup table calibration may be combined with a custom response curve shape to provide custom responses such as a calibrated linear, logarithmic or exponential *Position* response.

9.6.4 Range

This step is required for sensors which do not measure a full rotation, such as linear or arced slider sensors. Full rotation sensors, such as encoders, may neglect this step, as the default IQS370 values ensure that no clamping will occur on the *Position* output. In the *System Control (0x30)* register must be set while ensuring that the *Differential Counts Calibration* bit is cleared.

A full motion sweep must be performed at least once and must be slow enough that the minimum and maximum range of *Angle_{LUT} (0x12)* is captured with the configured *Normal Power Report Rate*. Once the sweep is completed, the *Range Calibration* bit must be cleared. Finally, the angle range calibration values (*0x76; 0x77*) must be read and stored in non-volatile application memory.

Optionally, a dead zone may be added to the calibration values by the I²C controller after calibration. The following modification allows for a dead zone as a percentage p of the full movement range to be added on each side of the calibrated range:

$$\begin{aligned} \text{Angle Max} &\leftarrow \text{Angle Max} - \text{round}\left(\frac{p}{100}(\text{Angle Max} - \text{Angle Min})\right); \\ \text{Angle Min} &\leftarrow \text{Angle Min} + \text{round}\left(\frac{p}{100}(\text{Angle Max} - \text{Angle Min})\right). \end{aligned}$$

Due to mechanical tolerances, some applications may require range calibration on a per-device basis in order to utilise the full range of motion sensing. Otherwise, adding a sufficient dead zone, as described above, may allow for the same range calibration to be used globally.



10 I²C Interface

10.1 Device Resets

When a device boots, the RDY line briefly acts as an open-drain reset line (active low). When the RDY line is kept low after power-on, the IQS370 device will remain in reset and will not respond to I²C communication. Normal operation ensues once the RDY line is left to go high.

The device will indicate whether it has reset via the *Reset* bit in the [System Status \(0x10\)](#) register. To clear this bit and acknowledge the reset event (in order to detect any future resets), the *Ack Reset* bit must be set in the [System Control \(0x30\)](#) register.

10.2 I²C Module Specification

The device supports a standard two-wire I²C interface with the addition of a ready (RDY) line. Byte-level clock stretching is allowed. The communications interface of the IQS370 supports the following:

- > Fast-mode-plus standard I²C up to 1 MHz.
- > Streaming data as well as event mode.

The IQS370 implements 8-bit addressing with 2 bytes at each address.

10.3 I²C Address

The default 7-bit I²C address is 0x44. The default I²C address may be changed after an IQS370 device is booted via the [I²C Address \(0xB1\)](#) register. Refer to Section 10.14 for more detail on configuring different I²C addresses when using multiple IQS370 devices per I²C bus.

The IQS370 will also respond to the address whose first bit (LSb) is the complement of the primary address.

- > Example 1: If the configured primary I²C address is 0x31 (0b0110001), the device debug address is 0x30 (0b0110000).
- > Example 2: If the configured primary I²C address is 0x50 (0b1010000), the device debug address is 0x51 (0b1010001).

The debug address is for debugging purposes only and should not be used during normal operation.

10.4 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

10.5 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words, meaning that two bytes are stored at each address. For example, address 0x10 will provide two bytes. The next two bytes read will be from address 0x11.

The 16-bit data is sent in little-endian byte order (least significant byte first).



10.6 Communication Windows (RDY)

The communication has an open-drain active-low RDY signal to inform the I²C controller that the IQS370 is ready to communicate. It is optimal for the I²C controller to use this as an interrupt input and initiate I²C reads accordingly.

When an IQS370 device has data for the I²C controller, it will pull the RDY line low. This indicates that the IQS370 device has opened its communications window, and it is expecting the I²C controller to address it. When the communication window is closed, the RDY line is released.

On startup, the RDY line functions as an active-low reset line. When RDY is held low by the I²C controller while the device is booting, the device will be kept under reset and will not respond to I²C requests until the line is released.

10.6.1 Communication Modes

The *I²C Interface Type* bits in the [System Control \(0x30\)](#) register may be used to configure the manner in which the IQS370 opens communication windows. There are two modes available:

> Streaming

- Communication windows are opened at regular intervals, depending on the configured report rate.
- When in normal power, windows are opened approximately every [Normal Power Report Rate \(0x31\)](#) milliseconds after the latest normal power measurement has taken place.
- When in low-power, windows are opened approximately every [Low-power Report Rate \(ms\) \(0x32\)](#) milliseconds after the latest low-power measurement has taken place.

> Event

- Communication windows are only opened when triggered by an event.
- When the *Movement* event bit is set in the [System Status \(0x10\)](#) register, a communication window is always opened. Refer to Section 9.5 for more information on when this event is triggered.
- When a change of power mode occurs while the *Power Mode Select* bits in the [System Control \(0x30\)](#) register are “Automatic”, a communication window may optionally open on the change of the current power mode (*Current Power Mode* bits in the [System Status](#) register), depending on whether the *Power Event* bit is set in the [Events Mask \(0x61\)](#) register.

10.6.2 Timeout

If the communication window is not serviced within the [Transaction Timeout \(0x34\)](#) period (in milliseconds), the session is ended (RDY goes high), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the I²C controller is not responsive. However, the corresponding data will be missed/lost. The default I²C timeout period is set to 200 ms and can be set to a maximum of 250 ms. The *I²C Communication Timeout* is measured from the start of the communications window (RDY goes low).

10.6.3 Invalid Communications

The device will give an invalid communication response (0xEE) under the following conditions:

- > The host is trying to read from a memory map register that does not exist.
- > The host is trying to read from the device outside of a communication window (i.e. while RDY is high).



10.7 I²C Read

A single I²C read is initiated by first writing the register address and then proceeding to read bytes after issuing an I²C RESTART on a read request. The IQS370 device will ACK (acknowledge) the register address byte that is written.

The I²C controller responds with an ACK on each read byte and ends the read sequence by issuing a NACK (not-acknowledge). Once the STOP bit is issued by the I²C controller, the communication window is closed by the IQS370 device. Register addresses are automatically incremented while the I²C controller clocks out the data. Refer to Figure 10.1 for an illustration of this procedure.

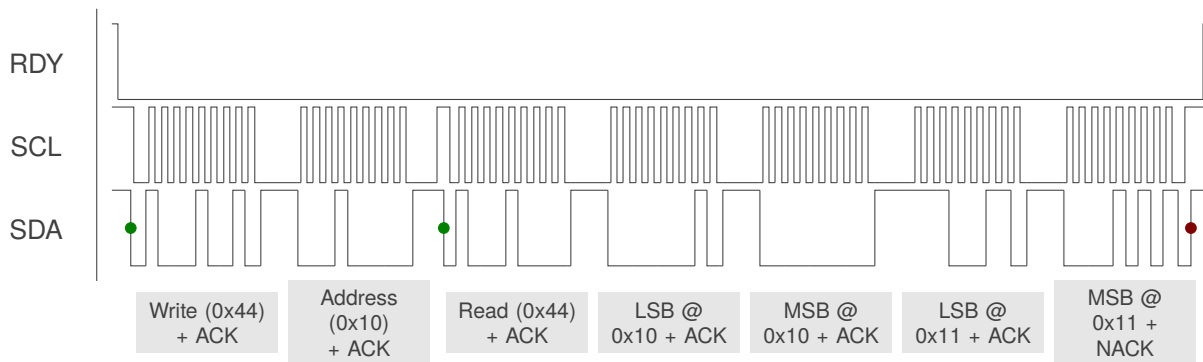


Figure 10.1: I²C Read Example: 4 Bytes Starting at Address 0x10

10.8 I²C Multiple Read

Multiple I²C reads from multiple register addresses may be performed. The procedure from Section 10.7 must be followed, but instead of ending the first register read with a STOP bit, a RESTART is issued by the I²C controller, and the process repeats until a STOP bit is issued on the last register reading transaction. An example is shown in Figure 10.2.

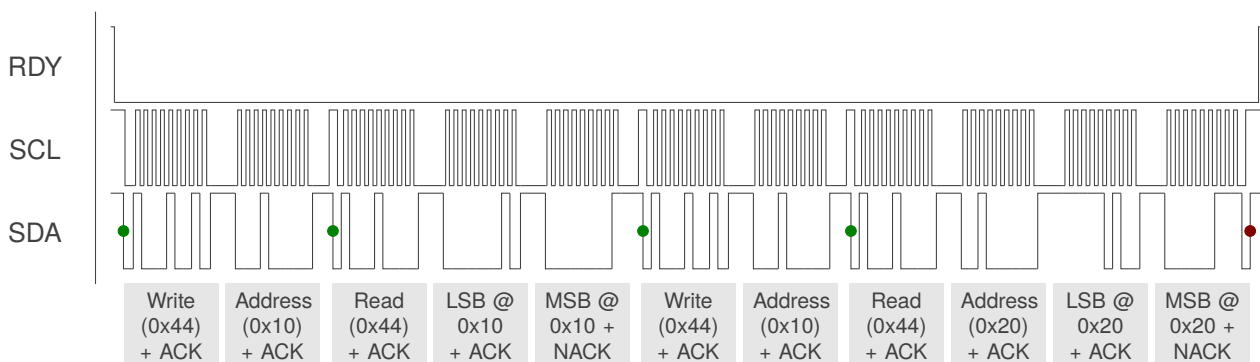


Figure 10.2: I²C Multiple Read Example: 2 Bytes at Address 0x10; 2 Bytes at Address 0x20

10.9 I²C Write

Writing to a single register is achieved by first writing the register address, immediately followed by the data bytes to be written to that address. The IQS370 device will ACK every byte. Similar to the read in Section 10.7, ending the transaction with a STOP bit will close the communication window. This is illustrated in Figure 10.3.

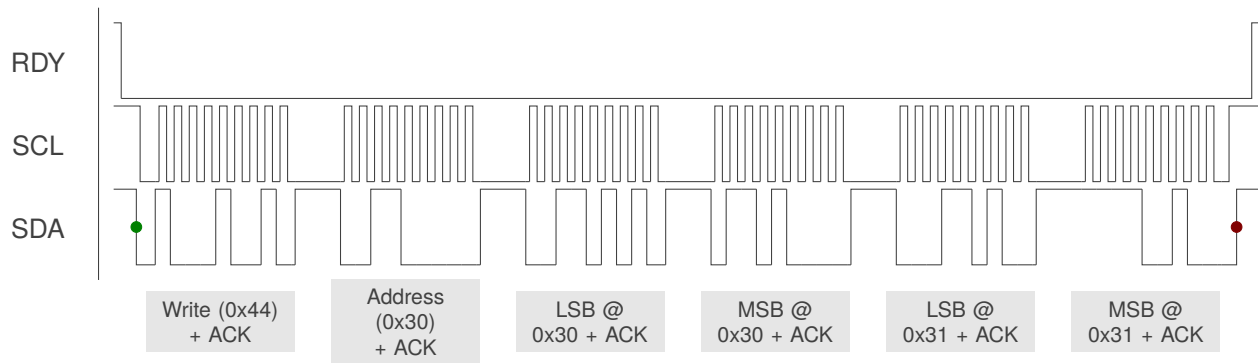


Figure 10.3: I²C Write Example: 4 Bytes Starting at Address 0x30

10.10 I²C Multiple Write

Multiple register addresses may be written in the same communication window. This is done by following the procedure in Section 10.9 but sending a RESTART write request followed by a new register address and data. The communication window is closed by issuing a STOP bit on the last writing transaction. Figure 10.4 illustrates an example.

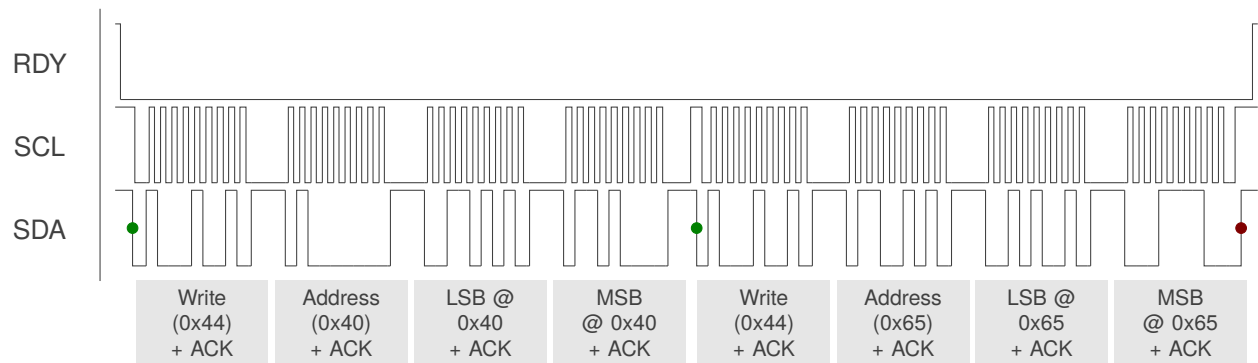


Figure 10.4: I²C Multiple Write Example: 2 Bytes Starting at Address 0x40; 2 Bytes Starting at Address 0x65

10.11 I²C Read and Write Sequence

Reading and writing sequences may be chained in the same communication window prior to a STOP bit being issued to close the communication window. The procedures in Sections 10.8 and 10.10 must be followed. An example of such a mixed transaction is shown in Figure 10.5.

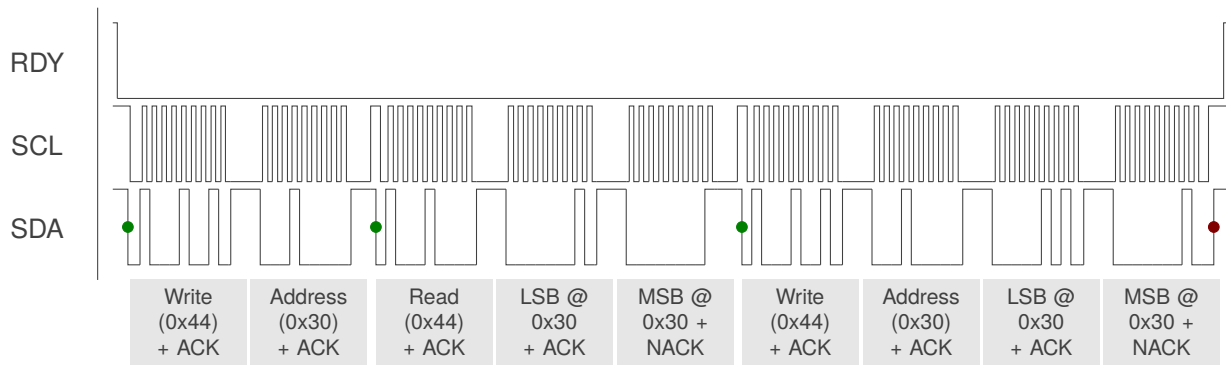


Figure 10.5: I²C Read and Write Example: Read, Modify and Write 2 Bytes Starting at Address 0x30

10.12 Force Closing Communication

A standard I²C STOP will close the current communication window. Contact Azoteq for more information on how to change this behaviour.

A communication window may be closed without sending a STOP by writing 0xFF to the device (as if it were a register address). This is shown in Figure 10.6.

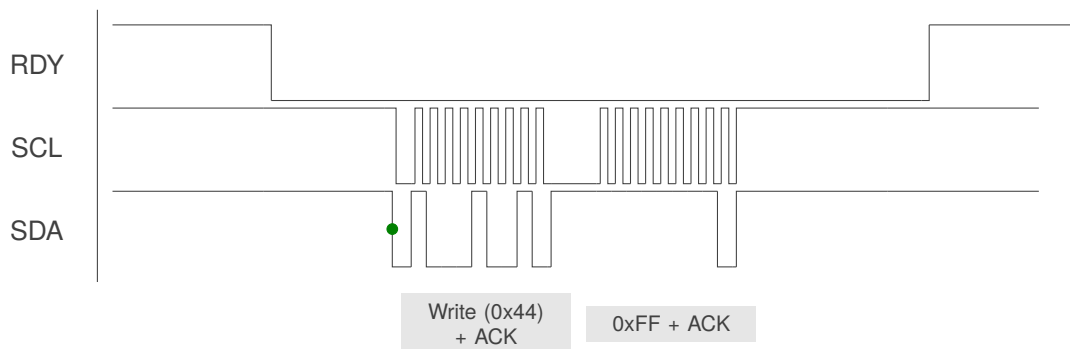


Figure 10.6: Closing the Communication Window While it Is Open. The STOP Bit at the End of “0xFF” is Optional

10.13 Force Starting Communication

In streaming mode, the IQS370 will provide communication windows (RDY pulled low by the IQS370 device) at intervals specified by the power mode sampling period. Refer to Section 10.6.1 for more detail.

Ideally, communication with the IQS370 should only be initiated in a RDY window. However, the I²C controller may wish to force a communication window to open, especially when the IQS370 device’s communication is in event mode. When the communication window is closed, i.e., RDY is high, the I²C controller may write 0xFF to the device (as if it were a register address) to request a communication window as soon as possible.

The time before the requested window is opened depends on the current state of the IQS370 device and its configured settings.

This behaviour is illustrated in Figure 10.7.

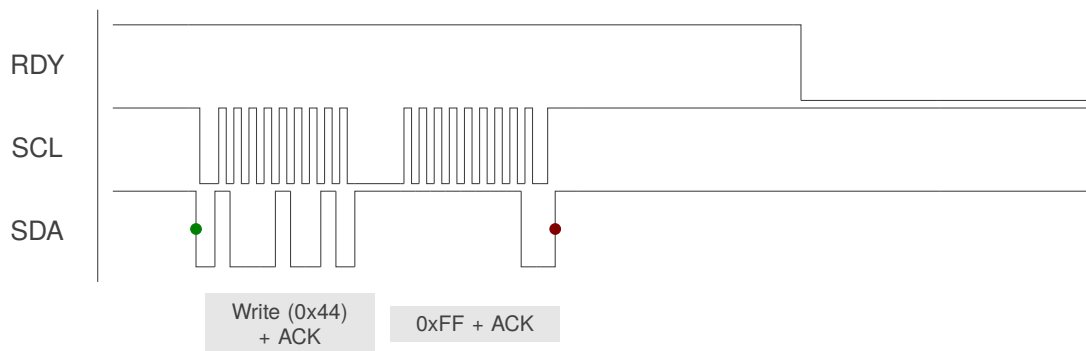


Figure 10.7: Forcing the Communication Window While it is Closed

10.14 Multiple Devices and Custom I²C Addresses

Multiple IQS370 devices may be connected to the same I²C bus if the following procedures are followed. Since RDY briefly acts as a reset line on startup, the master controller may utilise power-line reset circuitry to ensure that the devices can be held in their reset states on boot. During this time, the devices held in reset will not respond to I²C communication.

An example power-line reset circuit is shown in Figure 10.8, where the reset circuitry is implemented with P-channel MOSFETs. An additional MOSFET is used to discharge the capacitors connected to the IQS370 power lines. Without this discharging circuit, a significant waiting time may be required before all connected devices are guaranteed to be reset as a result of the power line disconnecting.

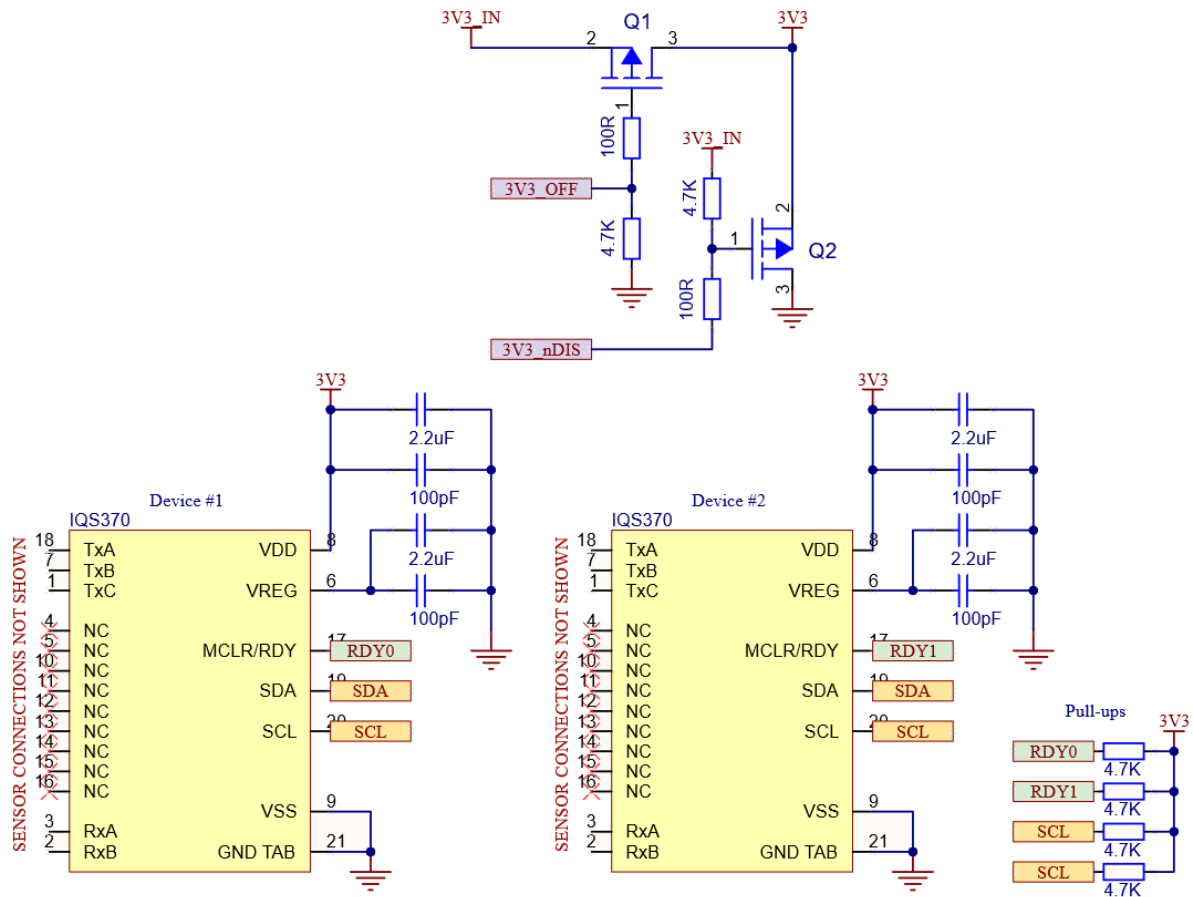


Figure 10.8: Example Schematic for Connecting Multiple IQS370 Devices to Same I²C Bus

An example control signal for assigning custom I²C addresses to multiple IQS370 devices connected to the same bus is shown in Figure 10.9. Refer to Section 10.3 for more information on how to change the I²C address of a specific device. It is recommended to only assign even addresses (e.g., 0x20, 0x22, 0x46, etc.) and avoid the use of the default I²C address (0x44).

If any device resets at any stage of operation (see Section 10.1), the entire I²C address assignment procedure should be repeated from the start.

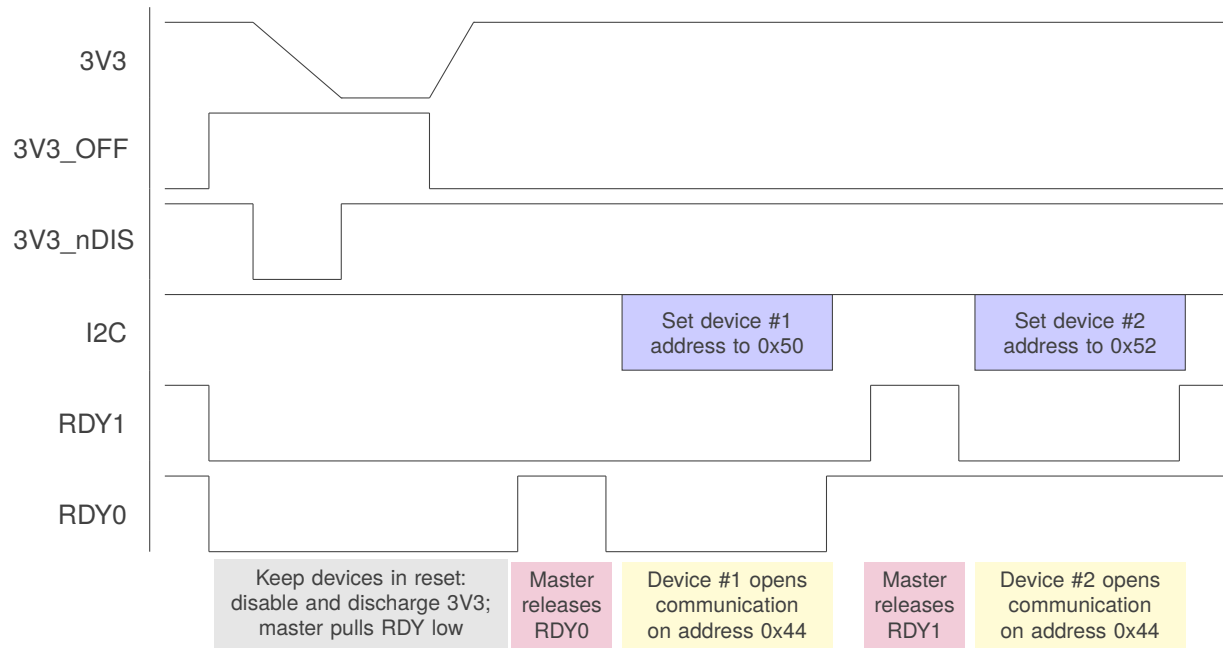


Figure 10.9: An Example of Multiple Device I²C Address Configuration, Based on the Example Schematic in Figure 10.8



11 I²C Memory Map

Table 11.1: I²C Memory Map

Address	Description	Default	Data Type
Read-Only	Version Information		
0x00	Product Number	2742	u16
0x01	Major Version	1	u16
0x02	Minor Version	2	u16
0x03 – 0x09	Reserved	-	u16[7]
Read-Only	Output Data		
0x10	Status	-	Appendix A.1
0x11	Position	-	u16
0x12	Angle _{LUT}	-	u16
0x13	Angle	-	u16
0x14	sin _{norm}	-	i16
0x15	cos _{norm}	-	i16
Read-Only	Intermediate Data		
0x20	sin ⁺	-	u16
0x21	sin ⁻	-	u16
0x22	cos ⁺	-	u16
0x23	cos ⁻	-	u16
0x24	sin _{lin} ⁺	-	i16
0x25	sin _{lin} ⁻	-	i16
0x26	cos _{lin} ⁺	-	i16
0x27	cos _{lin} ⁻	-	i16
0x28	Low-power Reference	-	u16
0x29	Low-power Counts	-	u16
Read-Write	General Settings		
0x30	System Control	0x0000	Appendix A.2
0x31	Normal Power Report Rate (ms)	0x000A	u16
0x32	Low-power Report Rate (ms)	0x0096	u16
0x33	Movement Timeout (ms)	0x03E8	u16
0x34	Transaction Timeout (ms)	0x00C8	u16
Read-Write	Conversion Settings		
0x40	Excitation Frequency	0x0200	Appendix A.3
0x41	Max Counts	0x1275	Appendix A.4
0x42	Reserved	0x008D	u16
0x43	Pin Selection	0x0000	Appendix A.5
0x44	Differential Polarity	0x0000	Appendix A.6
0x45	Stabilisation Times	0x0005	Appendix A.7
0x46	Low-power Reference Sample Skip	0x0004	Appendix A.8
0x47	Multipliers and Dividers	0x5EE3	Appendix A.9
0x48	Compensation	0x0000	Appendix A.10
0x49	Base	0x0190	u16
0x4A	Target	0x0190	u16



Table 11.1: I²C Memory Map (Continued)

Read-Write	DSP Settings		
0x60	General Processing Settings	0x0502	Appendix A.11
0x61	Events Mask	0x000E	Appendix A.12
0x62	Movement Threshold	0x0005	u16
0x63	Betas	0x0206	Appendix A.13
0x64	Reserved	0x0104	u16
0x65	Fast Angle Beta Threshold	0x0064	u16
0x66	Linearisation Multiplier	0x0040	u16
0x67	Resolution	0x00FF	u16
Read-Write	Calibration Data		
0x70	Sin Max	0x8000	i16
0x71	Sin Min	0x7FFF	i16
0x72	Cos Max	0x8000	i16
0x73	Cos Min	0x7FFF	i16
0x74	Cos Offset 0	0x0000	i16
0x75	Cos Offset 1	0x0000	i16
0x76	Angle Max	0x7FFF	u16
0x77	Angle Min	0x0000	u16
Read-Write	Lookup Table		
0x80	LUT Size	0x0000	Appendix A.14
0x81 – 0x91	LUT[0] – LUT[16]	-	u16[17]
Read-Write	Custom I ² C Address		
0xB0	Reserved	0x00	u16
0xB1	I ² C Address	0x44	Appendix A.15



12 Ordering Information

12.1 Ordering Code

Table 12.1: Order Code Description

IQS370 zzz ppb

IC NAME			IQS370
CONFIGURATION	zzz	=	001 I ² C inductive slider / rotary encoder
PACKAGE TYPE	pp	=	QF QFN-20 Package
BULK PACKAGING	b	=	R QFN-20 Reel (2000 pcs/reel)

12.2 Top Marking

12.2.1 QFN20 Package Marking Options

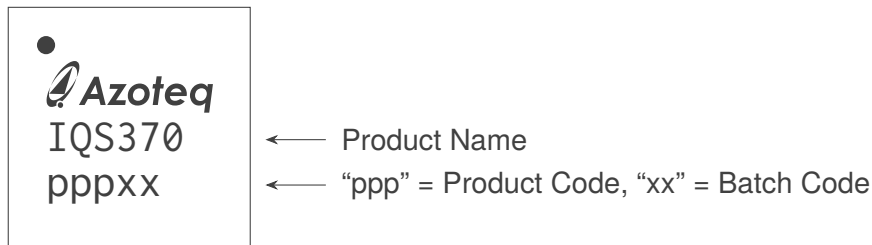


Figure 12.1: IQS370-QFN20 Package Top Marking

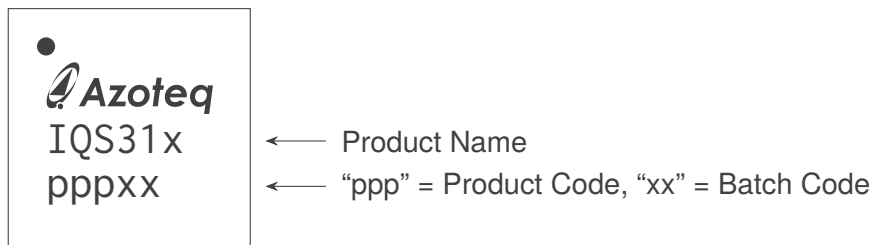


Figure 12.2: IQS31x-QFN20 Package Top Marking

13 Package Specification

13.1 Package Outline Description – QFN20

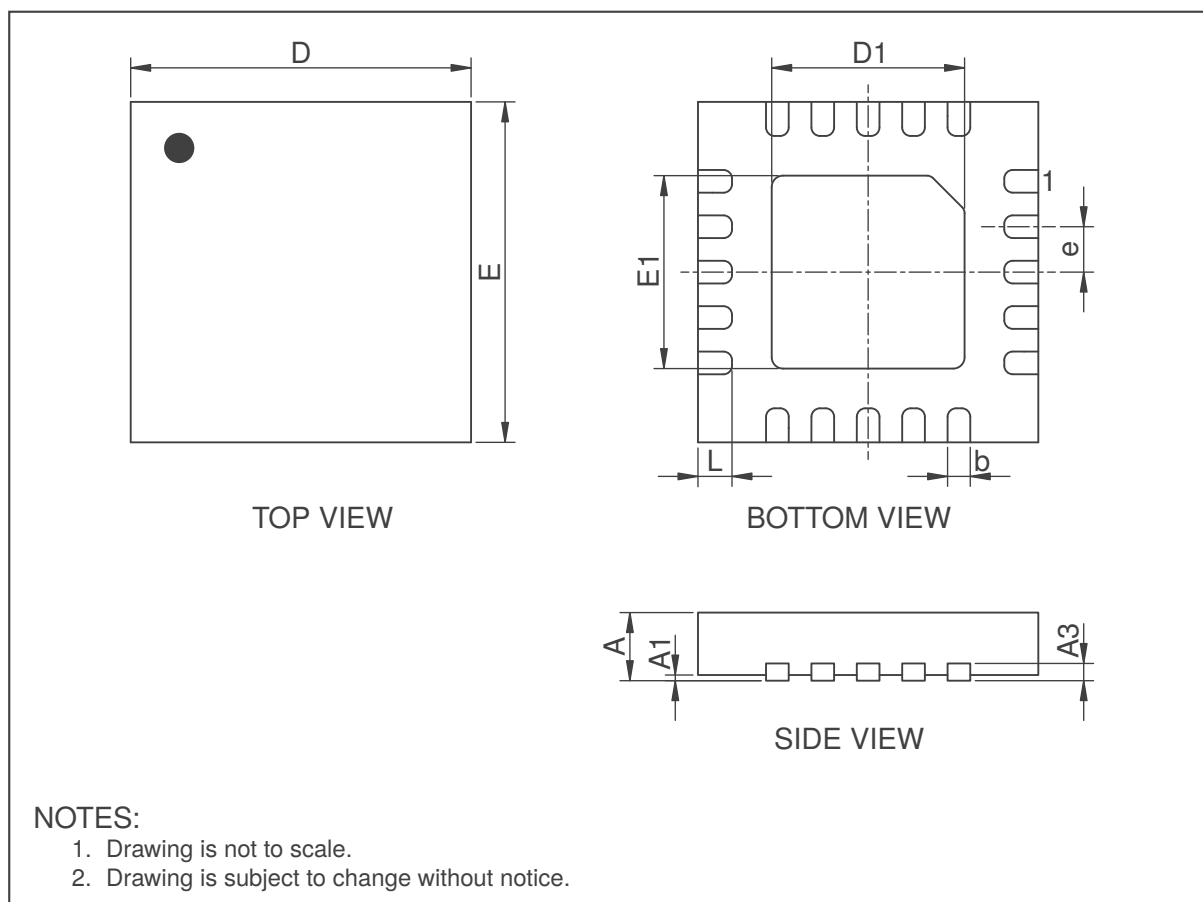


Figure 13.1: QFR (3x3)-20 Package Outline Visual Description

Table 13.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3	0.152 REF		
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.40 BSC		
L	0.25	0.30	0.35

13.2 Package Footprint Description – QFN20

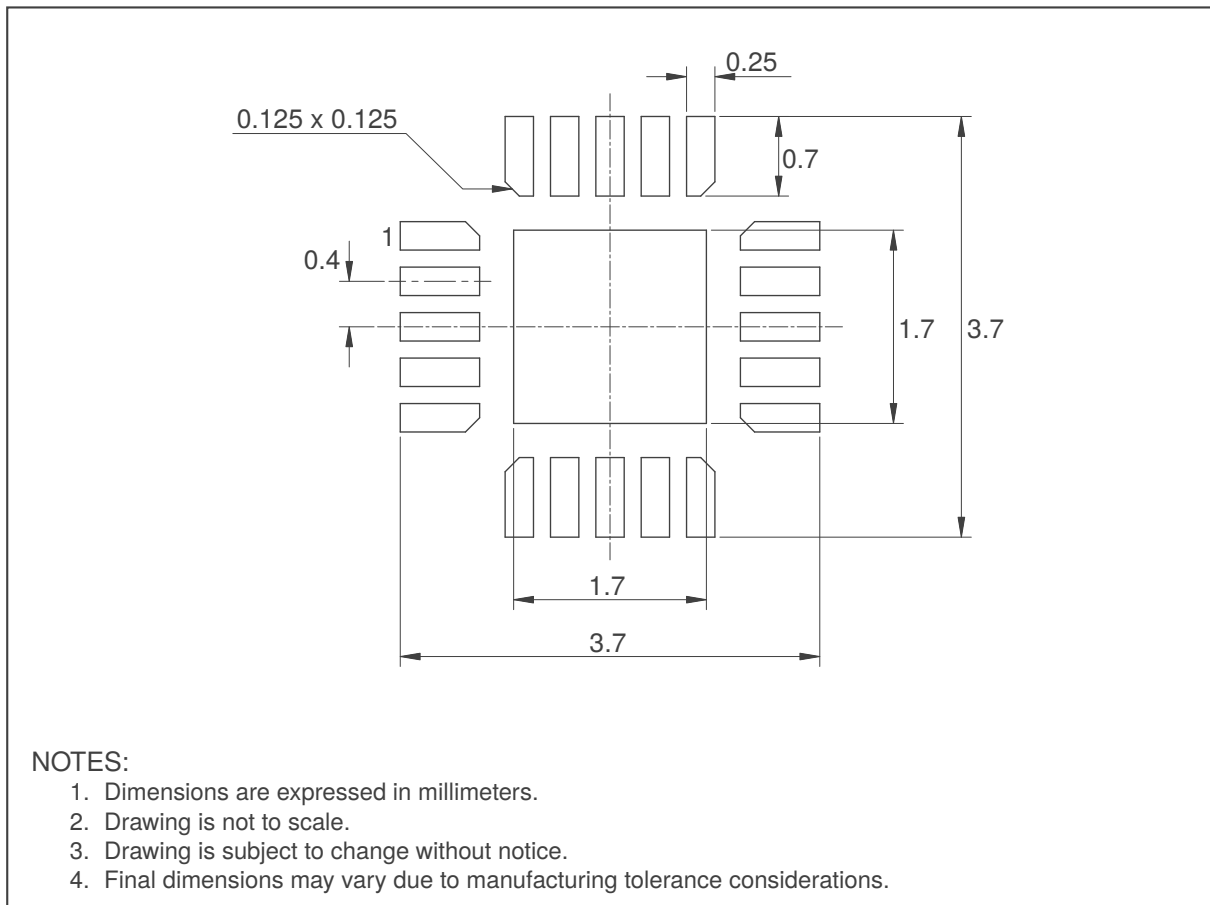


Figure 13.2: QFN20 Recommended Footprint

13.3 Tape and Reel Specifications

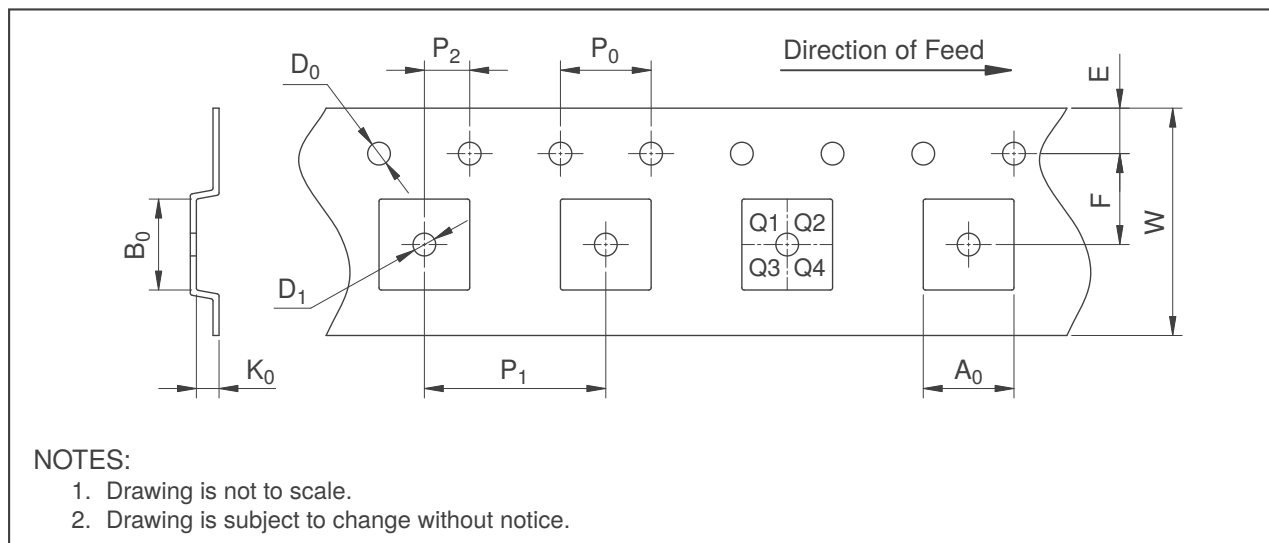
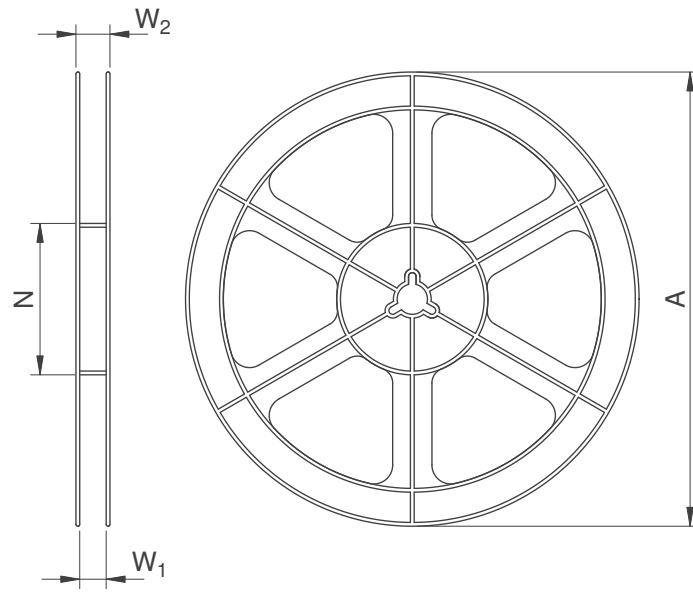


Figure 13.3: Carrier Tape Specification

Table 13.2: Carrier Tape Dimensions [mm]

Dimension	Package QFN20
A ₀	3.30
B ₀	3.30
K ₀	0.75
D ₀	1.50
D ₁	1.55
E	1.75
F	5.50
P ₀	4.00
P ₁	8.00
P ₂	2.00
W	12.00
Pin 1 Quadrant	Q2



NOTES:

1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 13.4: Reel Specification

Table 13.3: Reel Dimensions [mm]

Dimension	Package QFN20
A	178
N	60
W ₁	12.4
W ₂ (Max)	18.4



A Memory Map Descriptions

A.1 System Status (0x10)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							
Bit	7	6	5	4	3	2	1	0
Description	Reserved		Current Power Mode		Movement	Reserved	Power	Reset

- > Bit 4-5: **Current Power Mode**
 - 0: Normal
 - 1: Low
- > Bit 3: **Movement**
 - 0: No movement detected
 - 1: Movement detected — threshold defined by [Movement Threshold \(0x62\)](#)
- > Bit 1: **Power**
 - 0: No automatic power switch occurred
 - 1: Automatic power switch occurred
- > Bit 0: **Reset**
 - 0: No reset occurred
 - 1: Device reset occurred, cleared by Ack Reset (Appendix A.2)

A.2 System Control (0x30)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							Enable Conversions
Bit	7	6	5	4	3	2	1	0
Description	Range Calibration	Differential Counts Calibration	Do ATI	I ² C Interface Type	Power Mode Select		Soft Reset	Ack Reset

- > Bit 8: **Enable Conversions**
 - 0: Disabled
 - 1: Enabled
- > Bit 7: **Range Calibration**
 - 0: Disabled
 - 1: Enabled
- > Bit 6: **Differential Counts Calibration**
 - 0: Disabled
 - 1: Enabled
- > Bit 5: **Do ATI**
 - 0: Do Not Perform ATI
 - 1: Perform ATI (cleared on completion)
- > Bit 4: **I²C Interface Type**
 - 0: I²C Streaming — communicate after every sample
 - 1: I²C Event — communicate on detected movement only
- > Bit 2-3: **Power Mode Select**
 - 0: Normal
 - 1: Low (Forced)
 - 2: Automatic



- > Bit 1: **Soft Reset**
 - 0: Do not perform a software device reset
 - 1: Perform a software device reset
- > Bit 0: **Ack Reset**
 - 0: Do not acknowledge reset event
 - 1: Clear/acknowledge reset event (see Appendix A.1)

A.3 Excitation Frequency (0x40)

Bit	15	14	13	12	11	10	9	8
Description	Excitation Frequency							
Bit	7	6	5	4	3	2	1	0
Description	Reserved							

- > Bit 8-15: **Excitation Frequency**
 - 1: 3.50 MHz
 - 2: 2.33 MHz (Default)
 - 3: 1.75 MHz
 - 4: 1.40 MHz
 - 6: 1.00 MHz

A.4 Max Counts (0x41)

Bit	15	14	13	12	11	10	9	8
Description	0x12							
Bit	7	6	5	4	3	2	1	0
Description	Max Counts		0x35					

- > Bit 6-7: **Max Counts**
 - 0: 1023
 - 1: 2047
 - 2: 4095
 - 3: 16383

A.5 Pin Selection (0x43)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							Rx Pin Select
Bit	7	6	5	4	3	2	1	0
Description	Reserved		Tx C		Tx B		Tx A	

- > Bit 8: **Rx Pin Select**
 - 0: Rx A – Sin / Rx B – Cos
 - 1: Rx A – Cos / Rx B – Sin
- > Bit 4-5: **TxC**
 - 0: Inactive
 - 1: Vb
 - 2: Tx+
 - 3: Tx-



- > Bit 2-3: **TxB**
 - 0: Inactive
 - 1: Vb
 - 2: Tx+
 - 3: Tx-
- > Bit 0-1: **TxA**
 - 0: Inactive
 - 1: Vb
 - 2: Tx+
 - 3: Tx-

A.6 Differential Polarity (0x44)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							Cos Polarity

Bit	7	6	5	4	3	2	1	0
Description	Reserved							Sin Polarity

- > Bit 8: **Cos Polarity**
 - 0: Inverted
 - 1: Not inverted
- > Bit 0: **Sin Polarity**
 - 0: Inverted
 - 1: Not inverted

A.7 Stabilisation Time (0x45)

Bit	15	14	13	12	11	10	9	8
Description	Fine							

Bit	7	6	5	4	3	2	1	0
Description	Coarse							

- > Bit 8-15: **Fine**
 - The number of microseconds divided by 10
- > Bit 0-7: **Coarse**
 - Stabilisation time in milliseconds (max 200)

A.8 Low-power Reference Sample Skip (0x46)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Low-power Temp Track Sample Skip							

- > Bit 0-7: **Low-power Reference Sample Skip**
 - 8-bit value



A.9 Multipliers and Dividers (0x47)

Bit	15	14	13	12	11	10	9	8
Description	P-Multiplier		P-Divider					N-Multiplier

Bit	7	6	5	4	3	2	1	0
Description	N-Multiplier			N-Divider				

- > Bit 14-15: **Fine Multiplier**
 - 2-bit value
- > Bit 9-13: **Fine Divider**
 - 5-bit value
- > Bit 5-8: **Coarse Multiplier**
 - 4-bit value
- > Bit 0-4: **Coarse Divider**
 - 5-bit value

A.10 Compensation (0x48)

Bit	15	14	13	12	11	10	9	8
Description	Divider					Reserved	Select	

Bit	7	6	5	4	3	2	1	0
Description	Select							

- > Bit 11-15: **Divider**
 - 5-bit value
- > Bit 0-9: **Select**
 - 10-bit value

A.11 General Processing Settings (0x60)

Bit	15	14	13	12	11	10	9	8
Description	Wake Up Threshold							

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Enable Lookup Table	Oversampling		Linearise	Reserved

- > Bit 8-15: **Wake Up Threshold**
 - 8-bit value
- > Bit 4: **Enable Lookup Table**
 - 0: LUT bypassed
 - 1: LUT enabled
- > Bit 2-3: **Oversampling**
 - 0: 1x (None)
 - 1: 2x
 - 2: 4x
 - 3: 8x
- > Bit 1: **Linearise**
 - 0: Raw counts used directly
 - 1: 1/x linearisation applied to raw counts



A.12 Events Mask (0x61)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							
Bit	7	6	5	4	3	2	1	0
Description	Reserved						Power	Reserved

> Bit 1: **Power**

- 0: Power events do not open communication windows in I²C event mode
- 1: Power events open communication windows in I²C event mode

A.13 Betas (0x63)

Bit	15	14	13	12	11	10	9	8
Description	Fast Beta							
Bit	7	6	5	4	3	2	1	0
Description	Slow Beta							

> Bit 8-15: **Fast Beta**

- 8-bit value

> Bit 0-7: **Slow Beta**

- 8-bit value

A.14 LUT Size (0x80)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							
Bit	7	6	5	4	3	2	1	0
Description	LUT Size							

> Bit 0-7: **LUT Size**

- 0: 2 Points
- 1: 3 Points
- 2: 5 Points
- 3: 9 Points
- 4: 17 Points

A.15 I²C Address (0xB1)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							
Bit	7	6	5	4	3	2	1	0
Description	Reserved	I ² C Address						

> Bit 0-6: 7-bit I²C address



B Revision History

Release	Date	Changes
v 1.0	July 2025	Initial release
v 1.1	November 2025	Updated order code number
v 1.1.1	November 2025	Removed restricted watermark



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