



# **IQS324 Datasheet**

Off-Axis Hall-Rotation Sensor With Adjustable Interval UI and Inductive/Capacitive ProxFusion<sup>®</sup> Channel.

#### **1** Device Overview

The IQS324 ProxFusion<sup>®</sup> IC is a sensor fusion device for rotation and angle sensing applications using a diametrically-polarised magnet in an off-axis configuration. The included ProxFusion<sup>®</sup> channel can be used for integrated UI applications or as a wake-up channel.

#### 1.1 Main Features

- > Highly Flexible ProxFusion<sup>®</sup> Device
- > Hall-Effect Angle Sensor
  - 4 Hall plates
  - Off-axis orientation
  - 16-bit absolute angle output
  - <1° angle error<sup>i</sup>
  - · Wide operational range
  - Automatic Tuning Implementation (ATI)
  - Automatic synchronisation with mechanical ratchets
- > ProxFusion<sup>®</sup> Channel
  - Supports self-capacitive or inductive sensing
  - Automatic Tuning Implementation (ATI)
  - Button UI to detect large changes
  - Movement UI to detect small/rapid changes
- > Interval UI
  - Configurable number of intervals per rotation
  - · Configurable hysteresis between intervals
- > I<sup>2</sup>C Interface With IRQ/RDY Signal
- > Design Simplicity
  - PC software for configuration and debugging
  - Guidelines for magnet selection and mechanical constraints
- > Supply Voltage: 1.8 V to 3.6 V
- > QFN20 Package (3 × 3 × 0.5 mm) 0.4 mm pitch

### 1.2 Applications

- > Scroll wheels and thumb wheels for computer peripherals
- > Applications requiring flexible UI options with sensor fusion
- > Mechanical and optical rotary encoder replacements
- > Adjustment and control knobs

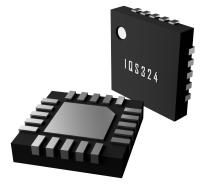


Figure 1.1: IQS324 QFN20 Package

Dependent on magnet alignment and mechanical tolerances



#### 1.3

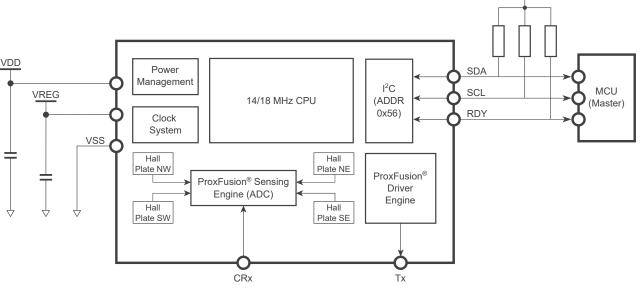


Figure 1.2: IQS324 Block Diagram





# Contents

1	Device Overview       -         1.1       Main Features       -         1.2       Applications       -         1.3       Block Diagram       -
2	Hardware Connections       6         2.1       QFN20 Pinout
3	Electrical Specifications       9         3.1       Absolute Maximum Ratings       9         3.2       General Operating Conditions       9         3.3       Recommended Operating Conditions       9         3.4       ProxFusion <sup>®</sup> Electrical Characteristics       10         3.5       ESD Rating       10         3.6       Reset Levels       10         3.7       Digital I/O Characteristics       10         3.8       I <sup>2</sup> C Characteristics       11         3.9       Current Consumption       11         3.9.1       Current Consumption With Two Active Hall Plates       12         3.9.2       Current Consumption With Four Active Hall Plates       12
4	ProxFusion® Hall Sensor Module       14         4.1       Magnet Orientation       14         4.2       Hall Rotation Measurements       15         4.3       Hall Rotation Channels       16         4.3.1       Hall Plate Selection       16         4.3.2       Hall Differentials and Phase Angle       16         4.3.3       Calculating the Phase Angle       17         4.4       Automatic Tuning Implementation (ATI)       17         4.4.1       Runtime ATI       18         4.5       Filtering       18         4.6.1       Interval Hysteresis       18         4.7       High-Accuracy Mode       19         4.8       Stationary Detection       19         4.9       Angle Offset Compensation       19         4.10       Automatic Interval Centering       19
5	Hall Normalisation       22         5.1       Normalisation Settings       22         5.2       Factory Calibration       22         5.2.1       Hall Runtime ATI       22
6	ProxFusion <sup>®</sup> Channel         24           5.1         Sensing Modes         24           5.2         Counts         24           6.2.1         Counts Linearisation         24





	6.3	Button Event Detection       24         6.3.1       Long-Term Average       25         6.3.2       Direction       25         6.3.3       LTA Reseeding       26
	6.4	Movement Event Detection       26         6.4.1       Long-Term Average       26         6.4.2       Movement Flags       27
	6.5 6.6 6.7 6.8	Dormancy       27         Automatic Tuning Implementation       27         Automatic Re-ATI       27         Debouncing and Hysteresis       28
7	<b>Powe</b> 7.1 7.2	Options         29           Power Modes         29           AutoProx         30           7.2.1         AutoProx Limits         31           7.2.2         AutoProx Update Rate         31
8	Additi 8.1 8.2 8.3 8.4	Sphal Features         32           Debug and Display Software (GUI)         32           Main Oscillator         32           Watchdog Timer (WDT)         32           Reset         32           8.4.1         Reset Indication         32           8.4.2         Software Reset         33
9	<b>I<sup>2</sup>C In</b> 9.1 9.2 9.3 9.4 9.5 9.6 9.7 9.8 9.9 9.10 9.11	arface       34         l <sup>2</sup> C Module Specification       34         l <sup>2</sup> C Address       34         l <sup>2</sup> C Address       34         9.2.1 Reserved l <sup>2</sup> C Address       34         l <sup>3</sup> C Compatibility       34         Memory Map Addressing       34         Memory Map Data       34         RDY/IRQ       34         Read and Write Operations       35         9.7.1 l <sup>2</sup> C Read From Specific Address       35         9.7.2 l <sup>2</sup> C Write To Specific Address       35         9.7.3 Modifying Bits Over l <sup>2</sup> C       36         1 <sup>2</sup> C Timeout       36         1 <sup>2</sup> C Timeout       36         1 <sup>2</sup> C Timeout       37         Stational Communication       37         Station
10	12014	9.11.2 Force Communication
		mory Map 39
11	11.1	ng Information45Ordering Code45Top Marking45
12	Packa	ge Information 46





	12.1 12.2	QFN20 Package Outline	46 48
	12.3	Tape and Reel Specifications	49
Α	Memo	ory Map Descriptions	50
	A.1	System Commands (0x1000)	50
	A.2	Power Settings (0x1001)	50
	A.3	Event Masks (0x1002)	51
	A.4	ULP and Watchdog Settings (0x1003)	51
	A.5	ProxFusion Settings 0 (0x1014)	52
	A.6	ProxFusion Settings 1 (0x1015)	52
	A.7	Button Debounce (0x1024)	52
	A.8	Movement Debounce (0x1028)	53
	A.9	ProxFusion Dividers (0x1032)	53
	A.10	Hall Dividers (0x103E)	53
	A.11	Hall Plate Settings (0x1044)	54
	A.12	Hall General Settings (0x1045)	54
	A.13	Hall Init Length (0x1047)	54
	A.14	Rotation UI Settings (0x1062)	55
	A.15	Normalisation Mode (0x1075)	55
	A.16	Power Mode Flags (0x2000)	55
	A.17	Device Status (0x2001)	55
	A.18	Hall Flags (0x2002)	56
	A.19	Event Flags (0x2003)	56
	A.20	Proxfusion States (0x2004)	56
	A.21	Button Event Flags (0x2006)	57
	A.22	Movement Event Flags (0x2007)	57
В	Know	n Issues	58
	B.1	Soft Reset During Force Comms	58
	B.2	Force Communication Request may Close a Communication Window	58
С	Revis	ion History	60





### 2 Hardware Connections

# 2.1 QFN20 Pinout

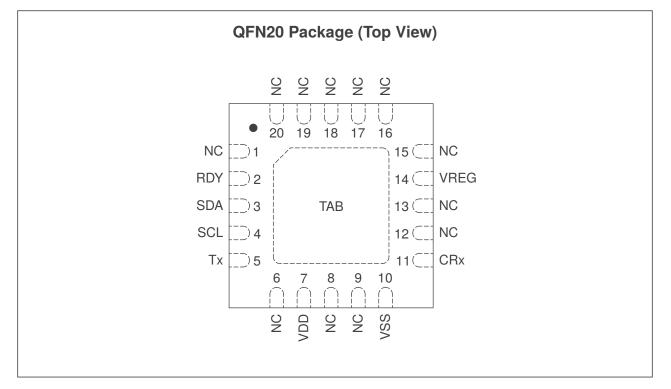


Figure 2.1: QFN20 Pinout

Pin	Name	Type <sup>i</sup>	Function	Description	
2	RDY	0	GPIO	I <sup>2</sup> C interrupt request	
3	SDA	I/O	12C	I <sup>2</sup> C data	
4	SCL	I/O	12C	I <sup>2</sup> C clock	
5	Тx	0	ProxFusion <sup>®</sup>	ProxFusion® inductive Tx pad	
7	VDD	Р	Power	Power supply input voltage	
10	VSS	Р	Power	Analog/digital ground	
11	CRx	I	ProxFusion <sup>®</sup>	ProxFusion <sup>®</sup> sensing pad	
14	VREG	Р	Power	Internally-regulated supply voltage	
*	NC	-	_	Not Connected	

#### Table 2.1: QFN20 Pin Descriptions

<sup>i</sup> Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power



# 2.2 **QFN20 Hall Plate Positions**

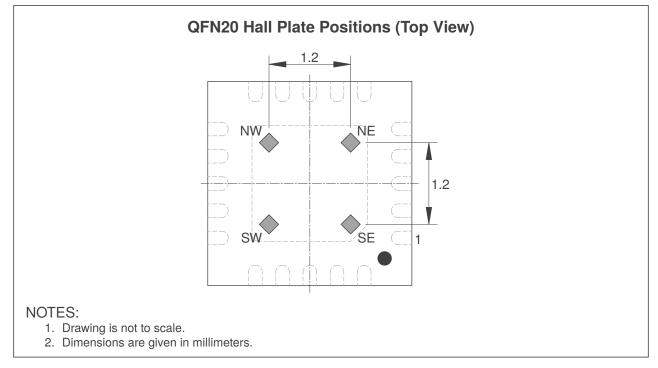
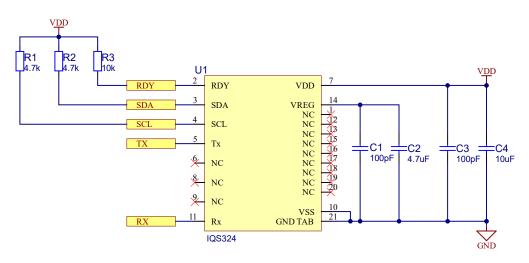


Figure 2.2: QFN20 Hall Plate Positions

# 2.3 Reference Schematic





### 2.3.1 RF Immunity

The IQS324 offers some immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on VREG and VDD.

Place a 100 pF in parallel with the 4.7  $\mu$ F ceramic capacitor on VREG. Place a 10  $\mu$ F ceramic capacitor on VDD, along with an optional parallel 100 pF capacitor. All decoupling capacitors should be placed as close as possible to the VDD and VREG pads.



If needed, series resistors can be added to the Rx electrodes that are used to reduce RF coupling into the sensing pads. Normally, these are in the range of  $100 \Omega$  to  $1 k\Omega$ .

PCB ground planes also improve noise immunity.





### **3** Electrical Specifications

### 3.1 Absolute Maximum Ratings

#### Table 3.1: Absolute Maximum Ratings

Symbol	Rating	Min	Мах	Unit
V <sub>DD</sub>	Voltage applied at VDD pin (referenced to VSS)	-0.3	3.6	V
V	Voltage applied to any ProxFusion <sup>®</sup> pin (referenced to VSS)	-0.3	V <sub>REG</sub>	V
V <sub>IN</sub>	Voltage applied to any other pin (referenced to VSS)	-0.3	V <sub>DD</sub> + 0.3 (3.6 V max)	V
T <sub>stg</sub>	Storage temperature	-40	85	°C

### 3.2 General Operating Conditions

#### Table 3.2: General Operating Conditions

Symbol	Parameter	Condition	Тур	Unit
E	Maatar alaak fraguanay	$F_{CLK} = 14 MHz$	14	MHz
FCLK	F <sub>CLK</sub> Master clock frequency		18	IVITIZ
F <sub>PROX</sub>	ProxFusion <sup>®</sup> engine clock frequency		F <sub>CLK</sub>	MHz
V	Internally-regulated supply output	$F_{CLK} = 14 MHz$	1.53	V
V <sub>REG</sub>		$F_{CLK} = 18 MHz$	1.8	V

### 3.3 Recommended Operating Conditions

#### Table 3.3: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Rec <sup>i</sup>	Мах	Unit
V	Standard operating voltage,	$F_{CLK} = 14 MHz$	1.71		3.6	V
V <sub>DD</sub>	applied at VDD pin	$F_{CLK} = 18 MHz$	2.2			v
T <sub>A</sub>	Operating free-air temperature		-20		85	°C
C <sub>VDD</sub>	Recommended capacitor at VDD		C <sub>VREG</sub>	2×C <sub>VREG</sub>		μF
C <sub>VREG</sub>	Recommended external buffer capacitor at VREG (ESR $\leq$ 200 m $\Omega$ )		2.2 <sup>ii</sup>	4.7	10	μF

<sup>i</sup> Recommended value

<sup>ii</sup> Absolute minimum allowed capacitance value is 1 μF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.



# 3.4 **ProxFusion<sup>®</sup> Electrical Characteristics**

Table 3.4: Recommended Operating Conditions for ProxFusion<sup>®</sup> Pins

Symbol	Parameter	Min	Max	Unit
Cx <sub>SELF-VSS</sub>	Capacitance between ground and external electrodes, in self-capacitance mode	1	400 <sup>i</sup>	pF
R <sub>Cx(SELF)</sub>	Series in-line resistance of self-capacitance electrodes	0	1 <sup>ii</sup>	kΩ

 $^{i}$  R<sub>Cx</sub> = 0  $\Omega$ 

<sup>ii</sup> Series resistance limit is a function of  $F_{xfer}$  and the circuit time constant, *RC*.  $R_{max} \times C_{max} = 1/(10 \times F_{xfer})$ , where *C* is the pin capacitance to VSS.

# 3.5 ESD Rating

#### Table 3.5: ESD Rating

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge voltage	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>i</sup>	±2000	V

<sup>i</sup> JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

## 3.6 Reset Levels

#### Table 3.6: Reset Levels

Para	Parameter		Max	Unit
V	Power-up (Reset trigger) - slope > 100 V/s	1.65		V
V <sub>DD</sub>	Power-down (Reset trigger) – slope < -100 V/s		0.9	V

## 3.7 Digital I/O Characteristics

#### Table 3.7: Digital I/O Characteristics

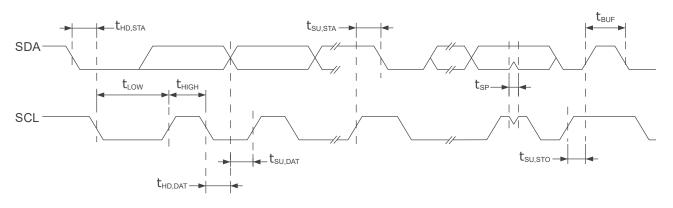
Paran	neter	Test Conditions	Min	Мах	Unit
V <sub>OL</sub>	SDA & SCL output low voltage	$I_{sink} = 20 \text{ mA}$		0.3	V
V OL	GPIO output low voltage	$I_{sink} = 10  mA$		0.15	V
V <sub>OH</sub>	Output high voltage	$I_{source} = 20  mA$	$V_{DD} - 0.2$		V
VIL	Input low voltage		V <sub>SS</sub> – 0.3	$0.3 \times V_{DD}$	V
V <sub>IH</sub>	Input high voltage		$0.7 \times V_{DD}$	$V_{DD} + 0.3$	V
	Output current sunk by any GPIO pin			10	
I <sub>GPIO</sub>	Output current sourced by any GPIO pin			20	mA
Cb	SDA & SCL bus capacitance			550	pF



# 3.8 I<sup>2</sup>C Characteristics

#### Table 3.8: I<sup>2</sup>C Characteristics

Parame	ter	Min	Max	Unit
f <sub>SCL</sub>	SCL clock frequency		1000	kHz
t <sub>HD,STA</sub>	Hold time (repeated) START condition	0.26		μs
t <sub>LOW</sub>	LOW period of the SCL clock	0.5		μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	0.26		μs
t <sub>SU,STA</sub>	Set-up time for a repeated START condition	0.26		μs
t <sub>HD,DAT</sub>	Data hold time	0		ns
t <sub>SU,DAT</sub>	Data set-up time	50		ns
t <sub>SU,STO</sub>	Set-up time for STOP condition	0.26		μs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	0.5		μs
t <sub>SP</sub>	Pulse duration of spikes suppressed by input filter	0	50	ns





## 3.9 Current Consumption

The current consumption of the IQS324 is highly dependent on the specific parameters configured during initialisation, as well as on the frequency and duration of  $I^2C$  communications. Therefore, the following tables serve as an illustration of the expected power consumption for similar configurations<sup>i</sup>. All measurements are taken with *Event Mode* enabled, without any sensor activations, and without any  $I^2C$  communications. All other settings, unless stated otherwise, are kept default.

Current consumption values are provided for both 14 MHz and 18 MHz  $F_{OSC}$  configurations. For more information, please refer to Section 8.2.

### 3.9.1 Current Consumption With Two Active Hall Plates

The following tables show the expected current consumption of the IQS324 in a diagonal off-axis configuration, where only two opposing corner Hall plates are sampled, as shown in Section 4.3.1.

<sup>&</sup>lt;sup>i</sup> These measurements are based on bench testing and have not been characterised over large volumes.



	Report Rate [ms]	Current Consumption [µA]		
Power Mode		Hall & Touch	Hall	Touch
High Accuracy	4	490	420	230
Normal Power	20	113	110	63
Low Power	100	24	24	14
Ultra Low Power	500	6	5.5	3.6
Auto Prox		N/A	2.1	1.5

#### Table 3.9: IQS324 Typical Current Consumption at 14 MHz F<sub>OSC</sub>

#### Table 3.10: IQS324 Typical Current Consumption at 18 MHz F<sub>OSC</sub>

		Current Consumption [µA]		
Power Mode	Report Rate [ms]	Hall & Touch	Hall	Touch
High Accuracy	4	480	470	290
Normal Power	20	124	114	67
Low Power	100	26	24	15
Ultra Low Power	500	7	6	4
Auto Prox		N/A	2.3	1.5

#### 3.9.2 Current Consumption With Four Active Hall Plates

The following tables show the expected current consumption of the IQS324 in a configuration that samples all four Hall plates. This applies to a "North-South" or "East-West" off-axis configuration.

Table 3.11: IQS324 Typical Current Consumption at 14 MHz F<sub>OSC</sub>

	Report Rate [ms]	Current Consumption [µA]		
Power Mode		Hall & Touch	Hall	Touch
High Accuracy	4	560	460	230
Normal Power	20	128	121	63
Low Power	100	27	27	14
Ultra Low Power	500	7	5.5	3.6
Auto Prox		N/A	2.2	1.5



Table 3.12: IQS324 Typica	l Current Consumption	n at 18 MHz F <sub>osc</sub>
---------------------------	-----------------------	------------------------------

		Current Consumption [µA]		
Power Mode	Report Rate [ms]	Hall & Touch	Hall	Touch
High Accuracy	4	650	500	280
Normal Power	20	142	124	67
Low Power	100	30	27	15
Ultra Low Power	500	8	6.2	4
Auto Prox		N/A	2.3	1.5



## 4 ProxFusion<sup>®</sup> Hall Sensor Module

The IQS324 contains four equally-spaced Hall plates that measure the magnetic field strength and orientation of a nearby diametrically polarised magnet. These Hall plates are used to calculate the relative angle of an off-axis magnet with regards to the IC. The angle can be divided into discrete intervals using the Interval UI, providing a convenient interface for scroll wheel applications.

# 4.1 Magnet Orientation

The IQS324 is designed to be used in an off-axis orientation with regard to the magnet. Figure 4.1 shows the recommended configuration for an off-axis Hall-rotation sensor. Here, the magnet is oriented diagonally relative to the IC, and two diagonal plates are used for the rotation sensing. This is generally recommended if off-axis is required, as it provides the largest phase angle.

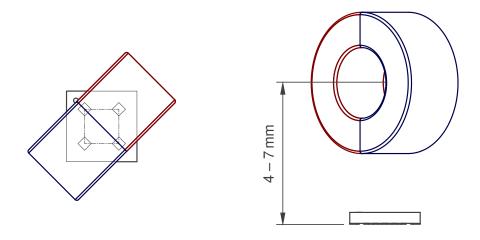


Figure 4.1: Recommended Magnet Orientation for an Off-Axis Angle Measurement Application

Figure 4.2 shows an alternate off-axis configuration that uses two plates per side to measure the Hall rotation. This configuration results in a smaller phase angle than when using the diagonal plates, and is thus only recommended for shorter distances between the magnet and IC.



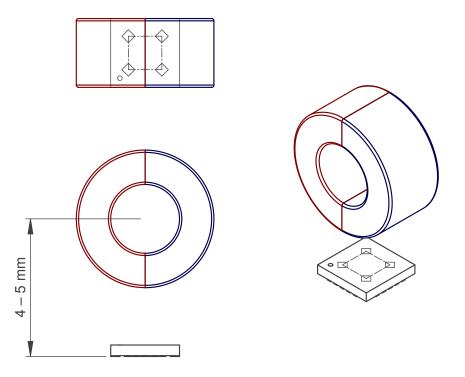


Figure 4.2: Alternate Magnet Orientation for Off-Axis Angle Measurement Applications

Please refer to Section 4.3.1 for settings related to off-axis configuration selections. Also refer to AZD127 for more information regarding off-axis design guidelines.

### 4.2 Hall Rotation Measurements

The IQS324 provides the angle measurement in three different values:

- > Absolute Angle: Raw angle measurement, provided as an unsigned 16-bit value, where the range [0, 65536) maps to [0°, 360°). This represents the angle of the magnet relative to the IC.
- > Processed Angle: Angle measurement after post-processing, also an unsigned 16-bit value. This output is filtered and includes an angular offset. This output can be used for applications requiring high-resolution measurements.
- > *Interval*: The output of the interval UI, which divides the unsigned 16-bit processed angle into several sections, or intervals. This output is recommended for applications with mechanical ratchets and is supplemented by the hysteresis and auto-zero features.

### 4.3 Hall Rotation Channels

The Hall-effect rotation measurement on the IQS324 relies on two measurements on each of the four Hall plates, where the second measurement is inverted to the first. These two measurements allow for the calculation of a reference value and a differential value, from which the relative strength of the magnetic field can be inferred. The reference value is calculated as the average of the two measurements, and the differential value is calculated as the difference between the measurements.

As a result, the IQS324 performs up to eight Hall-effect measurements, four of which are inverted to the others. These measurement values (channels) are available in the *Hall Plate Counts* and *Hall Reference* registers.



#### 4.3.1 Hall Plate Selection

By default, the IQS324 uses opposing diagonal plates to measure off-axis magnet rotation. Either pair can be selected by modifying the *Magnet Orientation* setting in the *Hall General Settings* register. The "diagonal axis" refers to the axis of rotation of the magnet. "NW to SE Axis" will use the NE and SW plates, and vice versa.

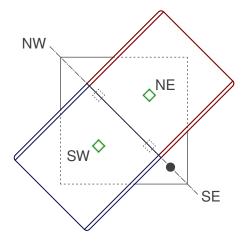


Figure 4.3: NW-SE Off-Axis Plate Selection

Alternatively, the "North-South (N-S)" or "West-East (W-E)" axes can be specified, which will use two pairs of plates to measure the off-axis rotation. "N-S" axis selection will use the East and West plates, and vice versa.

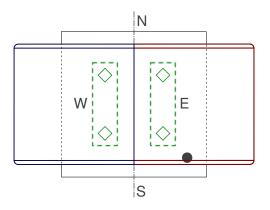


Figure 4.4: N-S Off-Axis Plate Selection

### 4.3.2 Hall Differentials and Phase Angle

For off-axis configurations, the Hall counts are combined into two *Hall Differential* signals, which are used to calculate the magnet's angle. The phase angle between these two signals, illustrated in Figure 4.5, are dependent on the geometry of the application. This phase angle must be calibrated, and set in the *Phase Angle* registers. With a measured phase angle,  $\theta$ , the register values must be set to:





Phase Angle Sin =  $65536 \times \sin(\theta)$ Phase Angle Cos =  $65536 \times \cos(\theta)$ 

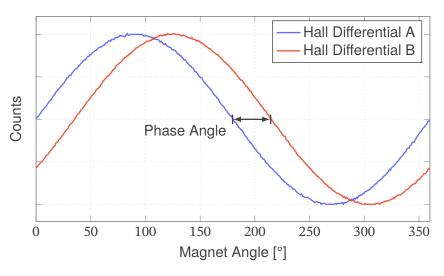


Figure 4.5: Hall Differential Signals

Off-axis applications typically have a smaller phase angle, in the range of 20° to 40°.

### 4.3.3 Calculating the Phase Angle

To calculate the phase angle of an off-axis magnet setup, the two Hall Differential signals must be recorded over at least one full rotation of the magnet. These signals then need to be normalised with:

$$A_{norm} = \frac{\frac{\max(A) - A}{A}}{\frac{\max(A) - \min(A)}{\min(A)}} \qquad B_{norm} = \frac{\frac{\max(B) - B}{B}}{\frac{\max(B) - \min(B)}{\min(B)}}$$

The data will now range between 0 and 1.

Sample both signals where  $A_{norm} \approx 0.5$ . With these values, the phase angle,  $\theta$ , can be calculated as:

$$\theta = \sin^{-1}(|B_{norm} - A_{norm}| \cdot 2)$$
 (where  $A_{norm} \approx 0.5$ )

### 4.4 Automatic Tuning Implementation (ATI)

ATI is an automatic sensor calibration algorithm that configures the *Hall Plate Offsets* to ensure accurate Hall-effect sensing for a range of different magnet sizes and strengths. The ATI aims to modify the Hall plate settings such that the Hall channel reference values are within the range defined by the *Target* and *ATI Band* parameters. Recommended value for the target is between 8000 and 14000.

The overall gain of the Hall sensing circuitry is controlled by three parameters:

- > Hall Amplifier Gain
- > Hall Dividers





#### > Hall Offsets

The first two parameters, Hall Amplifier Gain and Hall Dividers, must be chosen at design time. This can be done with the aid of the IQS324 GUI. Typically, the these can be chosen such that the Hall channels swing around ±2000 to ±4000 counts from the reference over a full rotation of the magnet. Once the gain parameters are chosen, they can be fixed for all modules across production. The ATI feature then uses the Hall Offset values to compensate automatically for any variation across production.

When tuning the Hall gain parameters, the Hall Amplifier Gain value (in the *Hall Plate Settings* register) can generally be set to a starting value of '1' (x2). Then, the Hall Dividers can be increased or decreased until the desired counts swing (±2000 to ±4000 counts) is achieved. Recommended Hall Divider values are given in Table A.2. It is generally recommended to keep the Hall Divider gain ratio lower than 1. If this provides insufficient gain, the Hall Amplifier Gain value should be increased as necessary.

#### 4.4.1 Runtime ATI

ATI is performed automatically at start-up, as well as when all the following criteria are met:

- > The stationary flag is set; see Section 4.8.
- > The *Hall Reference* of a channel is outside the threshold defined by Equation (1).

> Runtime ATI is enabled in *Hall UI Settings*.

### 4.5 Filtering

The IQS324 includes a dynamic angle filter that increases its bandwidth based on the magnet's current speed. This allows the filter to remove most high-frequency noise while the magnet is stationary, and prevents the filter from aliasing during high-speed rotations. The overall strength of the filter can be adjusted with the *Angle Filter Beta* value.

In Low and Ultra Low power modes, the *Low Power Beta* is used instead. This should be set to a *larger* value than the normal beta value, to reduce measured jitter at lower report rates.

### 4.6 Interval UI

The interval UI divides the 16-bit Processed Angle into a value between 0 and the *Number of Intervals*, where the size of each interval is defined as:

Interval Size = 
$$\frac{2^{16}}{\text{Number of Intervals}}$$
. (2)

This is especially useful for applications that do not require a high measurement resolution or that use mechanical ratchets.

#### 4.6.1 Interval Hysteresis

The Interval Hysteresis prevents the interval output from jittering between two intervals, causing unnecessary interval change events. The behaviour of the hysteresis is shown in Figure 4.6.

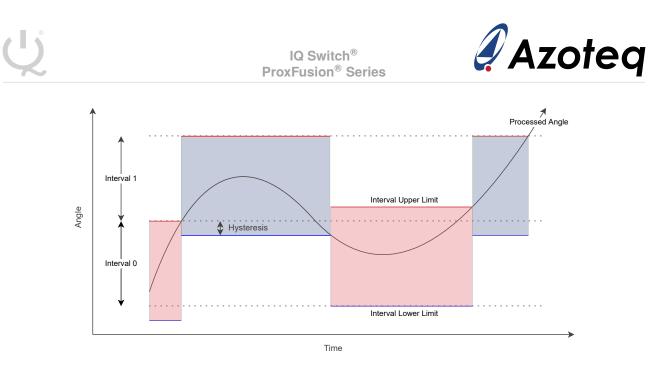


Figure 4.6: Illustration of the Interval Size and Interval Hysteresis

The amount of hysteresis applied can be modified by changing the *Interval Hysteresis* value. Hysteresis is a 16-bit value, in the same unit as the Processed Angle. Hysteresis should therefore be chosen based on the interval size calculated in the previous section, and on the amplitude of the noise on the Processed Angle.

### 4.7 High-Accuracy Mode

The High-Accuracy mode of the IQS324 will increase the report rate of the device to sample Hall rotation measurements more accurately and to reduce aliasing during high rotation rates. The IQS324 will enter High-Accuracy mode in the event of an interval change.

The *High-Accuracy* flag will remain set for the duration of the *High-Accuracy Timeout*. This flag is used to identify whether to transition into the High-Accuracy power mode and can be configured to signal an automatic interval centering event when High-Accuracy mode is exited.

## 4.8 Stationary Detection

The IQS324 will set a *Stationary* flag if no movement is detected during the period defined by the *Stationary Timeout* value. This Stationary flag is used to identify whether to go into a lower power mode. Runtime ATI for the Hall channels is also only executed when stationary.

## 4.9 Angle Offset Compensation

Angle offset compensation is applied to ensure the output angle corresponds to the angle of the wheel, rather than the raw angle of the magnet, as shown in Figure 4.7. This is especially important for ratchet applications, where the intervals generated by the IC must match the mechanically-defined intervals of the wheel.



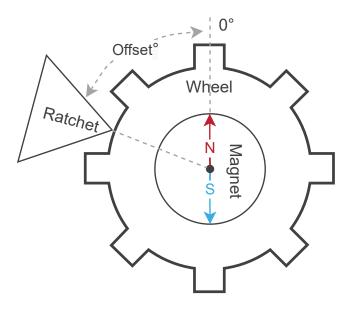


Figure 4.7: Illustration of the Absolute Angle Offset

The angle offset is updated when the *Zero* command in the *System Commands* register is set. This sets the Processed Angle to the centre of interval 0, and thus adjusts the angle offset accordingly. The *Zero* command is also set automatically on start-up.

The angle offset is also modified by the automatic interval centering functionality, to align the intervals with a mechanical ratchet automatically.

Finally, the angle offset can be manually changed via the *Angle Offset* register.

### 4.10 Automatic Interval Centering

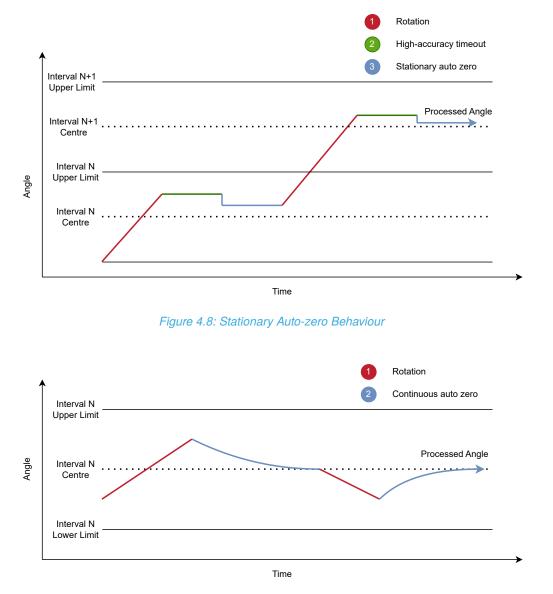
The interval centering functionality (or "auto-zero") of the IQS324 allows the device to modify the absolute angle offset of the Processed Angle such that the Processed Angle is at the centre of the current interval. This dynamically adjusts the absolute angle offset until the Processed Angle aligns with the physical intervals of a ratchet device.

The auto-zero functionality can be set to one of five different modes in the Hall UI Settings:

- > Off: The device will never allow an automatic interval zero action to happen, and the master device will have to send an instruction over I<sup>2</sup>C to set the Zero bit.
- Stationary: An auto-zero event will occur when the High-Accuracy timeout event occurs. A single adjustment is made to the absolute angle offset each time the device exits High-Accuracy mode. The *Auto-Zero Beta* parameter defines the size of the adjustment, with an auto-zero beta value of 0 resulting in a jump to the exact centre of the interval. This behaviour can be seen in Figure 4.8.
- > Continuous: The auto-zero filter will cause the Processed Angle to move continuously towards the centre of the current interval. It is recommended to use an auto-zero beta value of 10 or higher to allow the Processed Angle to move between intervals during slower rotations. This mode is recommended for devices without a mechanical ratchet. This behaviour can be viewed in Figure 4.9.



- Release: An auto-zero event will occur on a Movement Exit event on the ProxFusion channel. If the ProxFusion channel is configured as a capacitive touch channel, this exit event could indicate that the user released the device.
- > Continuous-Release: Performs auto-zero using Continuous mode, but only while the ProxFusion Button event is not in activation. This automatically adjusts the angle offset as long as the user is not interacting or touching the device.







# 5 Hall Normalisation

Off-axis magnet orientations require extremely tight mechanical tolerances to ensure accurate Hallrotation measurements. Magnet misalignments and wobble can result in differences in amplitudes of the measured magnetic field strengths across different Hall plates. To compensate for this, the IQS324 attempts to normalise the *Hall Differential* signals by tracking the minimum and maximum values of the Hall Differentials during runtime. These minimum and maximum values are then used to correct for differences in amplitude and DC offsets between the A and B Hall Differentials. Normalisation attempts to set the amplitude of the Differentials to approximately 16384 counts.

Min/max tracking is performed over the course of each full rotation, and the minimum and maximum values are stored in the *Normalisation Minimum/Maximum* registers. The resulting normalised Hall Differential signals are then stored in the *Normalised Hall Field* registers.

### 5.1 Normalisation Settings

Hall normalisation can be set to 'Off', 'Manual', or 'Auto'.

- > **Off:** Normalisation is disabled.
- Manual: The Hall Differential signals are normalised based on the values stored in the Normalisation Min/Max registers. However, these normalisation values are static. The IQS324 does not perform any tracking of minimum and maximum Differentials.
- > Auto: The IQS324 performs min/max tracking with each rotation, continuously updating these values to track and compensate for any changes that may be introduced due to environmental drift. The stored minimum and maximum values are filtered based on the *Normalisation Beta* value after each rotation. This is the default, and recommended, setting for off-axis configurations.

## 5.2 Factory Calibration

In 'Auto' normalisation mode, normalisation is only applied once valid (non-zero) minimum and maximum values have been measured. However, after start-up, these values are only seeded after completing a few full rotations. As a result, the first rotation after start-up may have lower accuracy than expected. In order to improve the accuracy of the Hall-rotation sensing from power-on, initial minimum and maximum normalisation values can be written to the IQS324. This requires a factory calibration procedure to measure, read, and store the nominal normalisation parameters. On all subsequent starts, these values can then be written to the IQS324.

The following factory calibration procedure is recommended:

- > Initialise the IQS324 over  $I^2C$  as normal, with the desired settings.
- > Perform an ATI by setting the *Hall ATI* bit in the *System Commands* register. This resets the minimum and maximum values to 0.
- > Wait for ATI to complete by waiting for the next communications (RDY) window.
- > Rotate the magnet by at least 540° (1.5 revolutions).
- > Read and store the values of the *Normalisation Minimum/Maximum* registers.

This calibration sequence only needs to be done once, during production. Once these compension values are known, they can be written to the IQS324 every time on start-up.

The following procedure is then recommended for normal operation:





- > Initialise the IQS324 over I<sup>2</sup>C as normal, with the desired settings.
- > Perform an ATI by setting the Hall ATI bit in the System Commands register.
- > Wait for ATI to complete by waiting for the next communications (RDY) window.
- > Disable the I<sup>2</sup>C read-only protection by setting the Disable Read-Only Check bit in the ULP and Watchdog Settings register to '1'.
- > Write the stored min/max values to the Normalisation Minimum/Maximum registers of the IQS324.
- > Re-enable the  $I^2C$  read-only protection.

#### 5.2.1 Hall Runtime ATI

Note that on the IQS324, the Normalisation minimum and maximum values are reset to 0 after any Hall ATI event. This means that these values may be unintentionally cleared during normal operation, during a runtime ATI.

This can be addressed in two ways:

- 1. Disable Hall Runtime ATI. This will prevent the IQS324 from doing ATI boundary checks. This may make the device more sensitive to environmental changes; however the Hall-rotation sensing is typically robust against these changes.
- 2. Monitor the *ATI Event* flag in the *Event Flags* register, and re-write the Normalisation min/max values to the device if an ATI event occurs.



# 6 **ProxFusion<sup>®</sup> Channel**

The IQS324 features a ProxFusion<sup>®</sup> sensing channel that uses Azoteq's patented on-chip ProxFusion<sup>®</sup> module to measure and process relative changes in capacitive and inductive sensors.

The channel provides two primary Event types – *Button* and *Movement* events. The Button event attempts to track slow changes and long term activations, whereas the Movement event detects smaller, fast changes. Each of these events store their own reference and delta values.

### 6.1 Sensing Modes

The ProxFusion<sup>®</sup> channel supports the following sensing modes:

- > Self-capacitive sensing
- > Resonated inductive sensing

The sensing mode can be modified in the *ProxFusion Settings 1* registers.

Please refer to the following application notes for more information:

- > AZD004: Overview of Azoteq's ProxFusion® Sensing
- > AZD115: Design Guidelines for Inductive Sensing
- > AZD125: Design Guidelines for Capacitive Touch Sensing

### 6.2 Counts

The ProxFusion<sup>®</sup> module reports a capacitance or inductance measurement as a relative, unit-less value referred to as "Raw Counts". These raw counts are related to the number of charge transfer cycles necessary to charge an internal sampling capacitor, and are typically inversely proportional to the signal measured on the external sensor.

#### 6.2.1 Counts Linearisation

The IQS324 does not directly use the "Raw Counts" obtained from the sensing module, but uses "Linearised Counts", which is calculated as

$$\text{Linearised Counts} = \frac{3276750}{\text{Raw Counts}}.$$
 (3)

All references to "Counts" in this datasheet, and in the I<sup>2</sup>C memory map, use these Linearised Counts values.

After linearisation, counts are filtered using a low-pass IIR filter to reduce the high-frequency noise in the measurement. The response of the filter can be adjusted with the *Counts Filter Beta* value in the *Filter Betas* registers. Higher beta values result in a slower filter response, with less noise on the channel.

### 6.3 Button Event Detection

The Button Event attempts to emulate the behaviour of a typical button, which stays in activation for as long as it is pressed.



#### 6.3.1 Long-Term Average

Button events are detected by comparing the filtered counts value to a reference value, known as the Long-Term Average (LTA). While the channel is not in activation, the LTA is slowly updated to track changes in the environment using a low-pass filter.

The difference between the filtered counts and the LTA is stored as the *Delta* value.

$$Delta = LTA - Counts$$
(4)

The delta is used to detect user interaction by comparing it to the *Button Threshold*. The channel enters the active state when the delta exceeds the threshold, and the *Button Active* bit in the *Button Events* register will be set.

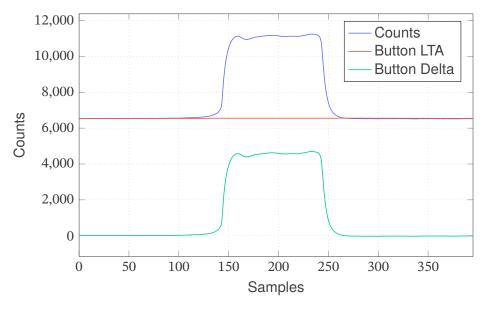


Figure 6.1: Button UI Activation

The LTA is then halted (kept constant) while the Button event is active, or while the delta exceeds the *LTA Halt Threshold*, as shown in Figure 6.1. The LTA Halt Threshold can typically be made smaller than the Button Threshold. This may help increase the sensitivity of the event detection during slower activations, preventing the LTA from drifting during user interaction.

The response of the LTA filter is controlled by the various *LTA Beta* values. The *LTA Beta* value sets the response of the filter during High-Accuracy and Normal power modes, whereas the *Low Power LTA Beta* is used during Low and Ultra-Low power modes. The Low Power Beta value should be set to a *larger* value than the Normal Beta value, to maintain adequate sensitivity at lower sampling rates.

### 6.3.2 Direction

Negative delta values are typically ignored, as they typically indicate an unexpected decrease in signal. If a negative delta value exceeds the *Fast LTA Bound* threshold, the LTA will be updated using the *Fast LTA Beta* filter. This behaviour can be disabled by setting the *Bi-Directional* bit, or the sign of the delta can be inverted by setting the *Inverse* bit in the *ProxFusion Settings 0* register.



### 6.3.3 LTA Reseeding

The reseed function of the device will replace the filtered counts and the long-term average value of the channel with the latest sampled counts value to reset the environmental reference of the channel. This may be necessary in certain instances when the Button event gets incorrectly stuck in an activation. Detection of stuck states is controlled by the *Button Timeout* parameter. If the Button event remains active for this timeout duration, the LTA is reseeded automatically. This behaviour can be disabled by setting the timeout parameter to 0.

A *Reseed* command can also be given manually by setting the corresponding bit in *System Commands*.

### 6.4 Movement Event Detection

The Movement Event detects small, rapid changes or movements on the ProxFusion channel. This may be used as a simple wake-up event, triggered as the user approaches the sensor.

#### 6.4.1 Long-Term Average

The Movement event tracks its own LTA and delta values, separately from the Button event. In contrast to the Button event, the Movement event does not halt its LTA. Instead, it filters using the regular LTA Beta value while not in activation, and filters with the Fast LTA Beta while the event is active (while the delta is larger than the *Movement Threshold*).

The purpose of this is to track increases in the rate of change of counts. This typically occurs as a user is approaching or releasing a proximity sensor. Outside of activations, the LTA is updated slowly to maximise sensitivity to changes in counts. As soon as the delta exceeds the threshold, the fast LTA is used to exit the movement event as quickly as possible, to be ready to detect the next change in counts. An example of the Movement's response to a quick tap is shown in Figure 6.2.

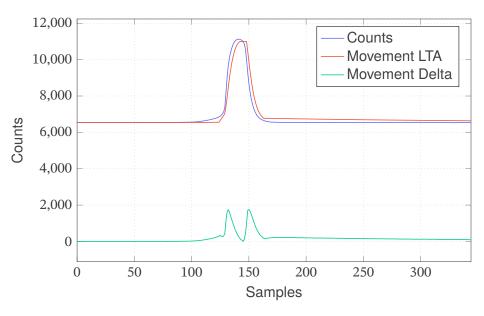


Figure 6.2: Movement UI Activation



#### 6.4.2 Movement Flags

The primary outputs of the Movement Event are the *Movement Entered* and *Movement Exited* flags in the *Movement Event Flags* registers. The Movement Entered flag is set while the delta exceeds the threshold with a positive sign, and indicates that a user approached the sensor, or entered touch. The Movement Exited flag is set while the delta exceeds the threshold with a negative sign, indicating that the user released the sensor. These flags can be flipped by setting the *Inverse* bit.

Note that the Movement event is not affected by the *Bi-Directional* setting.

During slower movements, the same flag may be set multiple times consecutively. For example, an Enter event may occur repeatedly as the user approaches the sensor.

#### 6.5 Dormancy

The touch dormancy flag will be set if the dormancy timeout event occurs after no touch input is received for the period defined in the *Dormancy Timeout* parameter. The IQS324 may only enter lower power states once the dormancy flag is set.

Note that the dormancy timer also acts as a timeout for the LTA Halt flag, if the channel's delta exceeds the LTA Halt Threshold while not in any active state. When dormancy is set, the LTA is reseeded, and will then continue to track environmental changes normally.

#### 6.6 Automatic Tuning Implementation

The ATI is a sophisticated technology implemented in ProxFusion<sup>®</sup> devices to allow optimal performance of the devices for a wide range of sensing electrode designs, without modification to external components.

The ATI functions by using the *Base* and *Target* parameters to calculate appropriate *Divider* and *Compensation* values to achieve an LTA approximately equal to the ATI target value. Note that the base and target values are specified in terms of Linearised Counts, and the base value should always be larger than the target. Typically, a base value of 10000 to 30000 can be used, while a target value between 3500 and 10000 is recommended.

If the ATI algorithm cannot achieve a counts value within the ATI Band, the IQS324 will set the channel's ATI Error flag.

The Coarse Gain parameter in the *ProxFusion Dividers* register can be tuned in the GUI. The ATI will then adjust the Fine Divider parameter until the counts reach the base value. The Coarse Gain should be manually adjusted at design time until the Fine Divider reaches a value between '4' and '14' after ATI. It can then be fixed across production.

## 6.7 Automatic Re-ATI

One of the most important features of the automatic Re-ATI functionality of the IQS324 is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. It is always recommended to have the automatic Re-ATI functionality enabled. When a Re-ATI is performed on the IQS324, the *ATI Event* status bit will be set momentarily to indicate that this has occurred.





An automatic Re-ATI operation is performed when the reference of a channel drifts outside the acceptable range around the ATI Target, which is defined by the *ATI Band* parameter. Automatic Re-ATI is also triggered on ATI Error states.

### 6.8 Debouncing and Hysteresis

Each of the Button and Movement events provides two mechanisms to prevent jitter: debouncing and hysteresis.

Debouncing occurs when the Button or Movement delta initially crosses the threshold. It forces the IQS324 to perform a number of quick measurements (at High-Accuracy report rate), checking that all measurements exceed the threshold. The event's *Debouncing* flag is set as long as debouncing is active. Once debouncing is complete, the event's *Active* flag is set.

The number of high-frequency measurements to execute can be configured independently for entering or exiting the event's active state in the *Debounce* register. Setting the debounce values to '0' or '1' will disable debouncing.

Hysteresis allows the channel to use different enter and exit thresholds for an event. Once the event has entered the active state by exceeding the normal threshold value, the exit threshold is calculated as

Exit Threshold = Threshold 
$$\times \left(1 - \frac{\text{Hysteresis Value}}{256}\right)$$
 (5)

For example, with a Button threshold of 100 counts, and a hysteresis value of 50, the Button event will enter the Active state when the delta exceeds 100 counts, and will exit the Active state when the delta drops down to  $100 \times (1 - 50/256) = 80$  counts.





# 7 Power Options

### 7.1 Power Modes

The IQS324 offers 5 power modes:

### > High-Accuracy (HA)

- Highest current consumption
- High-accuracy mode is always entered during debouncing on the ProxFusion channel.
- When in automatic power mode, high-accuracy mode is entered when:
  - \* The Interval value has changed.

#### > Normal Power Mode (NP)

- The default operating power mode
- When in automatic power mode, normal power mode is entered when:
  - \* Exiting high-accuracy mode after the high-accuracy timeout.
    - \* Touch or movement event on the ProxFusion channel.

### > Low Power Mode (LP)

- Typically configured with a slower report rate to reduce current consumption.
- When in automatic power mode, low power mode is entered when the two following conditions are met:
  - \* Hall *Stationary* flag is set.
  - \* ProxFusion *Dormant* flag is set.

### > Ultra-Low Power Mode (ULP)

- Recommended being configured for the slowest report rate.
- In automatic power mode, the device will enter ULP mode after the *ULP Timeout* Event occurs. The ULP timer is started when the device enters LP mode.
- By default, ULP mode still samples both the Hall plates and the ProxFusion channel every cycle. ULP mode can instead be configured to use AutoProx, which only samples a single channel each cycle to further reduce current consumption.

### > Halt Mode

- Is entered and exited by an I<sup>2</sup>C command.
- Places device in standby mode.
- No analog sampling events occur during halt mode.
- Entering halt mode safely requires the manual configuration of a *Watchdog Period* of 4000 ms.
- To exit halt mode the master device must open a forced communications window (Refer to Section 9.11.2) and select an alternative power mode for the IQS324.



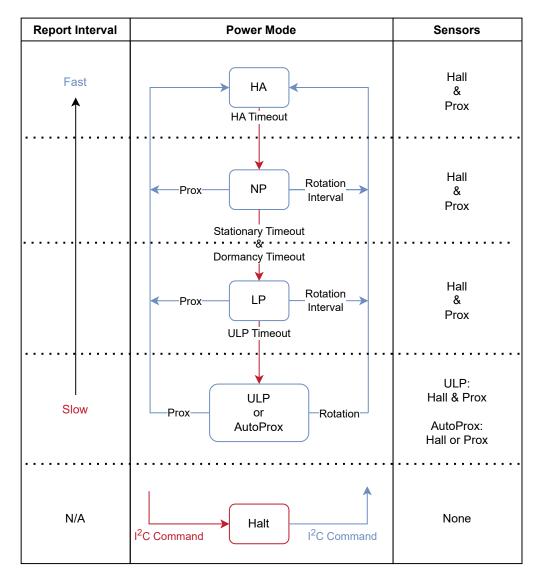


Figure 7.1: Power Modes

## 7.2 AutoProx

The IQS324 can be configured to use AutoProx when entering ULP Mode to further reduce current consumption. AutoProx is a feature that allows the IC to sample a single channel and perform basic limit checks on the counts, without running any power-intensive UIs or calculations. The channel then acts as a basic wake-up sensor. If the counts exceed the configured limit, the IQS324 will wake up and perform a full measurement and processing cycle.

AutoProx is enabled by setting the *AutoProx Enable* bit in the *ULP And Watchdog Settings* register. The wake-up channel can be selected as either the ProxFusion channel, or one of the Hall channels. This allows the IC to wake up on either a touch event, or when the magnet is rotated.

Note that AutoProx then replaces the regular ULP mode, and samples at the same rate as the ULP report rate. AutoProx should only be used with the Power Mode set to 'Auto'.





#### 7.2.1 AutoProx Limits

The AutoProx counts limit is set in the *AutoProx Threshold* register. Typical threshold values lie between 100 and 500 counts.

For the ProxFusion channel, the AutoProx threshold may be set to the same value as the *ProxFusion LTA Halt Threshold*.

For the Hall channels, the threshold can be chosen based on the size of the swing on the Hall channels, as well as the interval size. Ideally, the IQS324 should wake up within half an interval of rotation. For example, with 24 intervals (15° per interval) the device should wake up after a rotation of 7.5° or less. If the Hall Gain is adjusted to get  $\pm$ 4000 counts of swing on the Hall channels, the maximum allowed AutoProx limit is

Max Threshold =  $4000 \sin(7.5^\circ) = 522$ .

Note that certain invalid AutoProx Threshold configurations may result in an *AutoProx Error*, which is indicated in the *Device Status* register. At design time, it should be ensured that the chosen threshold does not cause this error flag to be set.

Note that if the AutoProx error flag is set during runtime, the IQS324 will fall back to performing regular measurements rather than AutoProx conversions while in ULP. Please contact Azoteq for more information.

#### 7.2.2 AutoProx Update Rate

After a certain number of AutoProx measurements, the IQS324 will automatically wake up and sample all channels for a single cycle. This is configured in the *ULP and Watchdog Settings* register, and can be configured to wake the device up periodically after 4, 8, 16, or 32 AutoProx measurements.



### 8 Additional Features

### 8.1 Debug and Display Software (GUI)

The Azoteq IQS324 GUI can be utilised to configure the optimal settings required for a specific hardware setup or application. The device performance can be easily monitored and evaluated in the graphical environment until the optimal device configuration is obtained.

Once the IQS324 is configured in the GUI as desired, a C header file (*.h* file) can be exported that stores the values of all the read-write registers of the IQS324. The *.h* file displays the start address of each block of data, with each address containing one byte. An example of the *.h* file exported by the GUI is shown below.

```
/* Change the System Control Settings */
/* Memory Map Position 0x1000 - 0x1011 */
#define AUTO_CLEAR_SETTINGS 0x00
#define SETTINGS_0 0xC4
...
```

## 8.2 Main Oscillator

The main oscillator frequency can be configured for 14 MHz or 18 MHz. This is configured in the *Power Settings* register. The lower-frequency configuration reduces the requirements on VDD, as shown in Section 3.3.

The higher-frequency configuration allows for larger amplification of the Hall plate signals, reducing noise in situations with low magnetic fields. This can be achieved by setting the *Hall Plate Bias* register to a higher value. The following table provides recommended values:

F <sub>OSC</sub> [MHz]	Hall Bias Value
14	30
18	37

## 8.3 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability. The watchdog timer is reset at the start of the main loop before any measurements take place. If the timer expires, the device is reset, performing a soft reboot. The *Watchdog Period* in the *Watchdog Settings* register determines the period of the timer in milliseconds before the device will reset.

**Note:** Ensure that the watchdog timeout period is greater than the  $I^2C$  timeout period.

### 8.4 Reset

#### 8.4.1 Reset Indication

After a reset, the *Show Reset* bit in the *Device Status* register will be set by the system to indicate that the reset event occurred. This device reset bit will clear when the master sets the *Ack Reset* bit in the *System Commands* register. If the Show Reset bit becomes set again, the master will know a reset has occurred and can react appropriately.



#### 8.4.2 Software Reset

The IQS324 can be reset by means of an I<sup>2</sup>C command, by setting the *Soft Reset* bit in the *System Commands* register.





# 9 I<sup>2</sup>C Interface

### 9.1 I<sup>2</sup>C Module Specification

The device features a standard two-wire  $I^2C$  interface, complemented by a RDY (ready interrupt) line, supporting a maximum bit rate of up to 1 Mbit/s. The memory structures accessible over the  $I^2C$  interface are byte-addressable with 16-bit address values. 16-bit or 32-bit values are packed with little-endian byte order and are stored in word-aligned addresses.

- > Standard two-wire interface with RDY interrupt line
- > Fast-Mode Plus I<sup>2</sup>C with up to 1 Mbit/s bit rate
- > 7-bit device address
- > 16-bit little-endian register addressing
- > One data byte stored per register address

#### 9.2 I<sup>2</sup>C Address

The IQS324 has a default  $I^2C$  address of 0x54 (0b1010100). The full address byte will thus be 0xA8 (write) or 0xA9 (read).

#### 9.2.1 Reserved I<sup>2</sup>C Address

When communicating with the IQS324, it will acknowledge (ACK) communication attempts made to an additional address derived from its slave address. This derived address is obtained by flipping the least significant bit of the slave address.

For example, with the default slave address of 0x54, the derived address would be 0x55 (0b1010101), obtained by changing the LSB from '0' to '1'. This derived address is reserved for internal use and should not be used. Even though the device will acknowledge communication attempts to this address, it will not function as normal, and should therefore be avoided.

### 9.3 I<sup>3</sup>C Compatibility

This device is not compatible with an I<sup>3</sup>C bus due to clock stretching allowed for data retrieval.

#### 9.4 Memory Map Addressing

All memory locations are 16-bit addressable in little-endian byte order.

#### 9.5 Memory Map Data

Each 16-bit memory map address stores a single byte (8 bits), making the memory map byte-addressable. Since the data is packed in a little-endian sequence, a 16-bit value starting at, for example, address 0x1014 will have its least significant byte at address 0x1014 and its most significant byte at address 0x1015.

### 9.6 RDY/IRQ

The IQS324 has an open-drain active low RDY signal to inform the master that updated data is available. The IQS324 will pull the RDY line low to indicate that it has opened a communications window, or "RDY window", for the master to read the new updated data. While the master can communicate



with the device at any time according to the *Force Comms Method*, it is recommended to use the RDY signal for optimal power consumption. Integrating the RDY signal as an interrupt input allows the master MCU to read and write data efficiently.

The device provides both streaming and event modes. In streaming mode, the RDY line toggles continuously, with each sensing cycle, whereas in event mode the RDY toggles only when specific events occurs. The types of events that trigger the RDY window are configurable in the *Event Mask* register.

# 9.7 Read and Write Operations

#### 9.7.1 I<sup>2</sup>C Read From Specific Address

A typical read operation is displayed in Figure 9.1. The master device waits for the RDY line of the IQS324 to go low, indicating the availability of new data and an available communication window. Once the RDY interrupt is triggered, the master initiates communication by sending a start condition followed by the device address and a write command. The IQS324 responds with an acknowledgement, after which the master device will transmit two bytes defining the register address. The master then sends a repeated start condition, followed by the device address with a read command. The IQS324 transmits data from the requested address and will continue to do so while the master acknowledges each byte. The read operation is ended when the master does not acknowledge the last byte received and produces a stop condition.

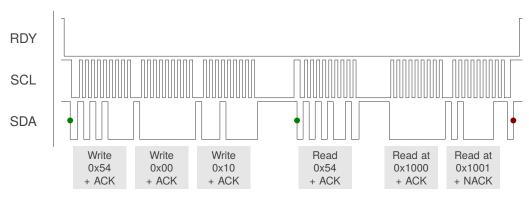


Figure 9.1: I<sup>2</sup>C Read Example — Read Status Registers 0x1000 and 0x1001

### 9.7.2 I<sup>2</sup>C Write To Specific Address

The write operation is displayed in Figure 9.2. Similar to the read transaction, when the RDY interrupt is triggered, the master initiates communication by sending a start condition followed by the device address and a write command. The IQS324 responds with an acknowledgement, after which the master device transmits two bytes defining the register address. The slave acknowledges the register address bytes. The master may then write a series of bytes to the register address and the addresses that follow, with each byte being acknowledged by the slave. The write operation is ended when the master produces a stop condition.



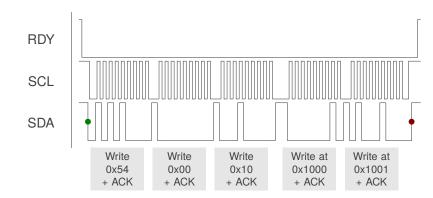


Figure 9.2: I<sup>2</sup>C Write Example — Write Two Bytes to Button Settings Registers 0x1000 and 0x1001

#### 9.7.3 Modifying Bits Over I<sup>2</sup>C

When modifying individual bits in a register, it is recommended to read the register first, make the necessary modifications, and then write the updated value back to the IQS324 register to prevent unintentional bit changes.

For example, setting the *Ack Reset* bit and *Power Mode* setting would involve:

- > Read the *System Control* Registers (0x1000 and 0x1001) as illustrated in Figure 9.1.
- > Set the *Ack Reset* bit using the bitwise OR operator. For example:

#### READ\_VALUE OR 0x01

> Set the *Power Mode* setting by clearing the bit field using a bitwise AND operation, then setting the bit field value with an OR operation. For example, to set the *Power Mode* to 'Auto':

#### (READ\_VALUE AND 0xF8) OR 0x04

> Write the new values back over  $I^2C$ , as shown in Figure 9.2.

Read-modify-write transactions should be done in a single communication window, using I<sup>2</sup>C restart conditions. Please refer to Section 9.9 for more information regarding multiple I<sup>2</sup>C transactions in a single communication window.

#### 9.8 I<sup>2</sup>C Timeout

If the communication window is not serviced within the  $I^2C$  *Timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be lost, so this should be avoided. The default  $I^2C$  timeout period is set to 250 ms.

#### 9.9 Terminate Communication

With the *Terminate Comms Window* setting enabled in the *Power Settings* register, a standard  $I^2C$  STOP ends the current communication window. If multiple  $I^2C$  transactions need to be done, then they should be strung together using repeated-start conditions instead of giving a STOP. Allowing an  $I^2C$  STOP to terminate the communication window is the recommended method, as illustrated in Figures 9.1 and 9.2.



This behaviour can be temporarily disabled by clearing the *Terminate Comms Window* setting. In this case, an I<sup>2</sup>C STOP will NOT terminate the communication window. Instead, the communication window can be closed manually, as desired, by setting the *Terminate Comms Window* bit as the final I<sup>2</sup>C transaction, followed by a STOP.

## 9.10 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- > The host is trying to read from a memory map register that does not exist.
- > The host is trying to read from the device outside a communication window (while RDY is high).

## 9.11 Event Mode Communication

The device can be set up to bypass the communication window when no activity is sensed by setting the *Event Mode* bit in the *Power Settings* register. This is usually enabled since the master does not need to be interrupted unnecessarily during every cycle if no activity occurs. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

Event mode can only be entered if the following requirements are met:

- > Events must be serviced by reading from the *Event Flags* register to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every cycle, similar to streaming mode.
- > The *Show Reset* bit in the *Device Status* register has been cleared by setting the *Ack Reset* bit in *System Commands*.

## 9.11.1 Events

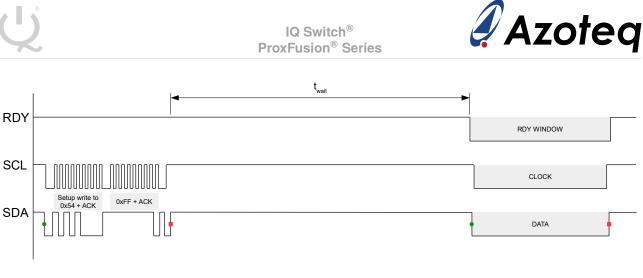
Numerous events can be individually enabled in the *Event Mask* register to trigger communication in Event Mode:

- > Power mode changes
- > ATI events
- > Touch/button events
- > Movement detection
- > Hall rotation event

## 9.11.2 Force Communication

In streaming mode, the IQS324 I<sup>2</sup>C will provide RDY windows at regular intervals specified by the relevant power mode report rate. This will provide the master with regular opportunities to perform I<sup>2</sup>C communication as necessary.

If the device is placed in Event Mode or Halt Mode, the IQS324 will not open RDY windows unless certain conditions are met. A new RDY window can be requested by writing 0xFF over I<sup>2</sup>C, followed by a stop condition. After a short delay, the IQS324 will pull the RDY line low and open a new communication window. This is shown in Figure 9.3.





After a short delay, a new communication window will be made available, indicated by the RDY signal. The delay between the communication request and the opening of a RDY window ( $t_{wait}$ ) is application specific, but will typically be under 2 milliseconds.





# 10 I<sup>2</sup>C Memory Map

## Table 10.1: I<sup>2</sup>C Memory Map

Address	Length	Description	Default	Notes
Read-Only No. Bytes		Version Info		
0x00	-			
0x01	2	Product Number	2389	
0x02				
0x03	2	Major Version	1	
0x04				
0x05	2	Minor Version	2	
Read-Write	No. Bytes	System Control Settings		
0x1000	1	System Commands	0	Appendix A.1
0x1001	1	Power Settings	196	Appendix A.2
0x1002	1	Event Masks	29	Appendix A.3
0x1003	1	ULP and Watchdog Settings	115	Appendix A.4
0x1004				
0x1005	2	AutoProx Threshold	200	
0x1006				
0x1007	2	HA Report Rate	2	0 - 3000
0x1008				
0x1009	2	NP Report Rate	20	0 - 3000
0x100A				
0x100B	2	LP Report Rate	100	0 - 3000
0x100C				
0x100D	2	ULP Report Rate	500	0 – 3000
0x100E				
0x100F	2	ULP Timeout	5000	
0x1010				
0x1011	2	I <sup>2</sup> C Timeout	250	
Read-Write	No. Bytes	ProxFusion <sup>®</sup> Settings		
0x1014	1	ProxFusion Settings 0	203	Appendix A.5
0x1015	1	ProxFusion Settings 1	55	Appendix A.6
0x1016				P.P
0x1017	2	Button Touch Timeout	8000	
0x1018				
0x1019	2	Button Dormancy Timeout	4000	
0x101A				
0x101B	2	Button ATI Timeout	1000	
0x101C	1	Counts Filter Beta	2	0 - 15
0x101D	1	LTA Filter Beta	8	0 - 15
0x101E	1	Fast LTA Filter Beta	4	0 - 15
0x101F	1	LP LTA Filter Beta	10	0 - 15
0x1020	· ·			
0x1020	2	Fast LTA Filter Band	5	
011021				



## Table 10.1: I<sup>2</sup>C Memory Map (Continued)

0x1022	2	Button Threshold	500	
0x1023				
0x1024	1	Button Debounce	18	Appendix A.7
0x1025	1	Button Hysteresis	20	
0x1026	2	Movement Threshold	200	
0x1027	_			
0x1028	1	Movement Debounce	18	Appendix A.8
0x1029	1	Movement Hysteresis	100	
0x102A	2	ProxFusion ATI Band	1000	
0x102B	L		1000	
0x102C	2	LTA Halt Threshold	100	
0x102D	L	En that the show	100	
Read-Write	No. Bytes	ProxFusion <sup>®</sup> ATI Settings		
0x102E	2	ProxFusion ATI Base	15000	
0x102F	2	T TOXT USION ATT Dase	15000	
0x1030	2	ProxFusion ATI Target	6500	
0x1031	2	Tioxi usion Arr larget	0500	
0x1032	2	ProxFusion Dividers		Appendix A.9
0x1033	2	FIOXFUSION DIVIDETS		Appendix A.
0x1034	2	Dray Euclary Componentian		
0x1035	2	ProxFusion Compensation		
Read-Write	No. Bytes	Hall Sensor Settings		
0x1036	2	Liell Diete Offect NW		
0x1037	2	Hall Plate Offset NW		
0x1037 0x1038				
	2	Hall Plate Offset NE		
0x1038	2	Hall Plate Offset NE		
0x1038 0x1039				
0x1038 0x1039 0x103A	2	Hall Plate Offset NE Hall Plate Offset SE		
0x1038 0x1039 0x103A 0x103B	2	Hall Plate Offset NE		
0x1038 0x1039 0x103A 0x103B 0x103C	2 2 2 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW		
0x1038 0x1039 0x103A 0x103B 0x103C 0x103D	2	Hall Plate Offset NE Hall Plate Offset SE	19942	Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103D 0x103E	2 2 2 2 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers		Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103D 0x103E 0x103F	2 2 2 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW	19942	Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103D 0x103E 0x103F 0x1040	2 2 2 2 2 2 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target	13000	Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103D 0x103E 0x103F 0x1040 0x1041	2 2 2 2 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers		Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103D 0x103F 0x1040 0x1041 0x1042	2 2 2 2 2 2 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target	13000	
0x1038 0x1039 0x103A 0x103B 0x103C 0x103D 0x103E 0x103F 0x1040 0x1041 0x1042 0x1043	2 2 2 2 2 2 2 2 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target Hall ATI Band	13000 2000	Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103D 0x103E 0x103F 0x1040 0x1041 0x1042 0x1043 0x1044	2 2 2 2 2 2 2 2 2 2 1	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target Hall ATI Band Hall Plate Bias	13000 2000 222	Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103E 0x103F 0x1040 0x1041 0x1042 0x1043 0x1044 0x1045	2 2 2 2 2 2 2 2 2 2 1 1 1	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target Hall ATI Band Hall Plate Bias Hall General Settings	13000 2000 222 91	Appendix A.1 Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103D 0x103F 0x1040 0x1041 0x1042 0x1043 0x1044 0x1045 0x1046	2 2 2 2 2 2 2 2 1 1 1 1 1 1 1	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target Hall ATI Band Hall Plate Bias Hall General Settings Reserved Hall Init Length	13000 2000 222 91 3	Appendix A.1 Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103E 0x103F 0x1040 0x1041 0x1042 0x1043 0x1044 0x1045 0x1046 0x1047	2 2 2 2 2 2 2 2 2 1 1 1 1 1	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target Hall ATI Band Hall Plate Bias Hall General Settings Reserved	13000 2000 222 91 3	Appendix A.1 Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103D 0x103E 0x1040 0x1041 0x1042 0x1042 0x1043 0x1044 0x1045 0x1044 0x1045 0x1046 0x1047 0x1048 0x1049	2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Dividers Hall Target Hall ATI Band Hall Plate Bias Hall General Settings Reserved Hall Init Length Phase Angle Sin	13000 2000 222 91 3	Appendix A.1 Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103E 0x103F 0x1040 0x1041 0x1042 0x1043 0x1044 0x1045 0x1044 0x1045 0x1046 0x1047 0x1048 0x1049 0x104A	2 2 2 2 2 2 2 2 1 1 1 1 1 1 1	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Target Hall ATI Band Hall Plate Bias Hall General Settings Reserved Hall Init Length	13000 2000 222 91 3	Appendix A.1 Appendix A.1
0x1038 0x1039 0x103A 0x103B 0x103C 0x103C 0x103D 0x103E 0x1040 0x1041 0x1042 0x1042 0x1043 0x1044 0x1045 0x1044 0x1045 0x1046 0x1047 0x1048 0x1049	2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 2	Hall Plate Offset NE Hall Plate Offset SE Hall Plate Offset SW Hall Dividers Hall Dividers Hall Target Hall ATI Band Hall Plate Bias Hall General Settings Reserved Hall Init Length Phase Angle Sin	13000 2000 222 91 3	Appendix A.1 Appendix A.1 Appendix A.1 Appendix A.1 Appendix A.1



## Table 10.1: I<sup>2</sup>C Memory Map (Continued)

0x1063	1	Reserved	0	
0x1064	2	Wheel To Meanet Aprile Offect		
0x1065	2	Wheel To Magnet Angle Offset		
0x1066	2	High Accuracy Timeout	300	
0x1067	2	High Acculacy Timeout	300	
0x1068	2	Stationary Timoout	5000	
0x1069	2	Stationary Timeout	5000	
0x106A	1	Auto Zero Beta	1	0 – 15
0x106B	1	Angle Filter Beta	12	0 – 31
0x106C	1	LP Angle Filter Beta	20	0 – 31
0x106D	1	CORDIC Resolution	14	
Read-Write	No. Bytes	Interval UI Settings		
Read-Write 0x106E	_		24	
	No. Bytes	Interval UI Settings Number of Intervals	24	
0x106E	2	Number of Intervals		Same unit as
0x106E 0x106F	_		24	Same unit as Processed Angle
0x106E 0x106F 0x1070	2	Number of Intervals Interval Hysteresis	250	Processed
0x106E 0x106F 0x1070 0x1071	2	Number of Intervals		Processed
0x106E 0x106F 0x1070 0x1071 0x1072	2	Number of Intervals Interval Hysteresis	250	Processed
0x106E 0x106F 0x1070 0x1071 0x1072 0x1073	2 2 2 2	Number of Intervals Interval Hysteresis Reserved	250	Processed



## Table 10.1: I<sup>2</sup>C Memory Map (Continued)

Read-Only	No. Bytes	System Flags			
0x2000	1	Power Mode Flags	Appendix A.16		
0x2001	1	Device Status	Appendix A.17		
0x2002	1	Hall Flags	Appendix A.18		
0x2003	1	Event Flags	Appendix A.19		
0x2004	1	ProxFusion <sup>®</sup> States	Appendix A.20		
0x2005	1	Reserved			
0x2006	1	Button Event Flags	Appendix A.21		
0x2007	1	Movement Event Flags	Appendix A.22		
Read-Only	No. Bytes	Hall Field Data			
0x2008	0	Liell Dista Deference NIM			
0x2009	2	Hall Plate Reference NW			
0x200A	0				
0x200B	2	Hall Plate Reference NE			
0x200C	0				
0x200D	2	Hall Plate Reference SE			
0x200E	0	Liall Dista Dafaranaa CW/			
0x200F	2	Hall Plate Reference SW			
0x2010					
0x2011	4	Loll Field Duffer NW	Signed 32-bi		
0x2012	4	Hall Field Buffer NW	value		
0x2013					
0x2014					
0x2015	4	Hall Field Buffer NE	Signed 32-bit		
0x2016	4		value		
0x2017					
0x2018					
0x2019	4	Hall Field Buffer SE	Signed 32-bit		
0x201A	4		value		
0x201B					
0x201C					
0x201D	4	Hall Field Buffer SW	Signed 32-bit		
0x201E	4		value		
0x201F					
0x2020					
0x2021	4	Field Differential A	Signed 32-bit		
0x2022	4		value		
0x2023					
0x2024					
0x2025	4	Field Differential B	Signed 32-bit		
0x2026	4		value		
0x2027					



## Table 10.1: I<sup>2</sup>C Memory Map (Continued)

Read-Only	No. Bytes	Hall Counts	
0x202A			
0x202B	2	Hall Counts NW	
0x202C			
0x202D	2	Reserved	
0x202E			
0x202F	2	Hall Inverse Counts NW	
0x2030	_		
0x2031	2	Reserved	
0x2032	-		
0x2033	2	Hall Counts NE	
0x2034	0		
0x2035	2	Reserved	
0x2036	0		
0x2037	2	Hall Inverse Counts NE	
0x2038	0	Deserved	
0x2039	2	Reserved	
0x203A	2	Hall Counts SE	
0x203B	2	Hail Courts SE	
0x203C	2	Reserved	
0x203D	2	neserveu	
0x203E	2	Hall Inverse Counts SE	
0x203F	۷.		
0x2040	2	Reserved	
0x2041	2	neserveu	
0x2042	2	Hall Counts SW	
0x2043	<u> </u>		
0x2044	2	Reserved	
0x2045	۲	neserveu	
0x2046	2	Hall Inverse Counts SW	
0x2047			
Read-Only	No. Bytes	<b>ProxFusion®Counts</b>	
0x204A	2	ProxFusion <sup>®</sup> Counts	
0x204B	_		
0x204C	2	ProxFusion <sup>®</sup> Filtered Counts	
0x204D	_		
0x204E	2	Reserved	
0x204F			
0x2050	2	ProxFusion <sup>®</sup> Button LTA	
0x2051			
0x2052	2	Reserved	
0x2053			
0x2054	2	ProxFusion <sup>®</sup> Movement LTA	
0x2055			
0x2056	2	Reserved	
0x2057			



## Table 10.1: I<sup>2</sup>C Memory Map (Continued)

0x2058	2	ProxFusion <sup>®</sup> Button Delta	Signed 16-bit
0x2059	2	value	
0x205A	2	Signed 16-bit	
0x205B	۲	ProxFusion <sup>®</sup> Movement Delta	value
Read-Only	No. Bytes	Hall Rotation Data	
0x2064	2	Current Interval	
0x2065	۷	ourient interval	
0x2066			Same unit as
0x2067	2	Interval Upper Limit	Processed Angle
0x2068			Same unit as
0x2069	2	Interval Lower Limit	Processed Angle
0x206A	2	Processed Angle	0 – 65536 →
0x206B	2	Tiblessed Aligie	0° – 360°
0x206C	2 Absolute Angle		$0-65536 \rightarrow$
0x206D		/ loolate / ligit	0° – 360°
Read-Only	No. Bytes	Hall Normalisation Data	
0x206E	_		
0x206F	4	Normalised Hall Field A	Signed 32-bit
0x2070			value
0x2071			
0x2072	_		
0x2073	4	Normalised Hall Field B	Signed 32-bit
0x2074			value
0x2075			
0x2076	2 Minimum Hall Field A		Unsigned 16-b
0x2077	<u>_</u>		value
0x2078	2	Reserved	
0x2079	<u> </u>	TICSCI VCG	
0x207A	2	Minimum Hall Field B	Unsigned 16-b
0x207B			value
0x207C	2	Reserved	
0x207D	-		
0x207E	2	Maximum Hall Field A	Unsigned 16-b
0x207F	-		value
0x2080	2	Reserved	
0x2081	<b></b>		
0x2082	2	Maximum Hall Field B	Unsigned 16-b
0x2083	<b>_</b>		value
0x2084	2	Reserved	
0x2085	<u> </u>	10001700	



# **11 Ordering Information**

## 11.1 Ordering Code

## Table 11.1: Order Code Description

IQS324 zzz ppb

IC NAME				IQS324
CONFIGURATION	ZZZ	=	001	I <sup>2</sup> C address: 0x54
PACKAGE TYPE	рр	=	QF	QFN-20 Package
BULK PACKAGING	b	=	R	QFN-20 Reel (2000 pcs/reel)

## 11.2 Top Marking

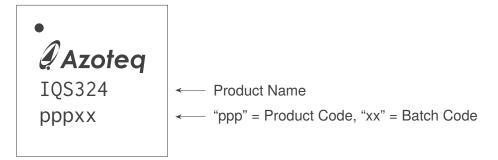


Figure 11.1: IQS324-QFN20 Package Top Marking

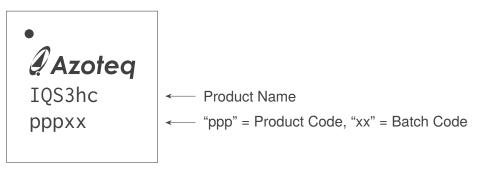


Figure 11.2: QFN20 Generic Package Top Marking





# 12 Package Information

# 12.1 QFN20 Package Outline

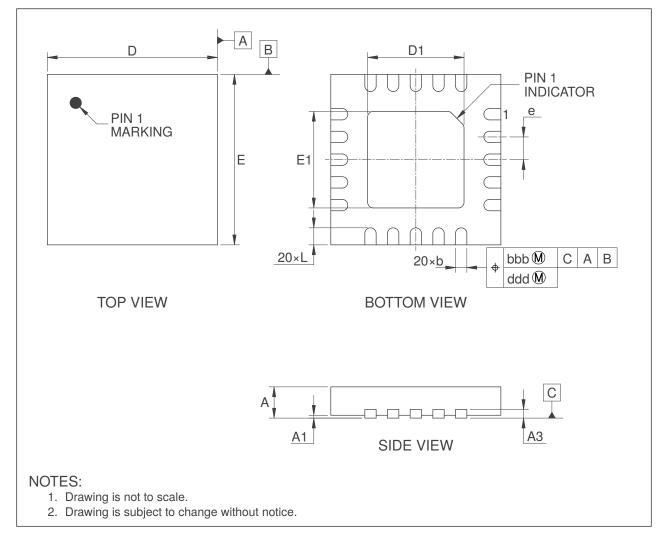


Figure 12.1: QFN20 Package Outline



## Table 12.1: QFN20 Package Dimensions [mm]

Dimension	Millimeters				
Dimension	Min	Тур	Мах		
А	0.50	0.55	0.60		
A1	0.00	0.02	0.05		
A3	0.152 REF				
b	0.15	0.25			
D		3.00 BSC			
E		3.00 BSC			
D1	1.60	1.70	1.80		
E1	1.60 1.70 1.80				
е	0.40 BSC				
L	0.25	0.30	0.35		

## Table 12.2: QFN20 Package Tolerances [mm]

Tolerance	Millimeters
bbb	0.07
ddd	0.05





# 12.2 QFN20 Recommended Footprint

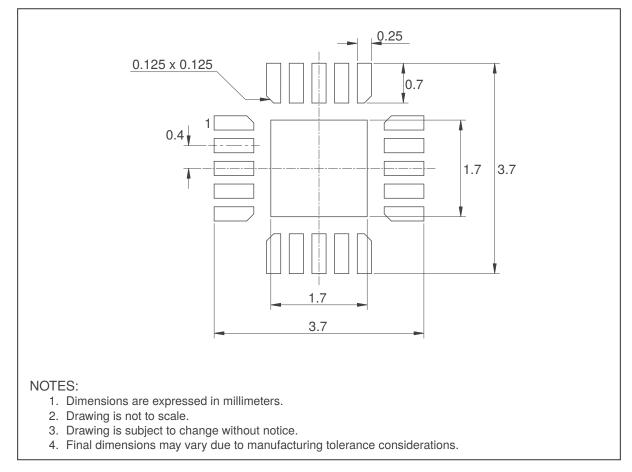
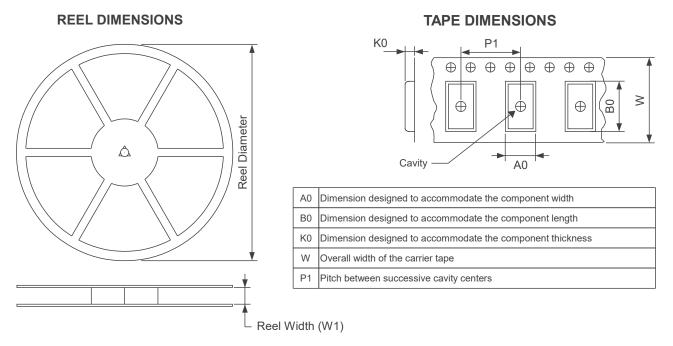


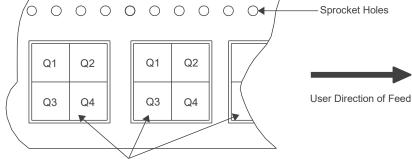
Figure 12.2: QFN20 Recommended Footprint



# 12.3 Tape and Reel Specifications



## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Pocket Quadrants

Figure 12.3: Tape and Reel Specification

#### Table 12.3: Tape and Reel Specifications

Paakaga			Pin 1						
Package Type	Pins	Reel Diameter	Reel Width	<b>A</b> 0	B0	К0	P1	W	Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2



# A Memory Map Descriptions

## A.1 System Commands (0x1000)

Bit	7	6	5	4	3	2	1	0
Description	Rese	erved	Reseed Proxfusion Channel	Zero	ATI Hall	ATI ProxFusion Channel	Soft Reset	Ack Reset

## > Bit 5: Reseed Proxfusion Channel

- 0: No action
- 1: Reseed the Proxfusion channel LTA
- Bit automatically cleared

## > Bit 4: Zero

- 0: No action
- 1: Set the processed Hall angle to the centre of interval 0
- Bit automatically cleared

## > Bit 3: ATI Hall

- 0: No action
- 1: Perform ATI calibration of the Hall channels
- · Bit automatically cleared

## > Bit 2: ATI ProxFusion Channel

- 0: No action
- 1: Perform ATI calibration of the ProxFusion channel
- Bit automatically cleared

## > Bit 1: Soft Reset

- 0: No action
- 1: Soft reset the device
- Bit automatically cleared

## > Bit 0: Ack Reset

- 0: No action
- 1: Acknowledge a device reset
- · Bit automatically cleared

## A.2 Power Settings (0x1001)

E	Bit	7	6	5	4	3	2	1	0
Desc	ription	Terminate Comms	Event Mode	Rese	erved	FOSC Select	Pov	ver Mode Set	ting

## > Bit 7: Terminate Comms on Stop

- 0: Keep I<sup>2</sup>C communications window open on I<sup>2</sup>C stop condition
- 1: Close I<sup>2</sup>C communications window on I<sup>2</sup>C stop condition

## > Bit 6: Event Mode

- 0: Streaming mode enabled. An I<sup>2</sup>C communications window is opened every cycle.
- 1: Event mode enabled. An I<sup>2</sup>C communications window is opened only if an enabled event occurs.

## > Bit 3: Fosc Select

- 0: 14 MHz
- 1: 18 MHz
- > Bit 0-2: Power Mode Setting
  - 0: High Accuracy
  - 1: Normal Power
  - 2: Low Power
  - 3: Ultra Low Power
  - 4: Auto
  - 7: Halt



# A.3 Event Masks (0x1002)

Bit	7	6	5	4	3	2	1	0
Description		Reserved		Hall Interval	Movement	Button	ATI	Power Mode

## > Bit 4: Hall Interval

- 0: Disabled
- 1: Open an I<sup>2</sup>C communications window on Hall interval changes
- > Bit 3: Movement
  - 0: Disabled
  - 1: Open an I<sup>2</sup>C communications window on Movement events

## > Bit 2: Button

- 0: Disabled
- 1: Open an I<sup>2</sup>C communications window on Button events
- > Bit 1: **ATI** 
  - 0: Disabled
  - 1: Open an I<sup>2</sup>C communications window on ATI events
- > Bit 0: Power Mode
  - 0: Disabled
  - 1: Open an I<sup>2</sup>C communications window on power mode changes

# A.4 ULP and Watchdog Settings (0x1003)

Bit	7	6	5	4	3	2	1	0
Descriptio	Disable Read-Only Check	W	/atchdog Perio	od	AutoProx Channel	AutoProx Enable		Conversion ting

## > Bit 7: Disable Read-Only Check

0: Disabled

## 1: Enabled

## > Bit 4-6: Watchdog Period

- 0: Off
- 1: 50 ms
- 2: 125 ms
- 3: 250 ms
- 4: 500 ms
- 5: 1000 ms
- 6: 2000 ms
- 7: 4000 ms

## > Bit 3: AutoProx Channel

- 0: Use ProxFusion channel as wake-up channel in AutoProx mode
- 1: Use Hall channels as wake-up channel in AutoProx mode

## > Bit 2: AutoProx Enable

- 0: AutoProx disabled
- 1: AutoProx enabled

## > Bit 0-1: AutoProx Conversion Setting

- 0: Update all channels and UIs after 4 AutoProx conversions
- 1: Update all channels and UIs after 8 AutoProx conversions
- 2: Update all channels and UIs after 16 AutoProx conversions
- 3: Update all channels and UIs after 32 AutoProx conversions



## IQ Switch<sup>®</sup> ProxFusion<sup>®</sup> Series



# A.5 ProxFusion Settings 0 (0x1014)

Bit	7	6	5	4	3	2	1	0
Description	ATI N	Node	Dual Threshold	Inverse		Rese	erved	

## > Bit 6-7: ATI Mode

- 0: Disabled
- 1: Divider Only
- 2: Compensation Only
- 3: Divider And Compensation

## > Bit 5: Dual Threshold

- Allow button events to trigger for both positive and negative delta values
- 0: Disabled
- 1: Enabled
- > Bit 4: Inverse
  - Set button events to trigger for negative deltas. May be necessary for inductive sensing.
  - 0: Disabled
  - 1: Enabled

# A.6 ProxFusion Settings 1 (0x1015)

Bit	7	6	5	4	3	2	1	0	
Description	FOSC Tx		Sensing Mode	Э	Button Conversion Frequency				

- > Bit 7: Fosc Tx
  - 0: Disabled
  - 1: Run sensor with TX at F<sub>OSC</sub> frequency. Recommended only for inductive sensing.

#### > Bit 4-6: Sensing Mode

- 0: Disabled
- · 3: Self-Capacitance
- 4: Inductance

#### > Bit 0-3: Conversion Frequency

- The following are recommended example values:
  - 0: 7 MHz / 9 MHz
  - 1: 3.5 MHz / 4.5 MHz
  - 3: 1.750 MHz / 2.25 MHz
  - 7: 0.875 MHz / 1.125 MHz
  - 15: 0.4375 MHz / 0.5625 MHz

Note: The maximum recommended conversion frequency for capacitive sensing is 1 MHz.

# A.7 Button Debounce (0x1024)

Bit	7	6	5	4	3	2	1	0
Description		Debour	nce Exit			Deboun	ce Enter	

## > Bit 4-7: Debounce Exit

- 4-bit value
- Number of high-frequency samples while exiting Button state

## > Bit 0-3: Debounce Enter

- 4-bit value
- Number of high-frequency samples while entering Button state



# Ц.

## A.8 Movement Debounce (0x1028)

Bit	7	6	5	4	3	2	1	0	
Description		Debour	nce Exit		Debounce Enter				

## > Bit 4-7: Debounce Exit

- 4-bit value
- Number of high-frequency samples while exiting Movement state

## > Bit 0-3: **Debounce Enter**

- 4-bit value
- Number of high-frequency samples while entering Movement state

# A.9 ProxFusion Dividers (0x1032)

Bit	15	14	13	12	11	10	9	8
Description	Rese	erved		Fine Divider			Coarse Gain	
Bit	7	6	5	4	3	2	1	0
Description				Coars	e Gain			

## > Bit 9-13: Fine Divider

5-bit value

## > Bit 0-8: Coarse Gain

- 9-bit value
- Coarse Gain can be chosen based on the following values:

## Table A.1: Coarse Gain Recommended Values

Gain Ratio	<b>Register Value</b>
4.00	258
2.00	130
1.00	66
0.50	68
0.43	206
0.29	71
0.14	78
0.07	91

# A.10 Hall Dividers (0x103E)

Bit	15	14	13	12	11	10	9	8
Description		Hall Divider						
Bit	7	6	5	4	3	2	1	0
Description				Hall C	livider			

## > Bit 0-15: Hall Divider

• Hall Gain can be chosen based on the following values:



## Table A.2: Hall Divider Recommended Values

Gain Ratio	<b>Register Value</b>
3.00	0x4721
2.25	0x4921
1.33	0x4702
0.82	0x5721
0.47	0x6721
0.29	0x4E82
0.25	0x4DE6
0.17	0x4644
0.10	0x4A44

## A.11 Hall Plate Settings (0x1044)

Bit	7	6	5	4	3	2	1	0			
Description	Hall An	Hall Amp Gain		Hall Plate Bias							

# > Bit 6-7: Hall Amplifier Gain 2-bit value

•	2-bit v
0	0: x1
0	1: x2
0	2: x4

- 2. x4 • 3: x8
- > Bit 0-5: Hall Plate Bias
  - 6-bit value
  - Refer to Table 8.1

# A.12 Hall General Settings (0x1045)

Bit	7	6	5	4	3	2	1	0
Description	Hall At FOSC	Runtime ATI		Ma	ignet Orientat	lion		Reserved

## > Bit 7: Hall At FOSC

- 0: Disabled
- 1: Run Hall measurements at F<sub>OSC</sub> frequency.
- > Bit 6: Runtime ATI
  - 0: Disabled
  - 1: Enabled
- > Bit 1-5: Magnet Orientation
  - 1: Off-axis N-S axis
  - 17: Off-axis W-E axis
  - 11: Off-axis NW to SE diagonal axis
  - 13: Off-axis NE to SW diagonal axis
  - 6: Hall sensing disabled

# A.13 Hall Init Length (0x1047)

Bit	7	6	5	4	3	2	1	0
Description			Reserved			ł	-Iall Init Lengtl	h

## > Bit 0-2: Hall Init Length





- 0: 8 counts
- 1: 16 counts
- 2: 32 counts
- 3: 64 counts
- 4: 256 counts (recommended)
- 5: 512 counts
- 6: 1024 counts
- 7: 2048 counts

# A.14 Rotation UI Settings (0x1062)

Bit	7	6	5	4	3	2	1	0
Description	Reserved	A	uto Zero Mod	le	Rese	erved	Reverse	Reserved

## > Bit 4-6: Auto Zero Mode

- 0: Off
- 1: Stationary
- 2: Continuous
- · 3: Stationary-Release
- 4: Continuous-Release

## > Bit 1: Reverse

- 0: Disabled
- 1: Reverse direction of sampled rotation

# A.15 Normalisation Mode (0x1075)

Bit	7	6	5	4	3	2	1	0
Description			Rese	erved			Norm	Mode

## > Bit 0-1: Normalisation Mode

- 0: Off
- 1: Auto
- 2: Manual

## A.16 Power Mode Flags (0x2000)

Bit	7	6	5	4	3	2	1	0
Description			Rese	erved			Power	Mode

## > Bit 0-1: Power Mode

- 0: High Accuracy
- 1: Normal Power
- 2: Low Power
- · 3: Ultra Low Power

## A.17 Device Status (0x2001)

Bit	7	6	5	4	3	2	1	0
Description			Rese	erved			AutoProx Error	Show Reset

## > Bit 1: AutoProx Error

- 0: Disabled
- 1: An error occurred with the AutoProx limits. The device will perform regular measurements rather than Auto-Prox conversions in Ultra Low power mode.



## > Bit 0: Show Reset

- 0: Disabled
- 1: System reset event occurred

# A.18 Hall Flags (0x2002)

Bit	7	6	5	4	3	2	1	0
Description		Rese	erved		High Accuracy	Stationary	Direction	Interval Change

## > Bit 3: High Accuracy

- 0: Device not in high-accuracy mode
- 1: IQS324 sampling at high-accuracy report rate to avoid aliasing

## > Bit 2: Stationary

- 0: Magnet moved recently. IQS324 samples at normal or high-accuracy report rate.
- 1: Magnet is considered stationary when interval has not changed for some time. IQS324 may transition to lower power mode.

## > Bit 1: Direction

- 0: Interval change in negative direction
- 1: Interval change in positive direction

## > Bit 0: Interval Change

- 0: No interval change occurred
- 1: Interval change occurred

# A.19 Event Flags (0x2003)

Bit	7	6	5	4	3	2	1	0
Description		Reserved		Hall Interval	Movement Event	Button Event	ATI Event	Power Mode Event

## > Bit 4: Hall Interval

- 0: No event
- 1: Interval change occurred
- Cleared on read
- > Bit 3: Movement Event
  - 0: No event
  - 1: Movement event occurred
  - Cleared on read

## > Bit 2: Button Event

- 0: No event
- 1: Button event occurred
- Cleared on read

## > Bit 1: ATI Event

- 0: No event
- 1: ATI event occurred
- Cleared on read

## > Bit 0: Power Mode Event

- 0: No event
- 1: Power mode change occurred
- Cleared on read

# A.20 Proxfusion States (0x2004)

Bit	7	6	5	4	3	2	1	0
Description			Rese	erved			ATI Error	Dormant



## > Bit 1: ATI Error

- 0: No error
  - 1: ProxFusion channel failed to calibrate correctly

## > Bit 0: Dormant

- 0: Recent activity on the ProxFusion channel occurred
- 1: ProxFusion channel is considered dormant after some period of inactivity. Allows device to transition to a lower power mode.

# A.21 Button Event Flags (0x2006)

Bit	7	6	5	4	3	2	1	0
Description	Rese	erved	Button Exit	Button Enter	LTA Halt	Debounce	Reserved	Button Event Active

## > Bit 5: Button Exit

- 0: No event
- 1: "Button release" event. Button Active state transitioned from '1' to '0'.
- > Bit 4: Button Enter
  - 0: No event
    - 1: "Button press" event. *Button Active* state transitioned from '0' to '1'.

## > Bit 3: LTA Halt

- 0: LTA is filtering normally
- 1: LTA filter is halted to improve channel sensitivity

## > Bit 2: Button Debounce

- 0: Button UI not currently debouncing
- 1: Button UI currently debouncing by sampling at high-accuracy report rate

## > Bit 0: Button Event Active

- 0: Button UI delta currently below threshold
- 1: Button UI delta currently above threshold. Button is considered "pressed".

## A.22 Movement Event Flags (0x2007)

Bit	7	6	5	4	3	2	1	0
Description	Rese	erved	Movement Exit	Movement Enter	Reserved	Debounce	Direction	Movement Active

## > Bit 5: Movement Exit

- 0: No event
- 1: "Release" event. Movement Active state transitioned from '0' to '1' with a negative delta.

## > Bit 4: Movement Enter

0: No event

• 1: "Touch" event. *Movement Active* state transitioned from '0' to '1' with a positive delta.

## > Bit 2: Movement Debounce

- 0: Movement UI not currently debouncing
- 1: Movement UI currently debouncing by sampling at high-accuracy report rate

## > Bit 1: Movement Direction

- 0: Movement delta is less than 0
- 1: Movement delta is greater than 0

## > Bit 0: Movement Event Active

- 0: No movement detected
  - 1: Movement occurring on ProxFusion channel. The movement UI delta is currently above the threshold.



# B Known Issues

# B.1 Soft Reset During Force Comms

An I<sup>2</sup>C transaction that addresses the IQS324 outside a valid communication window, such as a force communication request when the RDY pin is high, may cause the IQS324 to soft reset. This reset risk is present in a short time window (over a few microseconds) at the end of each measurement cycle, when the IQS324 enters a deep sleep mode. The reset risk is only present for report periods higher than 5 ms.

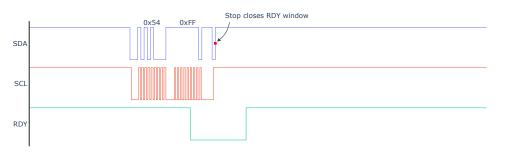
Application MCU firmware should reliably be able to handle a reset condition and reconfigure the IQS324. This can be done by checking the state of the reset bit on every RDY window. An example of this can be found in the Arduino example code provided on Azoteq's website.

The following strategies can help reduce the likelihood of encountering the reset issue:

- > Make use of the IQS324's automatic communications windows as far as possible. Avoid addressing the IQS324 while the RDY pin is high, and keep force communication requests to a minimum.
- If a large amount of data needs to be written to the IQS324 over multiple I<sup>2</sup>C transactions, enable the device's Streaming Mode and then write the data within the automatic RDY windows. Streaming mode is enabled by writing a 0 to the *Event Mode* bit in the *Power Settings* register. To re-enter Event Mode, write a 1 to the *Event Mode* bit.
- > Device addressing and force communication requests should not be performed within 300 µs of a previous communications window (after the RDY pin transitioned to HIGH).

# **B.2** Force Communication Request may Close a Communication Window

A force communication request (0xFF command) may unintentionally close a communication window instead of opening it. This occurs if the IQS324 receives the force communication request while the RDY is low. The I<sup>2</sup>C STOP condition at the end of the 0xFF byte triggers the IQS324 to close its communication window, causing the RDY to go back high immediately. This may also happen if the communication window automatically opens during the transmission of the 0xFF byte, as shown in Figure B.1.



*Figure B.1: Force Communication Closing a Communication Window* 

As a result, the MCU may observe the RDY pin change, and then attempt to communicate with the IC as soon as the force communication transaction is complete. This will cause the IQS324 to respond with the error code 0xEE.

The following protocol can be used to minimise the likelihood of this error condition.





- Step 1: Before sending the 0xFF command, read the state of the RDY pin and verify that it is high (the communication window is closed). If the RDY pin is already low, the communications window is open and can be handled as normal.
- Step 2: If the RDY pin is high, issue the force communication I<sup>2</sup>C command.
- Step 3: As soon as the I<sup>2</sup>C transmission of the force communication command has started, wait for the RDY window.
- Step 4: Once the RDY is received, the MCU should wait at least 300  $\mu$ s, then re-check the state of the RDY pin.
  - (a) If the RDY pin is high, then the window was closed due to the STOP condition. Reissue the 0xFF command, repeating the above procedure.
  - (b) If the RDY pin is low, the communication window is still open, and normal I<sup>2</sup>C operations may resume.

Figure B.2 shows an example of this process. The first force communication request occurred simultaneously with a RDY window, and the RDY window was closed due to the STOP condition. The MCU detected the RDY window, waited  $300 \,\mu$ s, then checked the RDY pin state. The pin was HIGH, and the force communication request was repeated.

The second request opened the RDY window after some time, and the MCU waited 300 µs again before checking the RDY pin state. The RDY was low, and normal communication could continue.

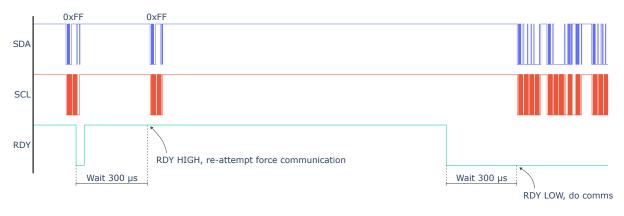


Figure B.2: Force Communication With RDY Check

It is also recommended to add checks for 0xEE error codes. All status and event flags have reserved upper bits that are always 0. Therefore, the value of those registers can be checked, and considered invalid if they are 0xEE.



# C Revision History

Release	Date	Comments
v1.0	September 2024	Initial document released.
v1.1	March 2025	Added Known Issues sections regarding force communication. Added block diagram. Added Hall Amplifier Gain bits to memory map, register 0x1044. Updated Hall ATI subsection to include Hall Amplifier Gain. Added ProxFusion Coarse Gain table with recommended values, register 0x1032.
		Added Hall Dividers table with recommended values, register 0x103E.
		Updated Minor Version value from '0' to '2'.



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