IQS320 DATASHEET

2 Channel proximity sensing/ single channel proximity sensing with reference tracking controller with Movement and SNR Boost User Interfaces. The device is specifically designed for SAR and other similar high performance proximity sensing requirements. The device features an I²C communications interface and the option to run the device in a standalone mode.

1 Device Overview

The IQS320 ProxFusion® IC is a self-capacitive sensing device optimised to work in SAR and similar applications that require the detection of very small capacitive changes in a high capacitive load environment. The sensor is fully I²C compatible with the ability to operate in a standalone mode. On-chip calculations allow the device to process small movements, and detect the smallest possible changes in capacitance. It is recommended to use the *SNR Boost UI* in conjunction with the *Reference UI* in applications with sensitive or critical proximity triggers and high capacitance load environments.

1.1 Main Features

- Dual channel self-capacitance Sensor
- 2 External sensor pad connections
- External sensor options:
  - 2 self-capacitance sensors
  - 1 self-capacitance sensor with a reference tracking sensor
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Debounce & Hysteresis
  - High performance in high capacitive load conditions
- Built-in Signal processing options:
  - Touch/Proximity output
  - Movement User Interface
  - Reference User Interface
  - Signal to Noise Ratio Boost User Interface by means of oversampling (add Reference UI for optimal performance)
- Design simplicity
  - PC Software for debugging & optimal setup for performance
- I²C communication interface with IRQ/RDY(up to fast plus - 1MHz)
- Event and streaming modes with I²C
- Selectable I²C address
- Standalone output mode
- Supply Voltage 1.71V to 3.5V
- Package options
  - WLCSP11 (1.48 x 1.08 x 0.345 mm) - interleaved 0.35mm x 0.35mm ball pitch
  - DFN12 (3 x 3 x 0.75 mm) - 0.5mm pitch

1.2 Applications

- SAR Safety Sensor
- Keyboard back-lighting
- Wireless charger wake-up

1.3 Block Diagram

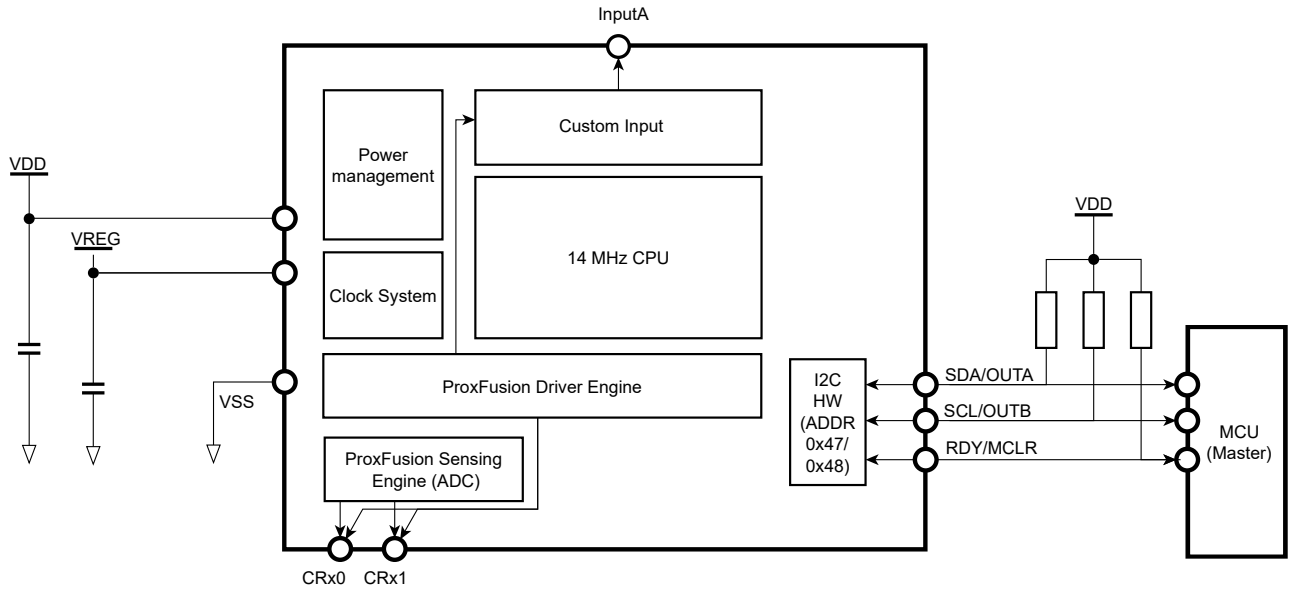


Figure 1.1: Functional Block Diagram

Contents

2 Hardware Connection

2.1 WLCSP11 Pin Diagram

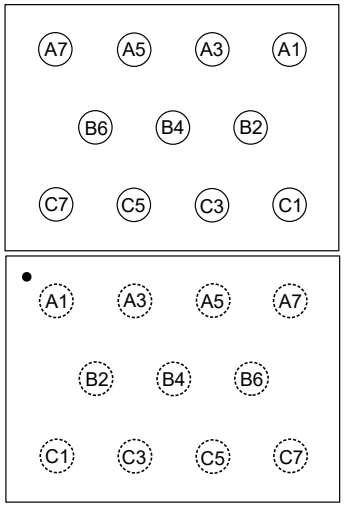


Table 2.1: 11-pin WLCSP11 Package

Pin no.	Signal
A7	VSS
A5	SDA/OutA
A3	VREG
A1	CRx1/CTx1
B6	InputA
B4	Unused
B2	CRx0/CTx0
C7	RDY/MCLR
C5	VDD
C3	SCL/OutB
C1	Unused

2.2 DFN12 Pin Diagram

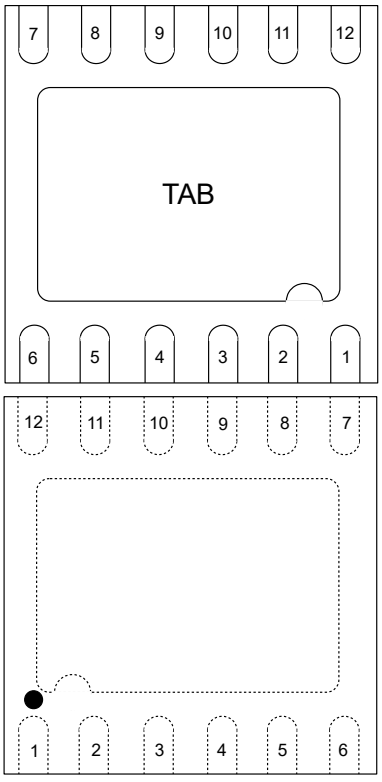


Table 2.2: 12-pin DFN Package

Pin no.	Signal
1	InputA
2	SDA/OutA
3	VDD
4	VREG
5	SCL/OutB
6	Unused
7	CRx0/CTx0
8	NC
9	CRx1/CTx1
10	Unused
11	RDY/MCLR
12	VSS

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP11	DFN12				
B6	1	InputA	Digital		VDD
A5	2	SDA/OutA	Digital		VDD
C5	3	VDD	Power	Power	N/A
A3	4	VREG	Power	Power	N/A
C3	5	SCL/OutB	Digital		VDD
C1	6	Unused	-		-
B2	7	CRx0/CTx0	Analog		VREG
-	8	NC	-		-
A1	9	CRx1/CTx1	Analog		VREG
B4	10	Unused	-		-
C7	11	RDY/MCLR	Digital		VDD
A7	12	VSS	Power	Power	N/A

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[i]	Description
		WLCSP11	DFN12		
ProxFusion®	CRx0/CTx0	B2	7	IO	ProxFusion® channel
	CRx1/CTx1	A1	9	IO	
	Unused	C1	6	-	
GPIO	InputA	B6	1	I	InputA pad
	Unused	B4	10	-	Unused pad
	RDY/MCLR	C7	11	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP
I^2C/Digital Out	SDA/OutA	A5	2	IO	I^2C Data / Digital Output
	SCL/OutB	C3	5	IO	I^2C Clock / Digital Output
Power	VDD	C5	3	P	Power supply input voltage
	VREG	A3	4	P	Internal regulated supply output
	VSS	A7	12	P	Analog/Digital Ground

[i] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.5 Reference Schematic

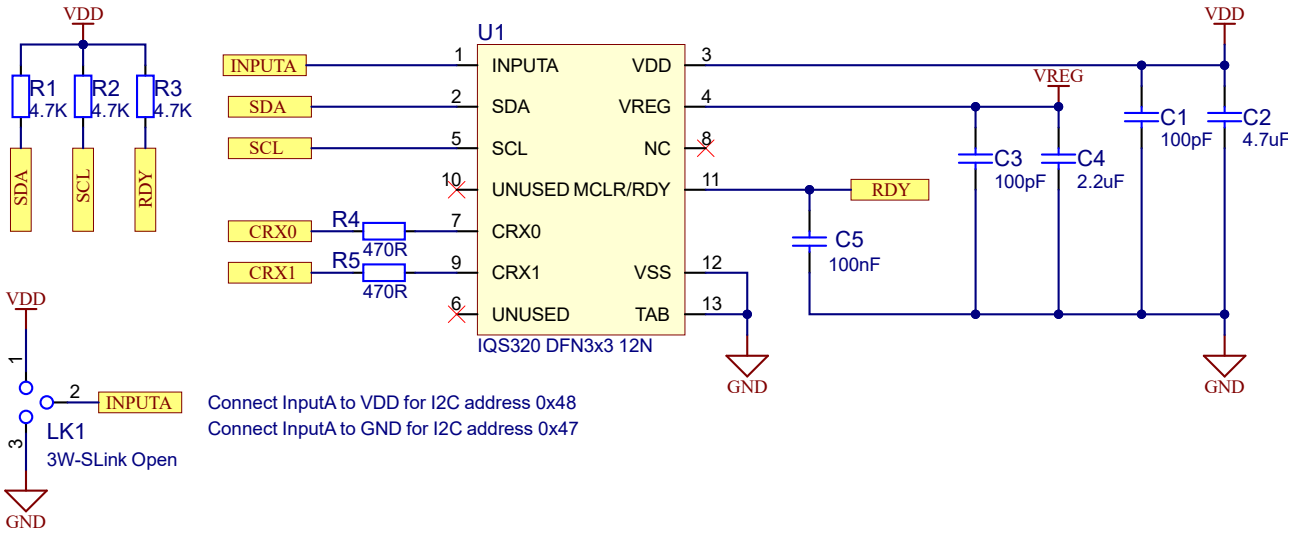


Figure 2.1: DFN12 I²C Reference Schematic

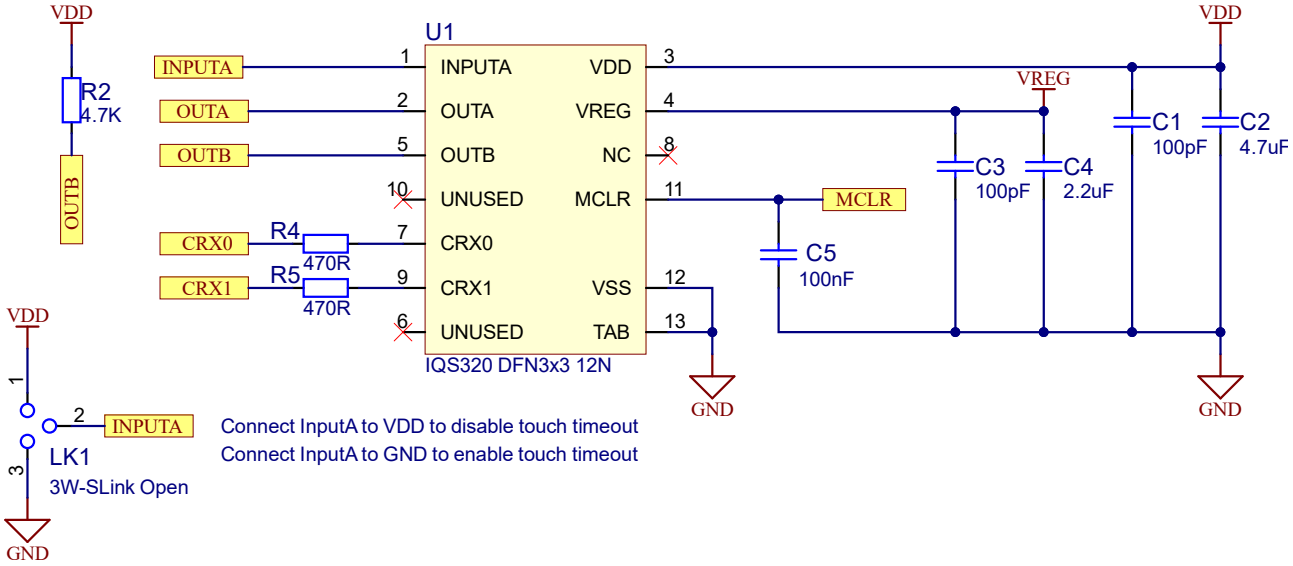


Figure 2.2: DFN12 Standalone Reference Schematic

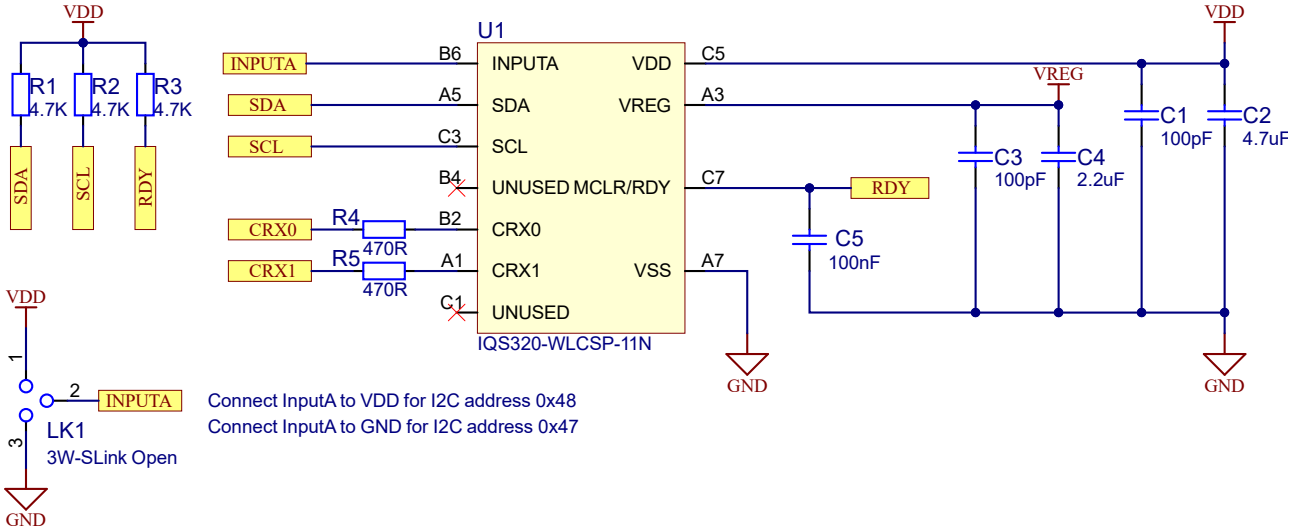


Figure 2.3: WLCSP11 I²C Reference Schematic

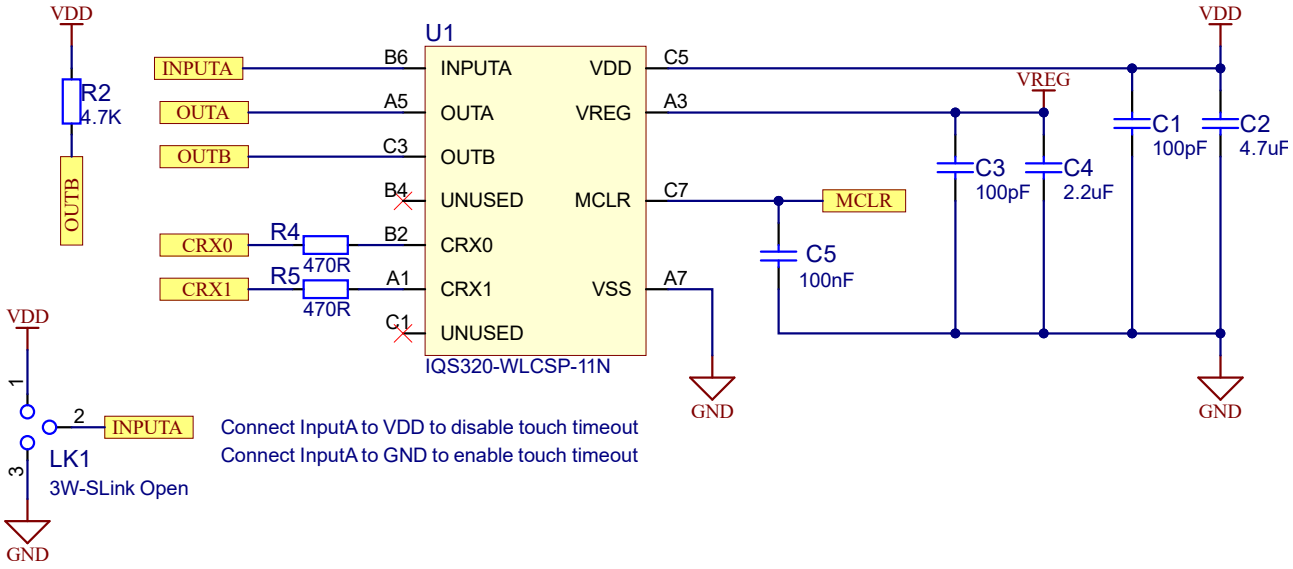


Figure 2.4: WLCSP11 Standalone Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.5	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.5V max)	V
Storage temperature, T_{stg}	-40	85	°C

3.2 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.5	V
VREG	Internal regulated supply output for analog domain		1.53		V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T_A	Operating free-air temperature	-40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2*C_{VREG}$	$3*C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	2	5	13	µF
$Cx_{\_SELF-VSS}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks (self-capacitance mode)	-	-	400	pF
$RCx_{\_SELF}$	Series (in-line) resistance of all self capacitance pins in self capacitance mode	0[i]	0.47	10[ii]	kΩ

3.3 ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[iii]	± 2000	V

[i] Nominal series resistance of 470Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection

[ii] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. R_{max} x C_{max} = $\frac{1}{(6x f_{xfer})}$ where "C" is the pin capacitance to Vss.

[iii] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

3.4 Current Consumption

Sensor Setup: Channels = 2
ATI Base = 80
ATI Target = 2600
F_{xfer} = 875kHz[i]

Interface Selection: Event mode

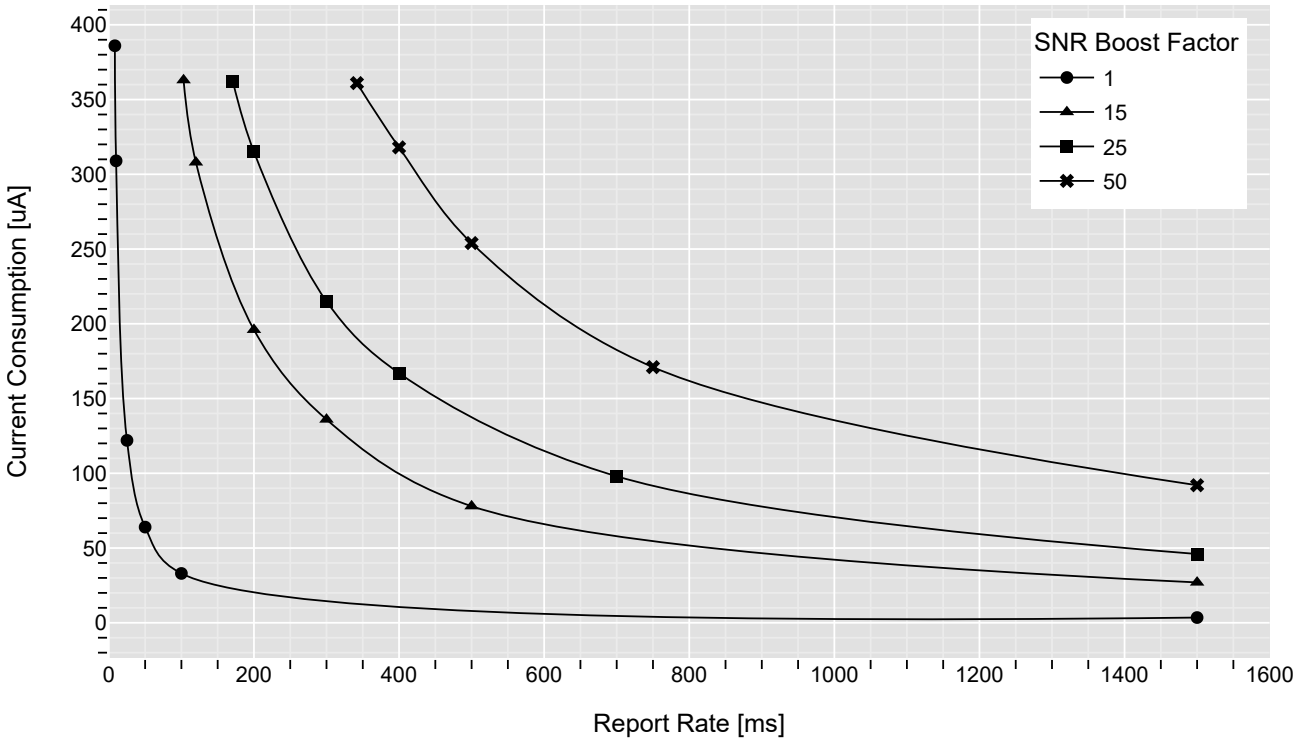


Figure 3.1: Report Rate vs Current Consumption at different SNR Boost Factors

[i]The report rate and current consumption will increase and decrease according to F_{xfer}

4 Noise Performance

Sensor Setup: Reference tracking = enabled
ATI Base = 80
ATI Target = 2600
F_{xfer} = 875kHz
Signal = 25fF

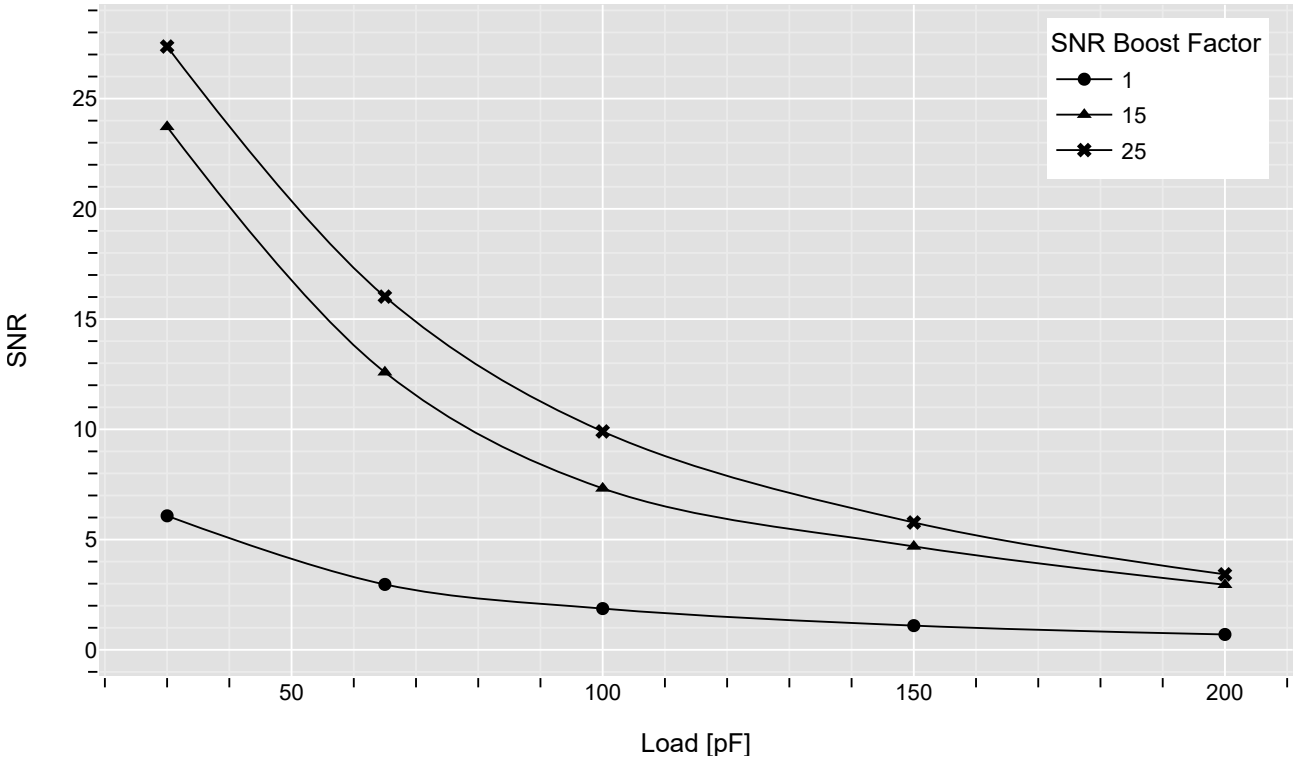


Figure 4.1: SNR vs Load Capacitance at various SNR Boost Factors and different Beta coefficients for a 25 fF signal[i]

[i] Using High SNR Boost Factors will cause a decrease in the dynamic resolution of the signal.

5 Timing and Switching Characteristics

5.1 Reset Levels

Table 5.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up/down level (Reset trigger) - slope >100V/s	1.040	1.353	1.568	V
V_{VREG}	Power-up/down level (Reset trigger) - slope >100V/s	0.945	1.122	1.304	V

5.2 MCLR Pin Levels and Characteristics

Table 5.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3V	VSS – 0.3	-	1.05	V
		VDD = 1.7V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3V	2.25	-	VDD + 0.3	V
		VDD = 1.7V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3V	-	-	15	ns
		VDD = 1.7V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

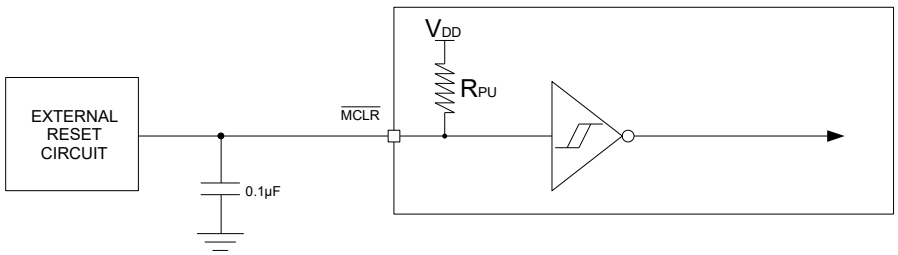


Figure 5.1: MCLR Pin Diagram

5.3 Miscellaneous Timings

Table 5.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	42	500-1500	5000	kHz

5.4 Digital I/O Characteristics

Table 5.4: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	SDA/OutA & SCL/OutB Output low voltage	I_{sink} = 20mA			0.3	V
V_{OL}	RDY/MCLR Output low voltage	I_{sink} = 10mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20mA	VDD - 0.2			V
V_{IL}	Input low voltage		VDD * 0.3			V
V_{IH}	Input high voltage				VDD * 0.7	V
C_{b_max}	SDA/OutA & SCL/OutB maximum bus capacitance				550	pF

5.5 I²C Characteristics

Table 5.5: I²C Characteristics

Parameter		Test Conditions	VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency		1.8V, 3.3V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START		1.8V, 3.3V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START		1.8V, 3.3V	0.26			µs
$t_{HD,DAT}$	Data hold time		1.8V, 3.3V	0			ns
$t_{SU,DAT}$	Data setup time		1.8V, 3.3V	50			ns
$t_{SU,STO}$	Setup time for STOP		1.8V, 3.3V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		1.8V, 3.3V	0		50	ns

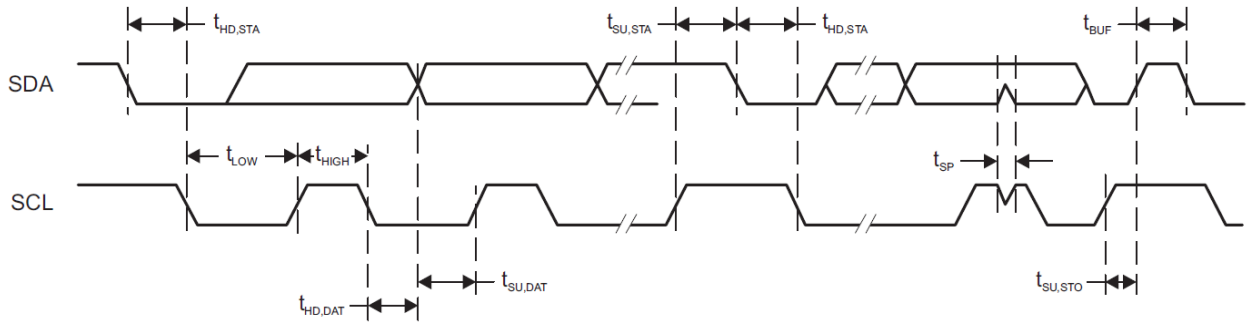


Figure 5.2: I²C Mode Timing Diagram

6 ProxFusion® Module

The IQS320 contains a single ProxFusion® module that uses patented technology to measure and process the sensor data.

6.1 Channel Options

The IQS320 is a dual channel self-capacitance sensor intended for SAR and other similar proximity applications.

- Dual self-capacitance channels
- Single self capacitance channel with reference channel

6.2 Count

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance. The counts are filtered with the SNR Boost UI which oversamples the raw counts to improve the SNR, as such the counts do not reflect the target counts set by the user. The counts are shifted with a DC offset to a counts value of 16383 after an ATI occurs to ensure that measurements with large amounts of oversampling do not encounter numerical overflow.

6.2.1 Max Counts

Each channel is limited to having a count value smaller than the configurable limit *(Max counts)*. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value. This max value refers to a single raw measurement before oversampling has been applied.

6.2.2 Linearise Counts

If the *Linearise* option is set the IQS320 linearises the counts before reporting them. If this option is set the counts are inverted and the *Invert* bit must be set to invert the channel logic.

6.3 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value known as the *LTA*. The LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

6.3.1 Reseed

Since the *LTA* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the *Reseed* bit in Table A.16.

6.4 Prox and Touch Thresholds

Each channel has its own independently adjustable *Prox* and *Touch* Thresholds. If the difference between the channel's *Counts* and *LTA* (also referred to as the *Delta* of the *Counts*), exceeds the thresholds, an event will be triggered. Once a channel enters a *Prox* or *Touch* state, the corresponding

flags in the *System Status* register will be updated. The events flags for *Prox* and *Touch* will be triggered on the entry and the exit of an event.

A channel will enter *Prox* if:

$$\textbf{Delta} > \textbf{Prox Threshold}$$

for more than the number of samples specified by *Prox Debounce Enter*. The channel will exit *Prox* if the above condition is not met for more than the number of samples set by *Prox Debounce Exit*.

A channel will enter *Touch* if:

$$\textbf{Delta} > \textbf{Touch Threshold}$$

and exit *Touch* if:

$$\textbf{Delta} < \textbf{Touch Threshold} - \textbf{Hysteresis}$$

Settings for the touch and proximity thresholds can be found in Table A.11 and Table A.12.

6.5 Event Timeout

When a proximity or touch event it triggered an event timeout will be fired. When the timeout is reached, a reseed event will occur which will bring the channel out of its proximity and touch events.

Settings for the proximity and touch timeouts can be found in Table A.17.

6.6 Filter Betas

An Infinite Impulse Response(IIR) filter is applied to the digitized raw input for both the counts value and the LTA.

Damping options for the counts filters, LTA filters and movement filters are defined in Table A.14 and Table A.15.

$$\textbf{Damping factor} = \frac{\textbf{Beta}}{\textbf{256}}$$

6.7 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductance, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

6.8 Automatic Re-ATI

6.8.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always

have this enabled. When a Re-ATI is performed the *ATI Event* status bit will be set. It is cleared when read by the master through I^2C.

6.8.2 Conditions for Re-ATI to Activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range around the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.8.

$$\textbf{Re-ATI Boundary} = \textbf{LTA snapshot} \pm \textbf{ATI Band}$$

The ATI algorithm executes in a short time, and therefore goes unnoticed by the user.

Note that I^2C communications are disabled for the duration of the ATI process.

6.8.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if the following is true for any channel after the ATI has completed:

- Counts are outside the **Re-ATI Boundary** upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set *(ATI Error)*. The flag status is only updated again when a new ATI algorithm is performed.

A Re-ATI will not be automatically triggered if an ATI Error occurs. If an ATI Error occurs the master should manually trigger a Re-ATI using the Re-ATI bit in Table A.16. Sampling will, however, continue with the suboptimal ATI parameters. There is no indication of an ATI error in standalone mode.

7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Only certain parameters are described below. The other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Reset Event* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *(ACK Reset)*. If it becomes set again, the master will know a reset has occurred, and can react appropriately.

7.2.2 Software Reset

The IQS320 can be reset by means of an I²C command *(Soft Reset)*.

7.2.3 Hardware Reset

The MCLR/RDY pin (active LOW) can be used to hard reset the device when outside an I²C communication window by pulling the pin low. For more details see Section 5.2.

8 Additional Features

8.1 Reference UI

The IQS320 implements a Reference Tracking User Interface (Reference UI).

A reference channel adjusts the counts of the primary sensing channel by subtracting the change in counts of the reference channel from the counts of the primary sensing channel. The change in counts of the reference channel is calculated by taking a snapshot of the LTA of the reference channel after the device completes an ATI routine and subtracting the counts of the reference channel from the snapshot.

The Reference UI is able to reduce the effects of sensor drift due to temperature. The Reference UI also has the ability to reduce noise that is common to both sensing and reference channels which improves the signal to noise ratio. The reference UI performs best when used in conjunction with the *SNR Boost UI*

There is a reference scaling multiplier and divider which will allow the user to compensate for any differences in the amount of drift between the sensing and the reference channel.

$$\mathbf{Counts}_{\mathbf{Adjusted}} = \mathbf{Counts} - (\mathbf{Counts}_{\mathbf{Ref}} - \mathbf{Counts}_{\mathbf{Ref\ LTA\ Snapshot}}) \times \frac{\mathbf{Multiplier}_{\mathbf{Ref}}}{\mathbf{Divider}_{\mathbf{Ref}}}$$

The reference channel sensor should be exposed to the same conditions and capacitive loads as the sensing channel, and the user should not be able to affect the counts of the reference channel.

When reference tracking is enabled, Channel 0 is the dedicated sensing channel and Channel 1 is the dedicated reference channel as illustrated in figure 8.1. Channel 0 and Channel 1 can be configured to be either CRx0/CTx0 or CRx1/CTx1.

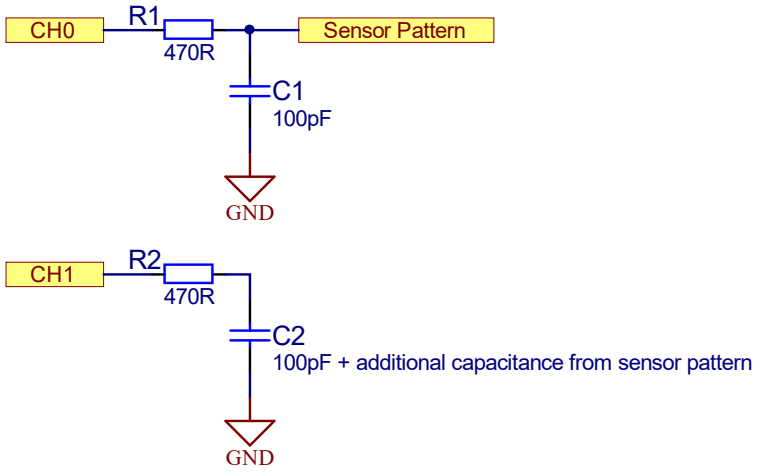


Figure 8.1: Example hardware schematic for Reference UI with 100pF load capacitor.

8.2 Movement UI

The IQS320 implements a Movement User Interface (Movement UI).

When a touch condition is entered and no movement is detected on the channel the channel will reseed once the touch timeout timer timeout is reached and the touch condition will be exited. Any movement will cause the timeout timer to reset, thereby keeping the channel in a touch condition.

The movement is calculated by subtracting a filtered version of the counts from the counts of the channel, which yields a pseudo-gradient function representing the movement. The damping factor used to calculate the movement can be set in Table A.15. A higher value will increase the sensitivity of the movement detector.

8.2.1 Movement Threshold

A movement event is triggered when the movement exceeds the movement threshold. Similar to the proximity threshold, the movement threshold uses debouncing to enter and exit a movement event. The movement settings can be found in table A.13.

8.3 SNR Boost UI

The IQS320 implements a Signal to Noise Ratio Boost User Interface (SNR Boost UI).

The signal to noise ratio is drastically improved by oversampling which decreases the quantisation noise while increasing the sampling resolution of the signal. Oversampling the signal will increase the sampling time and current consumption of the device. There is also a decrease in dynamic resolution at High SNR Boost Factors.

The SNR boost factor setting controls how many times the signal should be oversampled. SNR boost is disabled by setting the SNR boost factor to a value of 1. SNR boost factor values larger than 50 are not recommended.

8.4 Standalone Mode

The IQS320 is able to run in a standalone mode.

In standalone mode, InputA is used to toggle the touch event timeout. The timeout can be disabled by connecting InputA to VDD. If InputA is connected to VDD then the touch condition will never timeout and the device will remain in touch until the counts are no longer within the touch threshold. Connecting InputA to VSS will enable the touch event timeout. When the touch event timeout is reached, the LTA on that channel will reseed causing the channel to come out of the touch event[i].

The I^2C lines are used as digital outputs in standalone mode. SDA/OutA is a push-pull active high output and SCL/OutB is an open-drain active low output. These outputs will be active if a touch event occurs.

In standalone mode, an I^2C ready window will occur once on startup to allow the user to enter an I^2C debugging mode where ther user can access the settings and stream data as if in I^2C streaming mode. To enter the debugging mode, write 0xC0 to register *0x70* in the startup window. The device can be set back into standalone mode from the I^2C debugging mode and will retain any settings written to it.[ii]

8.4.1 ATI Indication

ATI indication can be enabled on the IQS320 device in standalone mode. SDA/OutA and SCL/OutB will be active while an ATI is active. An ATI event will always occur on startup which will indicate that the device is powered on. This can be enabled or disabled by writing to the ATI indication bit in *0x70*.

[i] Do not leave InputA in a floating state.
[ii] After the device exits debugging mode, a reset or power cycle is required to start another debugging session

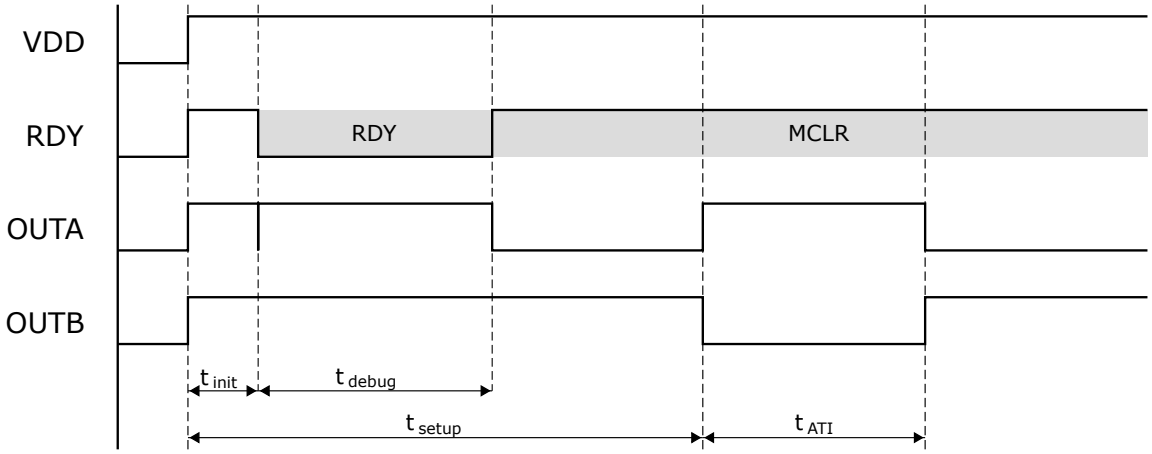


*Figure 8.2: Power On Sequence Specification with ATI indication **enabled***

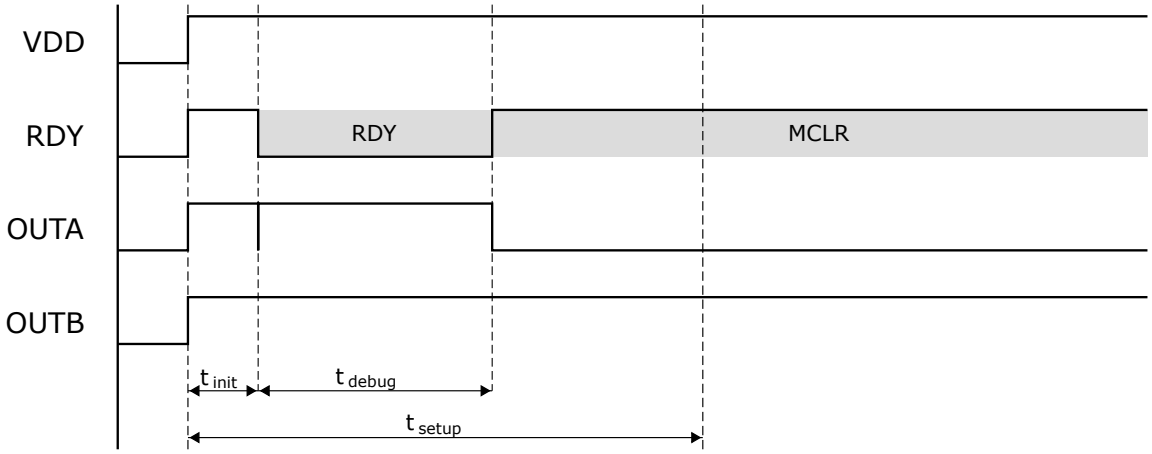


*Figure 8.3: Power On Sequence Specification with ATI indication **disabled***

Timing Parameter	Nominal	Tolerance	Unit
Initialisation	10.0	-	ms
Setup	361.5	-	ms
Debug window	208.5	-	ms
ATI	220.0	±20	ms

8.5 Watchdog Timer

The IQS320 implements a hardware watchdog timer. The watchdog timer is set to expire after 255ms if not kicked and will trigger a software reset upon expiration.

During I^2C communication the watchdog timer is reset whenever a read or write occurs. Therefore, if the master initiates communication by sending an I^2C START condition and does not complete the I^2C transaction then after 255ms the IQS320 will reset.

The I^2C transaction is completed either when an I^2C STOP notification is sent by the master or when the master ends the communication as described in Section 9.8.

9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The RDY pin also serves as a Master Clear (MCLR) and can be used to hard reset the device (Section 7.2.3). Byte level clock stretching is allowed. The communications interface of the IQS320 supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS320 implements 8-bit addressing with 2 bytes at each address.

9.2 I²C Address

The 7-bit device address is 0x47 ('01000111') with an alternate address which is 0x48 ('01001000'). The full address byte for address 0x47 will thus be 0x8F (read) or 0x8E (write) and the full address byte for address 0x48 will thus be 0x91 (read) or 0x90 (write)[i].

The device will check if InputA is set to VSS or VDD[ii]. If it is set to VSS it will choose to use address 0x47 and if it is set to VDD then it will choose to use address 0x48. This check is only performed on start up and the state of InputA will not affect the device address after startup.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words meaning that two bytes are stored at each address. For example, address 0x10 will provide two bytes. The next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

9.5 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and initiate I²C reads accordingly.

The RDY line allows the master MCU to be woken from low-power/sleep when user presence is detected by the touch device. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

[i] The device will also acknowledge an I²C address of 0x46 for address 0x47 and 0x49 for address 0x48. Writing to this address will cause the IQS320 to enter a low level debugging mode and should not be done under normal operating conditions. Therefore, both 0x47 and 0x46 or 0x48 and 0x49 are reserved on the I²C bus when using the IQS320.

[ii] Do not leave InputA in a floating state.

On the IQS320 the RDY line also serves as an MCLR pin. MCLR functionality is described in Section 7.2.3.

9.6 Communications Window

When the device has data for the master, it will pull the RDY line LOW. This indicates that the device has opened its *communications window* and is expecting the master to address it. When the communication window is closed the RDY line is released. For information on when the communications window is closed see section 9.8.

Transfer of data between the master and slave must occur during the communications window (RDY is LOW). If the master wishes to initiate communication, a *Force Communications Request* must be made, after which the master should wait for the slave to pull RDY LOW before attempting to read or write. Section 9.11.2 describes the *Force Communications Request* sequence.

9.7 I²C Transaction Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH) and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be missed/lost. The default I²C timeout period is set to 200ms and can be adjusted in register *0x72*. The I²C transaction timeout period should be set between 2ms and 230ms. The *I²C transaction timeout* is measured from the start of the communications window (RDY goes LOW).

Once communication between the master and the IQS320 has begun (START condition on I²C lines), the I²C transaction timeout is disabled leaving the watchdog timer in control. For more information on the behavior of the device under these conditions see Section 8.5.

9.8 Terminate Communication

A standard I²C STOP will close the current communication window.

If the stop bit disable bit (*Stop Bit Disable*) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF) shown in figure 9.1.

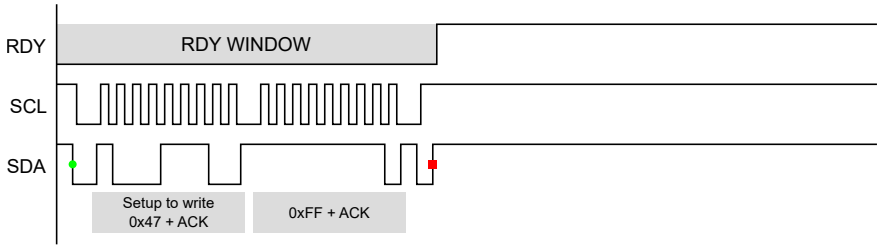


Figure 9.1: Force Stop Communication Sequence

9.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.

- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

9.10 I²C Interface

The IQS320 has 2 *Interface Types*, as described in the sections below.

9.10.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant report rate specified in register *0x71*.

9.10.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (Event mode). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs.

9.11 Event Mode Communication

For event mode to function correctly the following requirements must be met:

- Required events must first be enabled from the *Events Enable* register.
- Enabled events must be serviced by reading from the *System Status* register (0x10) to ensure all event flags are cleared. If these flags are not cleared continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode.

9.11.1 Events

Events can be individually enabled to trigger communication, bit definitions can be found in *System Status*.

Using the *Events Enable* register the following events can be enabled:

Table 9.1: Events Descriptions

Event	Trigger Condition
ATI Error	There has been an error during the ATI process
ATI Event	ATI has been triggered
Movement	There has been a transition of the movement state for either channels
Touch	There has been a transition of the touch state for either channels
Prox	There has been a transition of the prox state for either channels

9.11.2 Force Communication

In streaming mode, the IQ320 I²C will provide Ready (RDY) windows at intervals specified by the power mode report rate. Ideally, communication with the IQS320 should only be initiated in a RDY window. A communication request described in the figure below will force a RDY window to open. In event mode RDY windows are only provided when an event is reported. A RDY window must be

requested to write or read settings outside of this provided window. The time between the communication request and the opening of a RDY window (t_{wait}) is typically less than 0.5ms.[iii]

Communications has a higher priority than sampling on the IQS320. If forced communications occurs while the data is being sampled, the current data sample will be discarded and the previous sample will be retained. The period between force communications should be an integer multiple or longer than the sampling rate.

The communication request sequence is shown in figure 9.2.

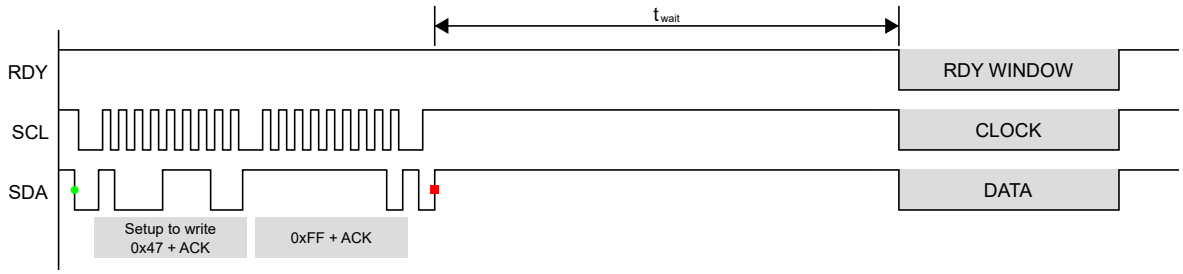


Figure 9.2: Force Communication Sequence

[iii] Only applicable for *Default Configuration 200*

10 Memory Map Register Descriptions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	See Table A.1
Read Only	**System Information**	
0x10	Systems Status	See Table A.2
0x11	Channel 0 Filtered Counts	16-bit value
0x12	Channel 1 Filtered Counts	
0x13	Channel 0 LTA	
0x14	Channel 1 LTA	
0x15	Channel 0 Movement	
0x16	Channel 1 Movement	
0x17	Channel 0 Pre Reference Tracking	
0x18	Channel 1 Pre Reference Tracking	
0x19	Channel 0 Raw	
0x1A	Channel 1 Raw	
0x1B	Channel 0 Post ATI Snapshot	
0x1C	Channel 1 Post ATI Snapshot	
Read/Write	**Sensor 0 Setup**	
0x20	Sensor Setup 0	See Table A.3
0x21	Conversion Frequency Setup	See Table A.4
0x22	Prox Control	See Table A.5
0x23	Timing Generator Control & Prox Input	See Table A.6
0x24	Inactive Rxs & Calibration Capacitor Selection	See Table A.7
0x25	ATI Setup	See Table A.8
0x26	ATI Base	16-bit value
0x27	ATI Multipliers and Dividers	See Table A.9
0x28	ATI Compensation	See Table A.10
Read/Write	**Sensor 1 Setup**	
0x30	Sensor Setup 0	See Table A.3
0x31	Conversion Frequency Setup	See Table A.4
0x32	Prox Control	See Table A.5
0x33	Timing Generator Control & Prox Input	See Table A.6
0x34	Pad Control and Calibration Capacitor Selection	See Table A.7
0x35	ATI Setup	See Table A.8
0x36	ATI Base	16-bit value
0x37	ATI Multipliers Selection	See Table A.9
0x38	ATI Compensation	See Table A.10
Read/Write	**Channel 0 Setup**	
0x40	Prox Settings	See Table A.11
0x41	Touch Settings	See Table A.12
0x42	Movement Settings	See Table A.13
Read/Write	**Channel 1 Setup**	
0x50	Prox Settings	See Table A.11
0x51	Touch Settings	See Table A.12
0x52	Movement Settings	See Table A.13
Read/Write	**Filter Betas**	
0x60	Counts Filter Beta & LTA Filter Beta	See Table A.14
0x61	LTA Fast Filter Beta & Movement Beta	See Table A.15
0x62	Fast Filter Band	16 bit value
Read/Write	**System Control**	
0x70	System Control	See Table A.16

0x71	Report Rate	16-bit value (ms) Range: 0 - 3000
0x72	I^2C Transaction Timeout	16 bit value (ms) Range: 2 - 230
0x73	Event Timeouts	See Table A.17
0x74	Events Enable & SNR Boost Factor	See Table A.18
0x75	Reference Scaling	See Table A.19
Read/Write	**I^2C Low Level Settings**	
0x80	I^2C Setup	See Table A.20

11 Ordering Information

11.1 Ordering Code

IQS320 zzz ppb

IC NAME	IQS320	=	IQS320	
DEFAULT CONFIGURATION	zzz	=	100	I^2C
		=	200	I^2C^i
PACKAGE TYPE	pp	=	CS	WLCSP-11 package
		=	DN	DFN-12 package
BULK PACKAGING	b	=	R	WLCSP-11 Reel (3000pcs/reel) DFN-12 Reel (6000pcs/reel)

Figure 11.1: Order Code Description

11.2 Top Marking

11.2.1 WLCSP11 Package

- IQS320
  pppxx

Product Name
ppp = product code
xx = batchcode

11.2.2 DFN12 Package Marking Option 1

- IQS320
  pppxx

Product Name
ppp = product code
xx = batchcode

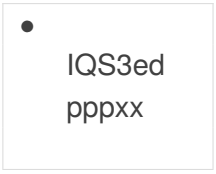
11.2.3 DFN12 Package Marking Option 2

- IQS3dd
  pppxx

Product Name
ppp = product code
xx = batchcode

[i] Improved force communications response time

11.2.4 DFN12 Package Marking Option 3



Product Name
ppp = product code
xx = batchcode

12 Package Specification

12.1 Package Outline Description - WLCSP11

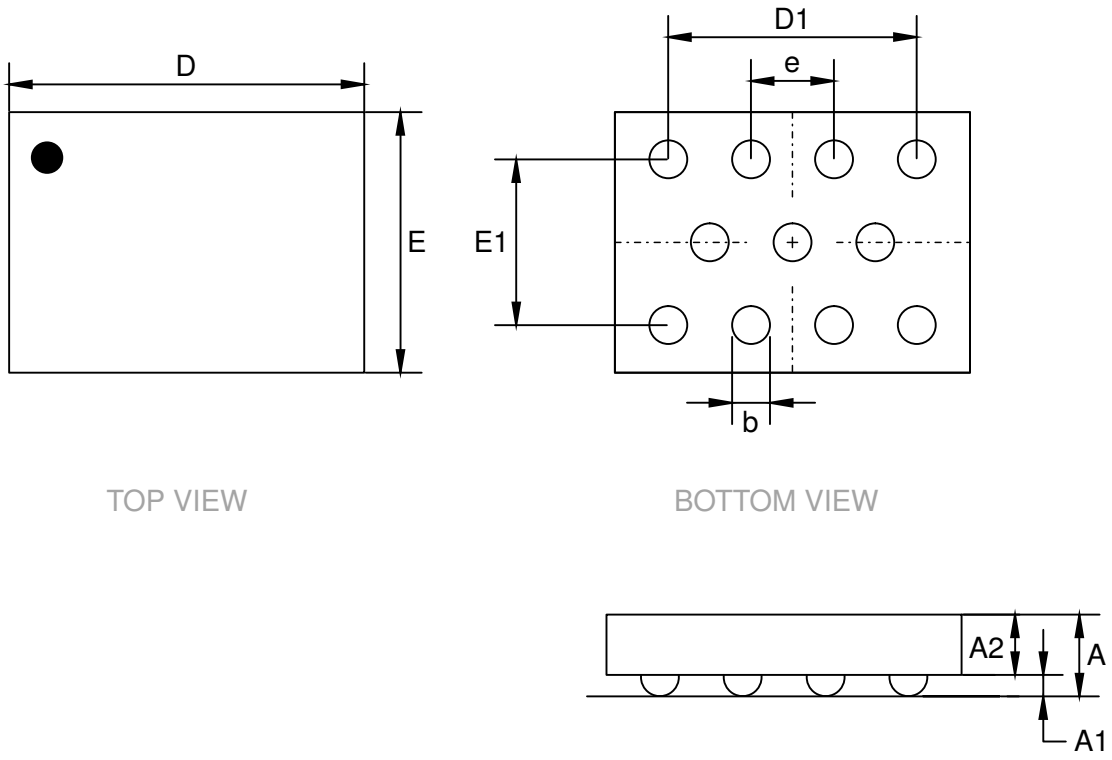


Figure 12.1: WLCSP (1.48x1.08) - 11 Package Outline Visual Description

Table 12.1: WLCSP (1.48x1.08) - 11 Package Outline Visual Description (mm)

Dimension	Min	Nom	Max
A	0.303	0.345	0.387
A1	0.076	0.090	0.104
A2	0.205	0.230	0.255
D	1.46	1.48	1.50
E	1.06	1.08	1.10
D1		1.05 BSC	
E1		0.700 BSC	
b	0.136	0.160	0.184
e		0.350 BSC	

12.2 Package Outline Description - DFN12

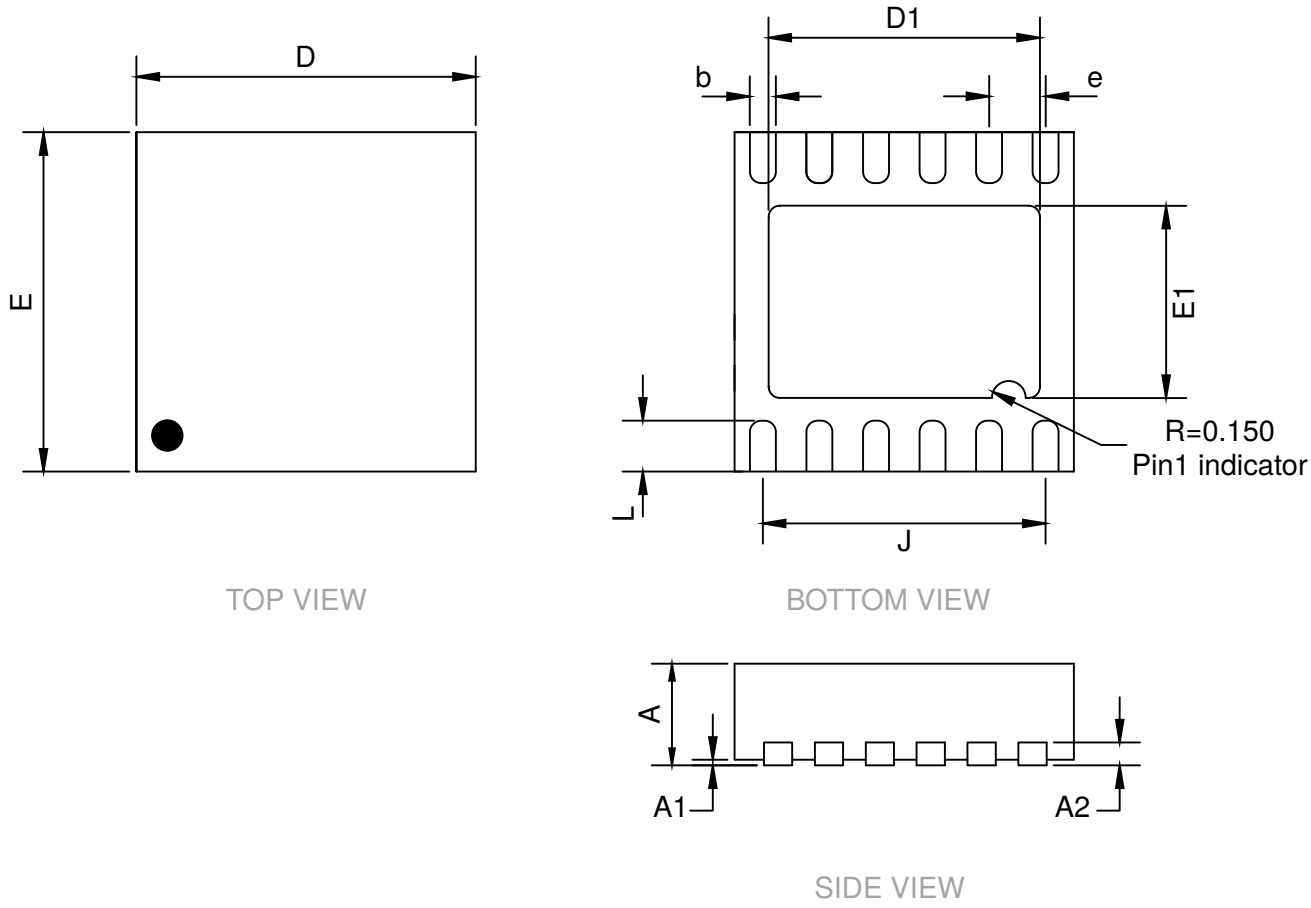
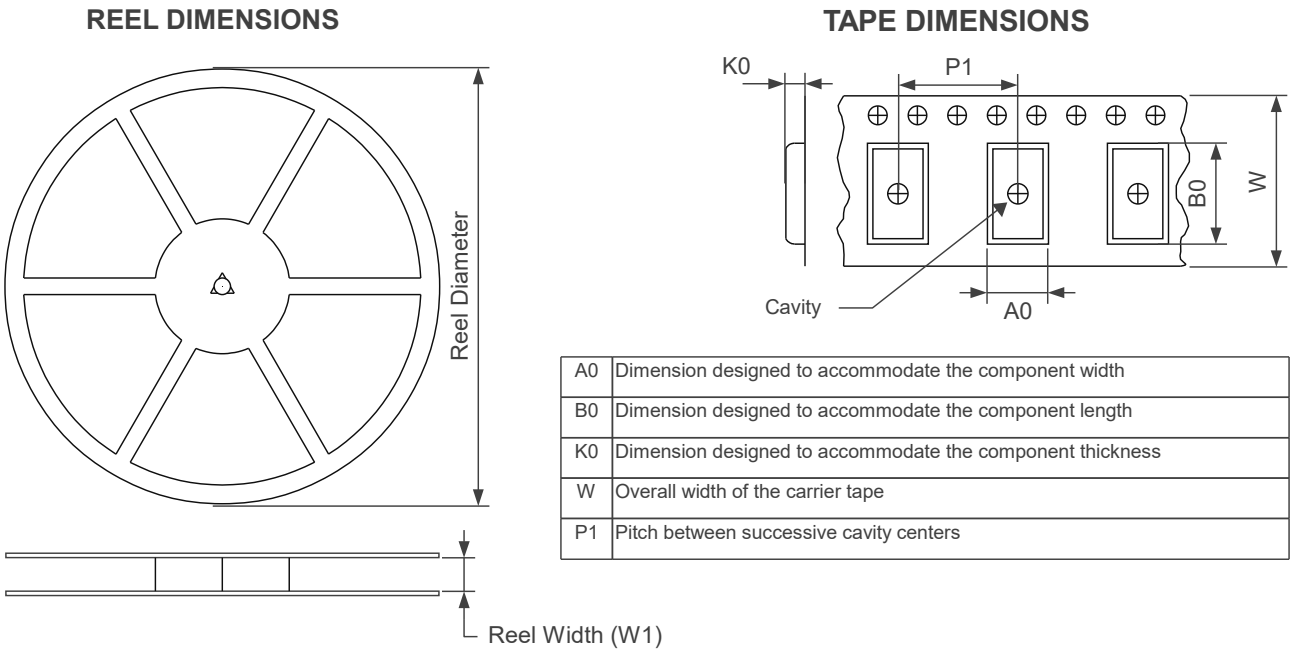


Figure 12.2: DFN (3x3)-12 Package Outline Visual Description

Table 12.2: DFN (3x3)-12 Package Outline Visual Description (mm)

Dimension	Min	Nom	Max
A	0.700	0.750	0.800
A1	0.000		0.050
A2		0.203 REF	
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	2.35	2.40	2.45
E1	1.65	1.70	1.75
J		2.50 REF	
L	0.400	0.450	0.500
b	0.180	0.230	0.280
e		0.500 BSC	

12.3 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 12.3: Tape and Reel Specification

Table 12.3: Tape and reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
WLCSP11	11	179	8.4	1.35	1.75	0.5	4	8	Q2
DFN12	12	330	12.4	3.3	3.3	1.1	8	12	Q1

A Memory Map Descriptions

Please note: The value of all Read-Write bits marked as Reserved, unless otherwise specified, can be set to 0 or 1 depending on customer's preference.

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Catergory	Name	Value	Order Code	
0x00	Application Version Info	Product Number	1304		16-bit value
0x01		Major Version	1		
0x02		Minor Version	0	100	
			1	200	
0x03		Patch Number (commit hash)	Reserved		
0x04					
0x05	ROM Library Version Info	Library Number	Reserved		
0x06		Major Version	Reserved		
0x07		Minor Version	Reserved		
0x08		Patch Number (commit hash)	Reserved		
0x09					

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Res-erved	Res-erved	CH1 Move-ment	CH1 Touch	CH1 Prox	CH0 Move-ment	CH0 Touch	CH0 Prox	Res-erved	Reset Event	ATI Error	ATI Active	ATI Event	Move-ment Event	Touch Event	Prox Event

- Bit 13-8: **CHx Touch/Prox/Movement**
  For CHx Movement
  - 0: CHx not in Movement
  - 1: CHx in Movement

  For CHx Touch
  - 0: CHx not in Touch
  - 1: CHx in Touch

  For CHx Prox
  - 0: CHx not in Prox
  - 1: CHx in Prox
- Bit 6: **Reset Event**
  - 0: No Reset Event occurred
  - 1: Reset Event occurred
- Bit 5: **ATI Error**
  - 0: No ATI Error occurred
  - 1: ATI Error occurred
- Bit 4: **ATI Active**
  - 0: No ATI routine active
  - 1: ATI routine active
- Bit 3: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 2: **Movement Event**
  - 0: No Movement Event occurred
  - 1: Movement Event occurred
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

Table A.3: Sensor Setup 0

Register: 0x20, 0x30

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	CalCap Rx	CalCap Tx	0	0	0	CTx1	CTx0	Reserved				Move-ment En-able	Invert	Dual Direct	Linear-ise Counts

- Bit 14: **CalCap Rx**
  - 0: CalCap Rx not selected
  - 1: CalCap Rx selected
- Bit 13: **CalCap Tx**
  - 0: CalCap Tx not selected
  - 1: CalCap Tx selected
- Bit 9-8: **CTxx**
  - 0: CTxx disabled
  - 1: CTxx enabled
- Bit 2: **Movement Enable**
  - 0: Movement disabled
  - 1: Movement enabled
- Bit 2: **Invert**
  - 0: Do not invert channel logic
  - 1: Invert channel logic
- Bit 1: **Dual Direction**
  - 0: Single direction thresholds
  - 1: Dual direction thresholds
- Bit 0: **Linearise Counts**
  - 0: Do not Linearise counts
  - 1: Linearise counts

Table A.4: Conversion Frequency Setup

Register: 0x21, 0x31

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 15-8: **Conversion Frequency Period**
  - The charge transfer frequency f_{xfer} is determined by the values of the Conversion Frequency Fraction and the Conversion Frequency Period. The required value of the Conversion Frequency Period is dependent on the dead time enabled bit (See Table A.6).
  - Dead time disabled:
    - $f_{xfer} = \frac{f_{osc}}{2 \times period + 2}$
  - Dead time enabled:
    - $f_{xfer} = \frac{f_{osc}}{2 \times period + 3}$
  - Range: 0 - 127
- Bit 7-0: **Conversion Frequency Fraction**
  - Set to 127
- For F_{OSC} = 14MHz, a fixed conversion frequency fraction of 127 and dead time enabled, the following values of the conversion frequency period are recommended and will result in the indicated conversion frequency:
  - 1: 2MHz
  - 5: 1MHz
  - 6: 875kHz
  - 12: 500kHz
  - 17: 350kHz
  - 26: 250kHz
  - 53: 125kHz

Table A.5: Prox Control

Register: 0x22, 0x32

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0v5 Dis-charge	0	Cs Size	0	0	S/H Bias Select		Max Counts		0	0	0	0	0	0

- Bit 14: **0v5 Discharge**
  - 0: Disabled
  - 1: Enabled
- Bit 12: **Cs Size**
  - 0: Use 40pF Cs
  - 1: Use 80pF Cs
- Bit 9-8: **S/H Bias Select**
  - 00: 2µA
  - 01: 5µA
  - 10: 7µA
  - 11: 10µA
- Bit 7-6: **Max Counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095 (recommended)
  - 11: 16383

Table A.6: Timing Generator Control & Prox Input

Register: 0x23, 0x33

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	Calibration Cap Select	0	Rx1	Rx0	1	Dead Time En-able	Res-erved	0	0	0	1	1

- Bit 11: **Calibration Capacitor Select**
  - 0: Calibration Capacitor enabled
  - 1: Calibration Capacitor disabled
- Bit 9-8: **Rxx**
  - 0: Rxx Disabled
  - 1: Rxx Enabled
- Bit 6: **Dead Time Enable**
  - 0: Dead Time Disabled
  - 1: Dead Time Enabled

Table A.7: Inactive Rxs & Calibration Capacitor Selection

Register: 0x24, 0x34

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Calibration Capacitor				Inactive Rxs			

- Bit 7-4: **Calibration Capacitor**
  - Calibration Capacitor size = 0.5pF × Calibration Capacitor
  - Max value = 7 (Calibration Capacitor size = 3.5pF)
- Bit 3-0: **Inactive Rxs**
  - Selects state of CX's when not in use
  - 0x00: Floating
  - 0x05: Bias voltage
  - 0x0A: VSS
  - 0x0F: VREG

Table A.8: ATI Setup

Register: 0x25, 0x35

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Resolution Factor												ATI Band	ATI Mode		

- Bit 15-4: **ATI Resolution Factor**
  - ATI TARGET = ACTUAL ATI BASE $\times \frac{\text{ATI Resolution Factor}}{16}$
- Bit 3: **ATI Band**
  - 0: Small ATI Band = $(\frac{1}{16} \times \text{ATI TARGET} \times \text{SNR Boost Factor})$
  - 1: Large ATI Band = $(\frac{1}{8} \times \text{ATI TARGET} \times \text{SNR Boost Factor})$
- Bit 2-0: **ATI Mode**
  - 000: Disabled
  - 001: Compensation Only
  - 010: ATI from Compensation Divider
  - 011: ATI from Fine Fractional Divider
  - 100: Full

Table A.9: ATI Multipliers and Dividers

Register: 0x27, 0x37

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Fine Fractional Multiplier		Fine Fractional Divider						Coarse Fractional Multiplier				Coarse Fractional Divider			

Table A.10: Compensation

Register: 0x28, 0x38

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Reserved	Compensation									

Table A.11: Prox Settings

Register: 0x40, 0x50

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Prox Debounce Exit				Prox Debounce Enter				Prox Threshold							

- Bit 15-12: **Prox Debounce Exit**
  - 0000: Prox Debounce Exit disabled
  - Number of debounce conversions on Prox Exit (4-bit value)
- Bit 11-8: **Prox Debounce Enter**
  - 0000: Prox Debounce Enter disabled
  - Number of debounce conversions on Prox Enter (4-bit value)
- Bit 7-0: **Prox Threshold**
  - 8 bit value

Table A.12: Touch Settings

Register: 0x41, 0x51

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 15-12: **Touch Hysteresis**
  - Touch Hysteresis Counts = $\frac{\text{Touch Hysteresis}}{256} \times$ Touch Threshold Counts
- Bit 7-0: **Touch Threshold**
  - Let k = Post ATI Counts Snapshot $\times$ SNR Boost Factor
  - Touch Threshold Counts = $\begin{cases} k \times \frac{\text{Touch Threshold}}{256} & \text{if } k < 16383 \\ 16383 \times \frac{\text{Touch Threshold}}{256} & \text{if } k \geq 16383 \end{cases}$

Table A.13: Movement Settings

Register:	0x42, 0x52															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Movement Debounce Exit				Movement Debounce Enter				Movement Threshold							

- Bit 15-12: **Movement Debounce Exit**
  - 0000: Movement Debounce Exit disabled
  - Number of debounce conversions on Movement Exit (4-bit value)
- Bit 11-8: **Movement Debounce Enter**
  - 0000: Movement Debounce Enter disabled
  - Number of debounce conversions on Movement Enter (4-bit value)
- Bit 7-0: **Movement Threshold**
  - 8 bit value

Table A.14: Counts Filter Beta & LTA Filter Beta

Register:	0x60															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Beta								Counts Beta							

Table A.15: LTA Fast Filter Beta & Movement Beta

Register:	0x61															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Movement Beta								LTA Fast Beta							

Table A.16: System Control

Register:	0x70															
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								ATI indication	Track Reference	Interface Type		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 7: **ATI Indication**
  - 0: ATI indication disbaled
  - 1: ATI indication enabled
- Bit 6: **Reference Tracking**
  - 0: Reference tracking disbaled
  - 1: Reference tracking enabled
- Bit 5-4: **Interface Selection**
  - 10: Standalone
  - 01: I^2C Events
  - 00: I^2C Streaming
- Bit 3: **Reseed**
  - 0: No Reseed
  - 1: Trigger Reseed
- Bit 2: **Re-ATI**
  - 0: No Re-ATI
  - 1: Trigger Re-ATI
- Bit 1: **Soft Reset**
  - 0: No Soft Reset
  - 1: Trigger Soft Reset
- Bit 0: **ACK Reset**
  - 0: No ACK Reset
  - 1: ACK Reset

Table A.17: Event Timeouts

Register:	0x73													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Prox Event Timeout								Touch Event Timeout							

- Bit 15-8: **Prox Event Timeout**
  - Prox Event Timeout = Prox Event Timeout × 512ms
  - Set to 0 to disable
  - Maximum value: 127
- Bit 7-0: **Touch Event Timeout**
  - Touch Event Timeout = Touch Event Timeout × 512ms
  - Set to 0 to disable
  - Maximum value: 127

Table A.18: Events Enable & SNR Boost Factor

Register:	0x74													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SNR Boost Factor								0	0	ATI Error	0	ATI Event	Move-ment Event	Touch Event	Prox Event

- Bit 15-8: **SNR Boost Factor**
  - Recommended values: 1-50
- Bit 5: **ATI Error Mask**
  - 0: ATI error disabled
  - 1: ATI error enabled
- Bit 3: **ATI Event Mask**
  - 0: ATI event disabled
  - 1: ATI event enabled
- Bit 2: **Movement Event Mask**
  - 0: Movement event disabled
  - 1: Movement event enabled
- Bit 1: **Touch Event Mask**
  - 0: Touch event disabled
  - 1: Touch event enabled
- Bit 0: **Prox Event Mask**
  - 0: Prox event disabled
  - 1: Prox event enabled

Table A.19: Reference Scaling

Register:	0x75													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reference Divider								Reference Multiplier							

- Bit 15-8: **Reference Multiplier**
- Bit 7-0: **Reference Divider**

Table A.20: I2C Settings

Register:	0x80													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														R/W Check Dis-able	Stop Bit Dis-able

- Bit 1: **Read/Write Check Disable**
  - 0: Read/Write Check enable
  - 1: Read/Write Check disabled
- Bit 0: **Stop Bit Disable**
  - 0: Stop Bit enabled
  - 1: Stop Bit disabled

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