IQS370 Overview

Quadrature mutual-inductive I²C sensing controller. Computes a temperature-stable position or angle. Resistant to external common-mode interferences.

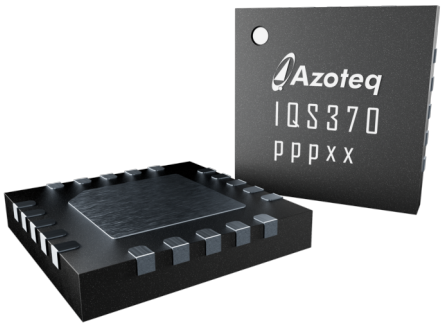
1 Device Overview

The IQS370 ProxFusion® IC is a two-channel I²C mutual-inductive sensing device. An absolute position or angle is calculated on chip. Measurements are stable against temperature drifts and external common-mode interferences following correct design procedures. Built-in routines are provided for the simple calibration of a sensor in factory. Error correction and/or custom response curves with a lookup table are provided. Noise filtering with fast movement responses and movement detection is configurable.

Typical sensor designs allow for 8-bit measurement resolution at 1 kHz report rates. Signal processing options are available to increase the resolution up to 11-bit at slower report rates. The sensor is fully I²C compatible, and the IQS370 responds effectively even when in a low-power mode.

1.1 Main Features

- External sensor options:
  - One absolute linear position sensor, or
  - One absolute angle sensor
- Built-in basic functions:
  - Calibration routines for in-factory calibration (external non-volatile memory required)
  - Design-time internal gain calibration
- Built-in signal processing options:
  - Slider or encoder position from sine/cosine sensors
  - Movement indication
  - Noise filtering with fast response to movement
  - Lookup table calibration, and/or
  - Lookup table custom functions (log, exponential, etc.)
- Low-power mode:
  - Automatic switching when no movement detected
  - Reduced functionality in lower power mode for ultra-low-power consumption
  - Automatic wake-up to normal operation on movement
  - Less than 15 µA at report rates of 250 ms for typical sensor designs when in low-power mode.
- Design simplicity:
  - Compatible with sensors of sizes ranging from 5–300 mm in length or diameter.
- Supply voltage range:
  - 1.71 V to 3.6 V
- Small package:
  - QFN20 (3 × 3 × 0.55 mm) – 0.4 mm pitch



QFN20 Package

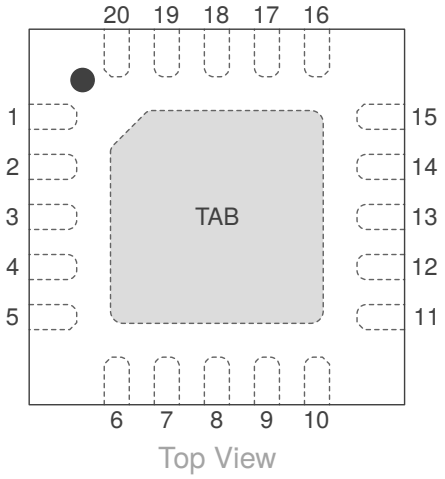
1.2 Applications

- Waterproof absolute position or angle sensing
- Sound or music equipment
- Low-power position or angle sensor applications
- Potentiometer replacement with I²C for digital UI systems

Contents

2 Hardware Connection

2.1 QFN20 Pin Diagram



Top View

Table 2.1: 20-pin QFN Package (Top View)

Pin no.	Signal	Pin no.	Signal
1	TxC	11	NC
2	RxB	12	NC
3	RxA	13	NC
4	NC	14	NC
5	NC	15	NC
6	VREG	16	NC
7	TxB	17	MCLR/RDY
8	VDD	18	TxA
9	VSS	19	SDA
10	NC	20	SCL

Area name	Signal
TAB[i]	Thermal pad (floating)

2.2 Signal Descriptions

Table 2.2: Signal Descriptions

Function	Signal Name	Signal Type	Pin Type[ii]	Description
ProxFusion®	RxB	Analog	I	ProxFusion® measurement input.
	RxA	Analog	I	
	TxA	Analog	O	ProxFusion® excitation signal output.
	TxB	Analog	O	
	TxC	Analog	O	
GPIO	MCLR/RDY	Digital	IO	Active pull-up — 200k resistor to VDD. Pulled low during Power-on Reset (POR[iii]), and MCLR function enabled by default.
I²C	SDA	Digital	IO	I²C Data
	SCL	Digital	IO	I²C Clock
Power	VDD	Power	P	Input supply voltage.
	VREG	Power	P	Internal regulated supply output.
	VSS	Power	P	Analog and digital ground.

[i] It is recommended to connect the thermal pad (TAB) to VSS.
[ii] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power
[iii] POR is used to reference a clean reset state after power-on.

2.3 Reference Schematic

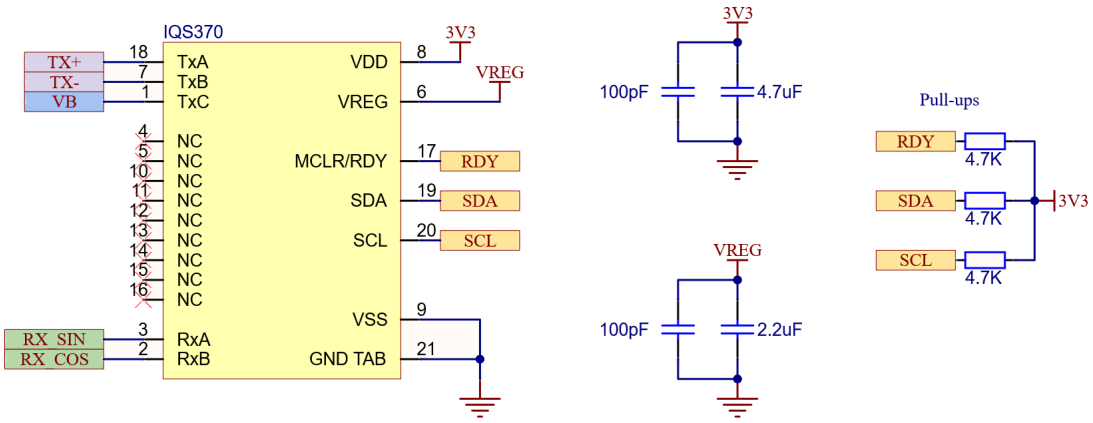


Figure 2.1: IQS370 Connections, Communication and Power Decoupling Reference Schematic

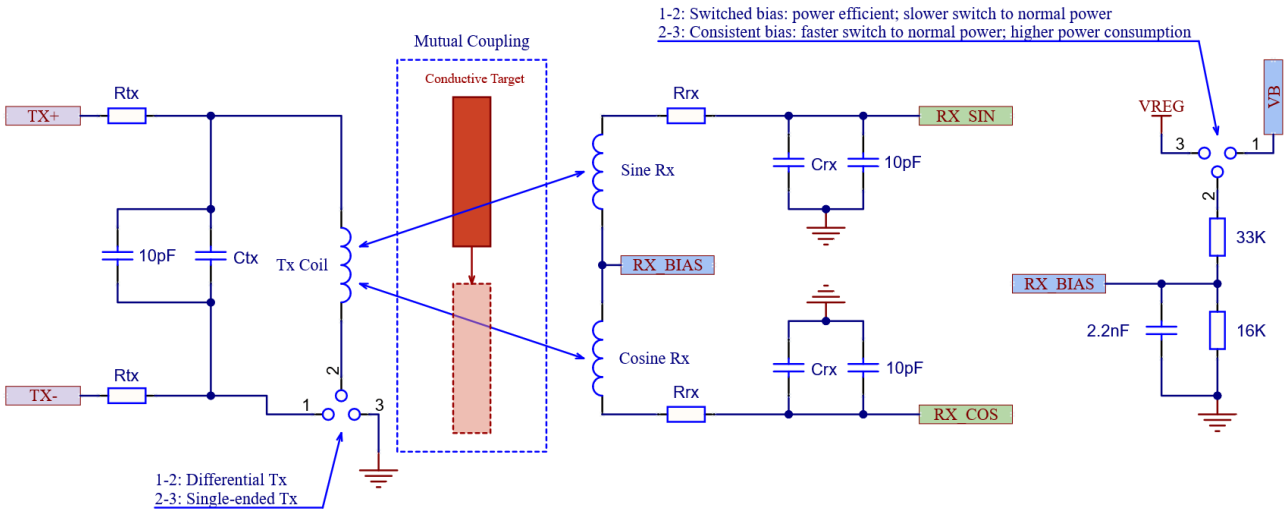


Figure 2.2: Sensor Reference Schematic

3 Block Diagram

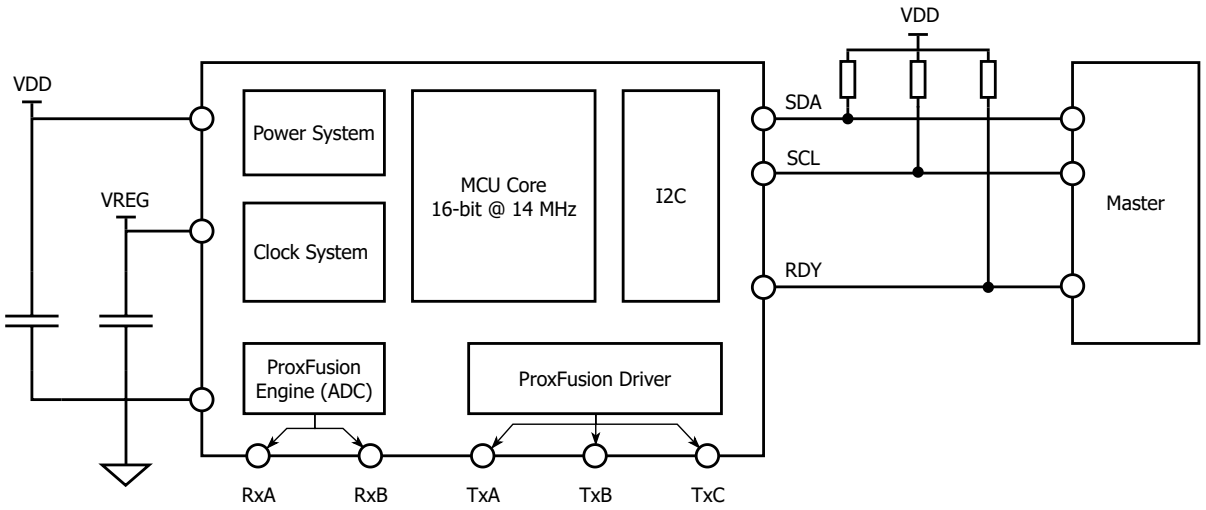
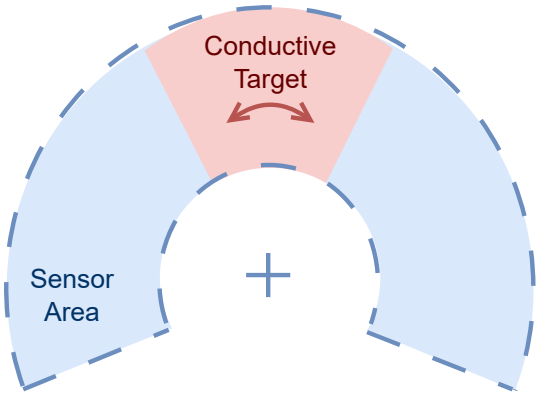


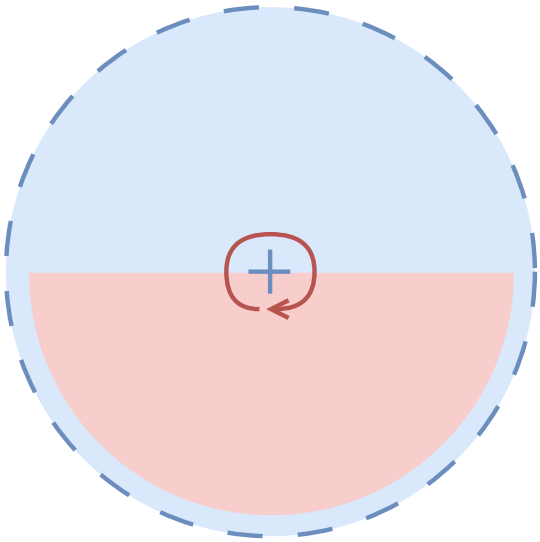
Figure 3.1: Functional Block Diagram

4 Supported Sensors

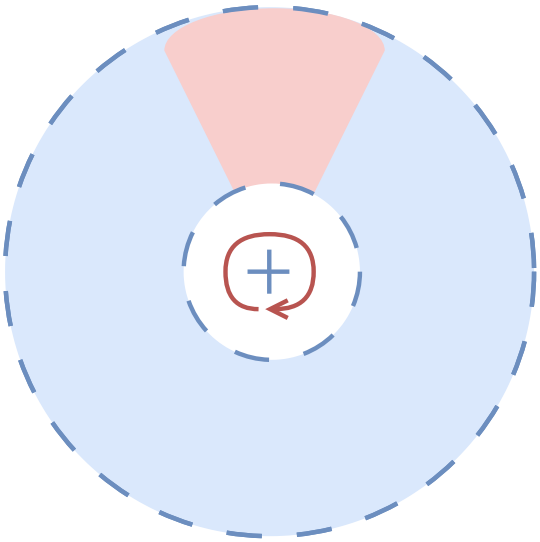
Arc Slider Sensor



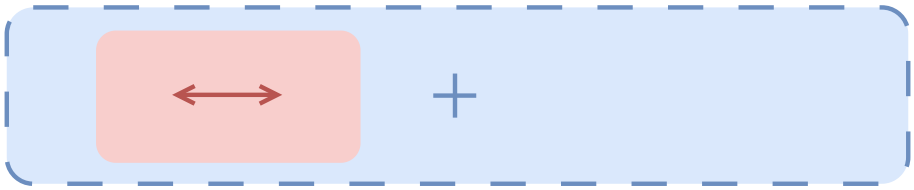
Full Area Encoder Sensor



Partial Area Encoder Sensor



Linear Slider Sensor



5 Electrical Characteristics

5.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	-40	85	°C

5.2 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.6	V
VREG	Internal regulated supply output for analog domain		1.53		V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T_A	Operating free-air temperature	−40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREG}$	$3\times C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR≤ 200 mΩ	2[i]	5	13	µF

5.3 ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[ii]	± 2000	V

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to the AZD004 application note for more information regarding capacitor derating.

[ii] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

6 Timing and Switching Characteristics

6.1 Reset Levels

Table 6.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

6.2 MCLR Pin Levels and Characteristics

Table 6.2: MCLR Pin Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

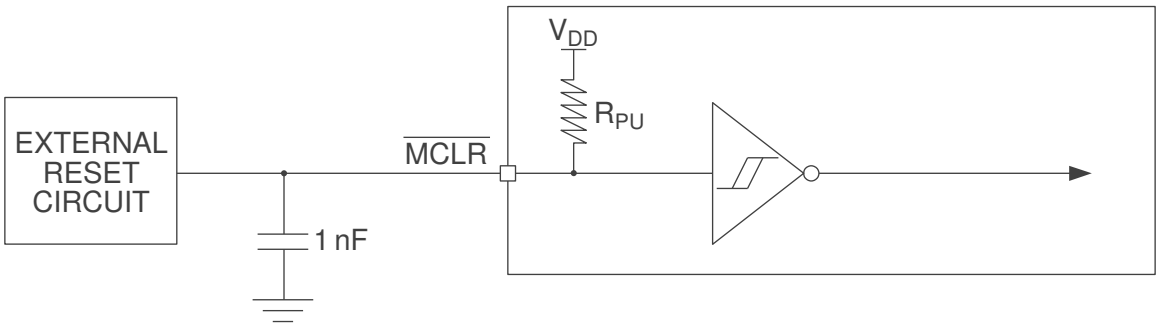


Figure 6.1: MCLR Pin Diagram

6.3 Digital I/O Characteristics

Table 6.3: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL Output low voltage	I_{sink} = 20 mA		0.3	V
V_{OL}	TxA Output low voltage TxB Output low voltage	I_{sink} = 10 mA		0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2		V
V_{IL}	Input low voltage			VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7		V
C_{b_max}	SDA & SCL maximum bus capacitance			550	pF

6.4 I²C Characteristics

Table 6.4: I²C Characteristics

Parameter		VDD	Min	Max	Unit
f_{SCL}	SCL clock frequency	1.8 V, 3.3 V		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	1.8 V, 3.3 V	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	1.8 V, 3.3 V	0.26		µs
$t_{HD,DAT}$	Data hold time	1.8 V, 3.3 V	0		ns
$t_{SU,DAT}$	Data setup time	1.8 V, 3.3 V	50		ns
$t_{SU,STO}$	Setup time for STOP	1.8 V, 3.3 V	0.26		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	1.8 V, 3.3 V	0	50	ns

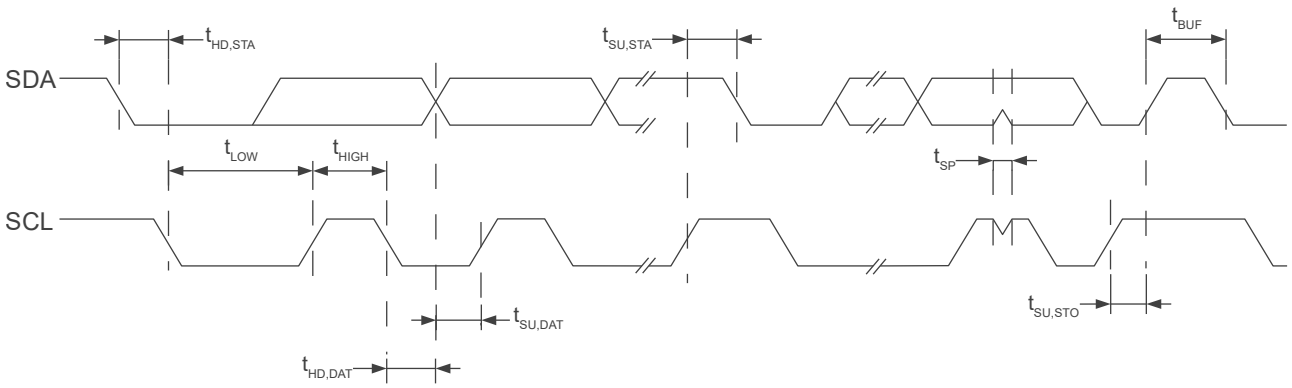


Figure 6.2: I²C Mode Timing Diagram

7 I²C Interface

7.1 Device Resets

When a device boots, the RDY line briefly acts as an open-drain reset line (active low). When the RDY line is kept low after power-on, the IQS370 device will remain in reset and will not respond to I²C communication. Normal operation ensues once the RDY line is left to go high.

The device will indicate whether it has reset via the *Reset* bit in the *System Status (0x10)* register. To clear this bit and acknowledge the reset event (in order to detect any future resets), the *Ack Reset* bit must be set in the *System Control (0x30)* register.

7.2 I²C Module Specification

The device supports a standard two-wire I²C interface with the addition of a ready (RDY) line. Byte-level clock stretching is allowed. The communications interface of the IQS370 supports the following:

- Fast-mode-plus standard I²C up to 1 MHz.
- Streaming data as well as event mode.

The IQS370 implements 8-bit addressing with 2 bytes at each address.

7.3 I²C Address

The default 7-bit I²C address is 0x44. The default I²C address may be changed after an IQS370 device is booted via the *I²C Address (0xB1)* register. Refer to Section 7.14 for more detail on configuring different I²C addresses when using multiple IQS370 devices per I²C bus.

The IQS370 will also respond to the address whose first bit (LSb) is the complement of the primary address.

- Example 1: If the configured primary I²C address is 0x31 (0b0110001), the device debug address is 0x30 (0b0110000).
- Example 2: If the configured primary I²C address is 0x50 (0b1010000), the device debug address is 0x51 (0b1010001).

The debug address is for debugging purposes only and should not be used during normal operation.

7.4 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

7.5 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words, meaning that two bytes are stored at each address. For example, address 0x10 will provide two bytes. The next two bytes read will be from address 0x11.

The 16-bit data is sent in little-endian byte order (least significant byte first).

7.6 Communication Windows (RDY)

The communication has an open-drain active-low RDY signal to inform the I²C controller that the IQS370 is ready to communicate. It is optimal for the I²C controller to use this as an interrupt input and initiate I²C reads accordingly.

When an IQS370 device has data for the I²C controller, it will pull the RDY line low. This indicates that the IQS370 device has opened its communications window, and it is expecting the I²C controller to address it. When the communication window is closed, the RDY line is released.

On startup, the RDY line functions as an active-low reset line. When RDY is held low by the I²C controller while the device is booting, the device will be kept under reset and will not respond to I²C requests until the line is released.

7.6.1 Communication Modes

The *I²C Interface Type* bits in the *System Control (0x30)* register may be used to configure the manner in which the IQS370 opens communication windows. There are two modes available:

- **Streaming**
  - Communication windows are opened at regular intervals, depending on the configured report rate.
  - When in normal power, windows are opened approximately every *Normal Power Report Rate (0x31)* milliseconds after the latest normal power measurement has taken place.
  - When in low-power, windows are opened approximately every *Low-power Report Rate (ms) (0x32)* milliseconds after the latest low-power measurement has taken place.
- **Event**
  - Communication windows are only opened when triggered by an event.
  - When the *Movement* event bit is set in the *System Status (0x10)* register, a communication window is always opened.

7.6.2 Timeout

If the communication window is not serviced within the *Transaction Timeout (0x34)* period (in milliseconds), the session is ended (RDY goes high), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the I²C controller is not responsive. However, the corresponding data will be missed/lost. The default I²C timeout period is set to 200 ms and can be set to a maximum of 250 ms. The *I²C Communication Timeout* is measured from the start of the communications window (RDY goes low).

7.6.3 Invalid Communications

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY is high).

7.7 I²C Read

A single I²C read is initiated by first writing the register address and then proceeding to read bytes after issuing an I²C RESTART on a read request. The IQS370 device will ACK (acknowledge) the

register address byte that is written.

The I²C controller responds with an ACK on each read byte and ends the read sequence by issuing a NACK (not-acknowledge). Once the STOP bit is issued by the I²C controller, the communication window is closed by the IQS370 device. Register addresses are automatically incremented while the I²C controller clocks out the data. Refer to Figure 7.1 for an illustration of this procedure.

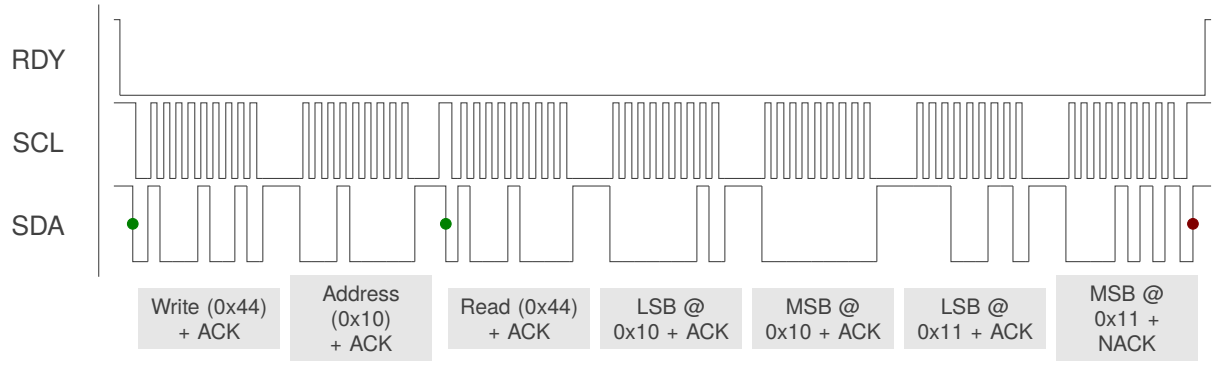


Figure 7.1: I²C Read Example: 4 Bytes Starting at Address 0x10

7.8 I²C Multiple Read

Multiple I²C reads from multiple register addresses may be performed. The procedure from Section 7.7 must be followed, but instead of ending the first register read with a STOP bit, a RESTART is issued by the I²C controller, and the process repeats until a STOP bit is issued on the last register reading transaction. An example is shown in Figure 7.2.

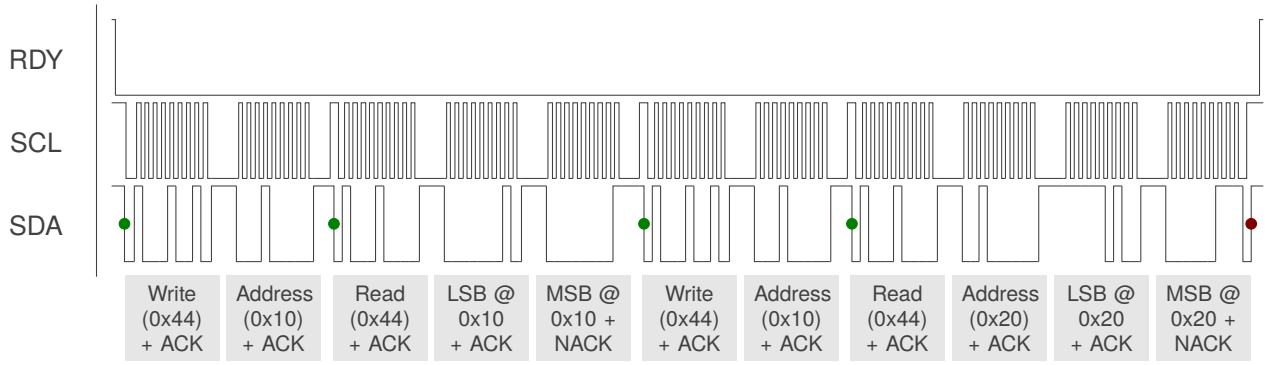


Figure 7.2: I²C Multiple Read Example: 2 Bytes at Address 0x10; 2 Bytes at Address 0x20

7.9 I²C Write

Writing to a single register is achieved by first writing the register address, immediately followed by the data bytes to be written to that address. The IQS370 device will ACK every byte. Similar to the read in Section 7.7, ending the transaction with a STOP bit will close the communication window. This is illustrated in Figure 7.3.

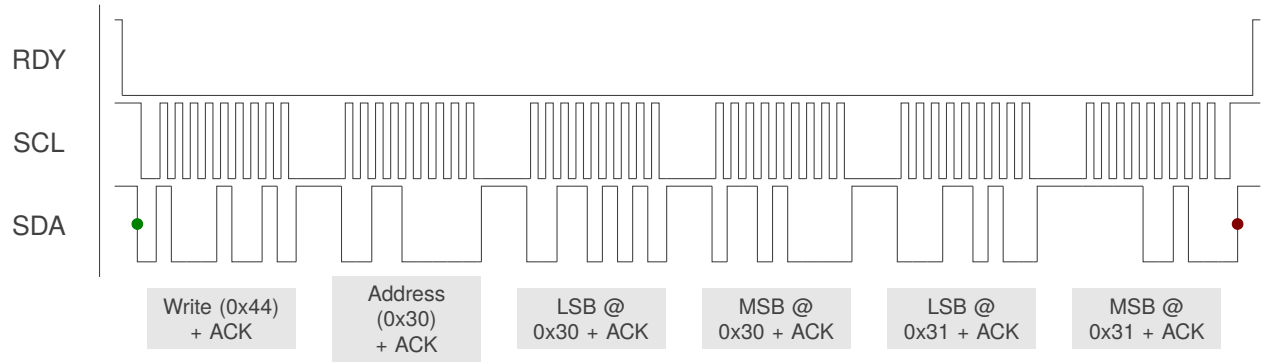


Figure 7.3: I²C Write Example: 4 Bytes Starting at Address 0x30

7.10 I²C Multiple Write

Multiple register addresses may be written in the same communication window. This is done by following the procedure in Section 7.9 but sending a RESTART write request followed by a new register address and data. The communication window is closed by issuing a STOP bit on the last writing transaction. Figure 7.4 illustrates an example.

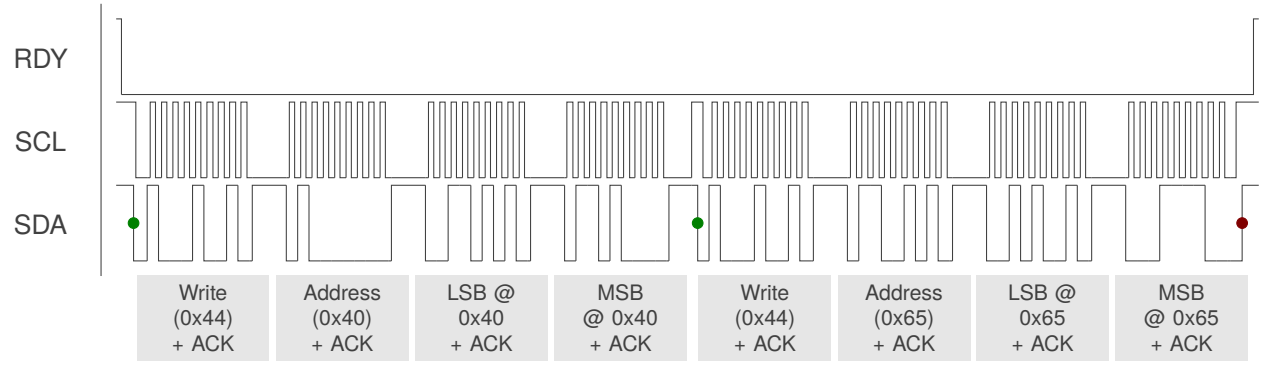


Figure 7.4: I²C Multiple Write Example: 2 Bytes Starting at Address 0x40; 2 Bytes Starting at Address 0x65

7.11 I²C Read and Write Sequence

Reading and writing sequences may be chained in the same communication window prior to a STOP bit being issued to close the communication window. The procedures in Sections 7.8 and 7.10 must be followed. An example of such a mixed transaction is shown in Figure 7.5.

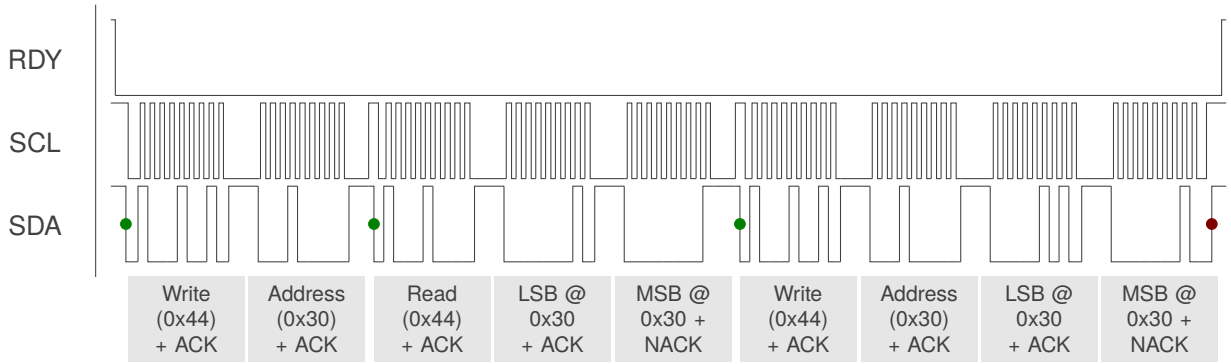


Figure 7.5: I²C Read and Write Example: Read, Modify and Write 2 Bytes Starting at Address 0x30

7.12 Force Closing Communication

A standard I²C STOP will close the current communication window. Contact Azoteq for more information on how to change this behaviour.

A communication window may be closed without sending a STOP by writing 0xFF to the device (as if it were a register address). This is shown in Figure 7.6.

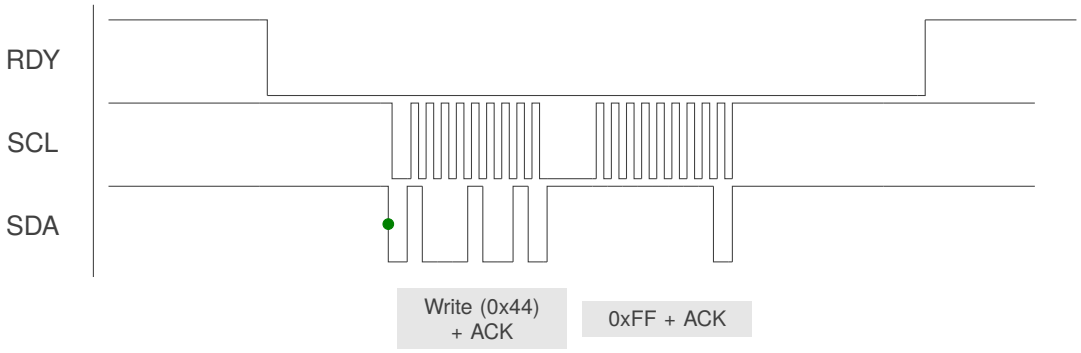


Figure 7.6: Closing the Communication Window While it Is Open. The STOP Bit at the End of "0xFF" is Optional

7.13 Force Starting Communication

In streaming mode, the IQS370 will provide communication windows (RDY pulled low by the IQS370 device) at intervals specified by the power mode sampling period. Refer to Section 7.6.1 for more detail.

Ideally, communication with the IQS370 should only be initiated in a RDY window. However, the I²C controller may wish to force a communication window to open, especially when the IQS370 device's communication is in event mode. When the communication window is closed, i.e., RDY is high, the I²C controller may write 0xFF to the device (as if it were a register address) to request a communication window as soon as possible.

The time before the requested window is opened depends on the current state of the IQS370 device and its configured settings.

This behaviour is illustrated in Figure 7.7.

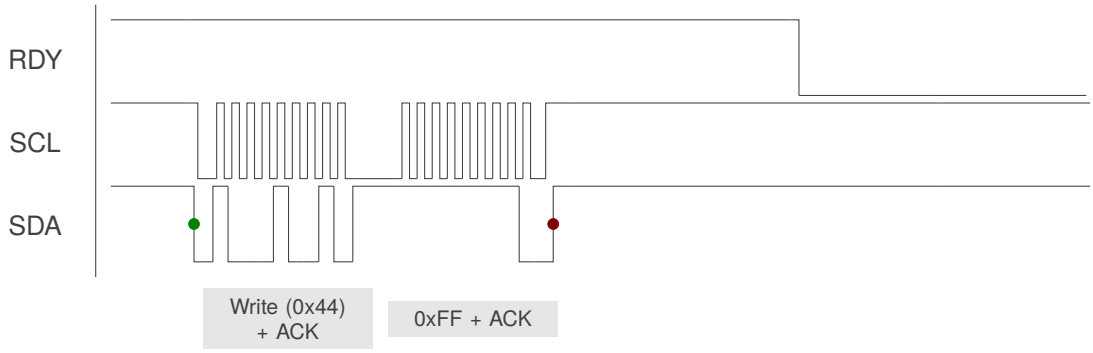


Figure 7.7: Forcing the Communication Window While it is Closed

7.14 Multiple Devices and Custom I²C Addresses

Multiple IQS370 devices may be connected to the same I²C bus if the following procedures are followed. Since RDY briefly acts as a reset line on startup, the master controller may utilise power-line reset circuitry to ensure that the devices can be held in their reset states on boot. During this time, the devices held in reset will not respond to I²C communication.

An example power-line reset circuit is shown in Figure 7.8, where the reset circuitry is implemented with P-channel MOSFETs. An additional MOSFET is used to discharge the capacitors connected to the IQS370 power lines. Without this discharging circuit, a significant waiting time may be required before all connected devices are guaranteed to be reset as a result of the power line disconnecting.

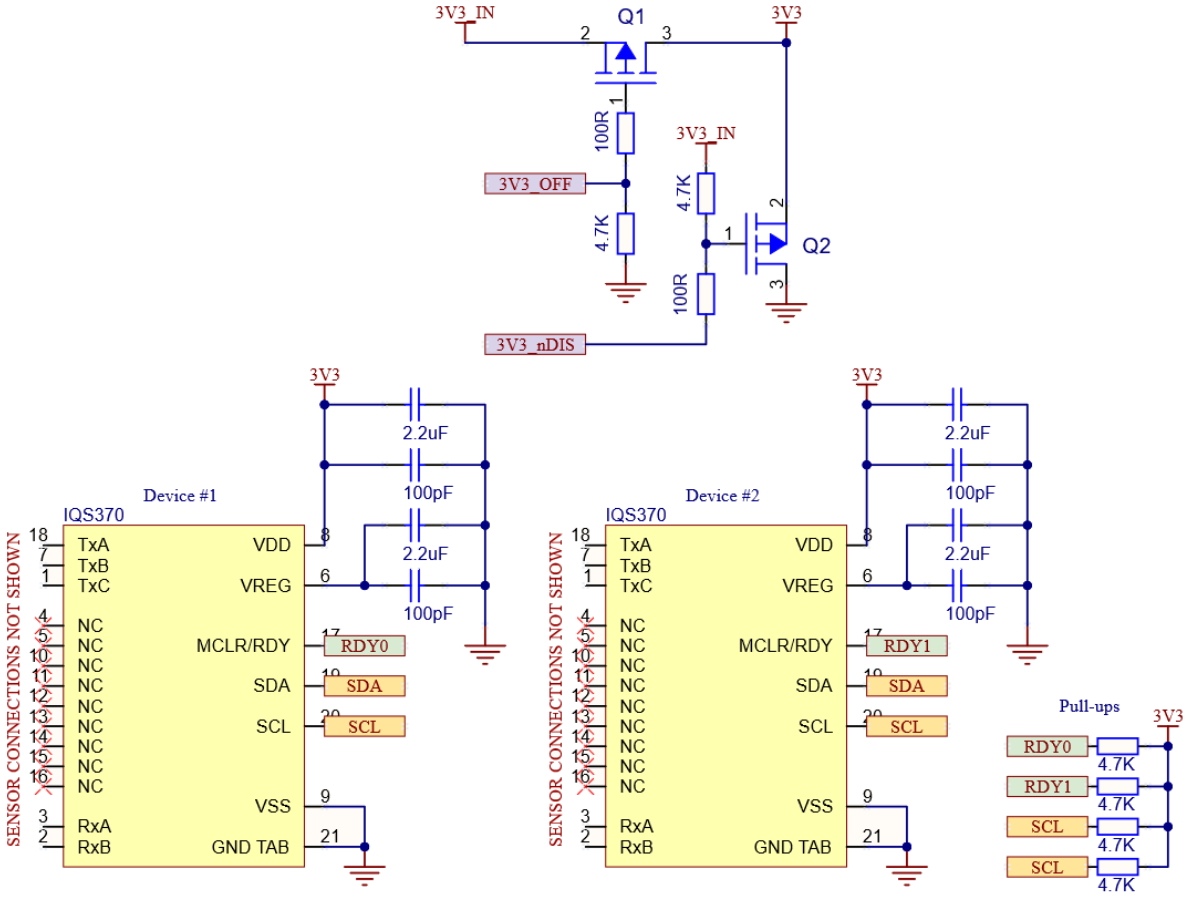


Figure 7.8: Example Schematic for Connecting Multiple IQS370 Devices to Same I²C Bus

An example control signal for assigning custom I²C addresses to multiple IQS370 devices connected to the same bus is shown in Figure 7.9. Refer to Section 7.3 for more information on how to change the I²C address of a specific device. It is recommended to only assign even addresses (e.g., 0x20, 0x22, 0x46, etc.) and avoid the use of the default I²C address (0x44).

If any device resets at any stage of operation (see Section 7.1), the entire I²C address assignment procedure should be repeated from the start.

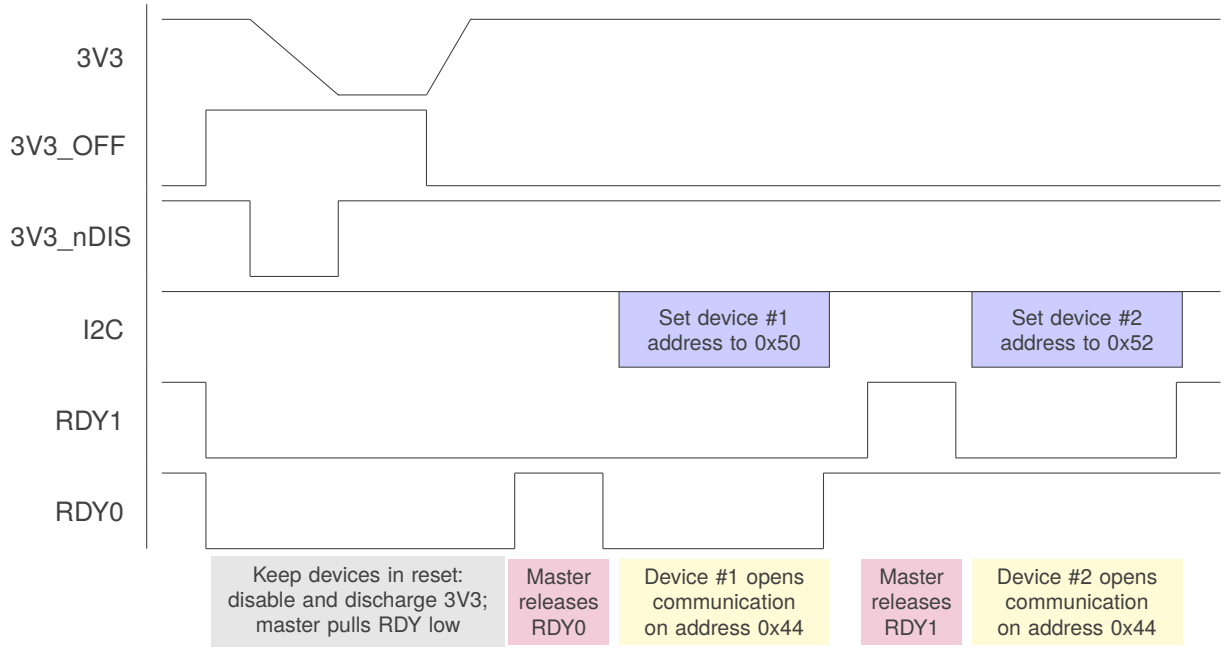


Figure 7.9: An Example of Multiple Device I²C Address Configuration, Based on the Example Schematic in Figure 7.8

8 I²C Memory Map

Table 8.1: I²C Memory Map

Address	Description	Default	Data Type
Read-Only	**Version Information**		
0x00	Product Number	2742	u16
0x01	Major Version	1	u16
0x02	Minor Version	2	u16
0x03 – 0x09	Reserved		u16[7]
Read-Only	**Output Data**		
0x10	Status		Appendix A.1
0x11	Position		u16
0x12	$\text{Angle}_{\text{LUT}}$		u16
0x13	Angle		u16
0x14	$\sin_{\text{norm}}$		i16
0x15	$\cos_{\text{norm}}$		i16
Read-Only	**Intermediate Data**		
0x20	$\sin^{+}$		u16
0x21	$\sin^{-}$		u16
0x22	$\cos^{+}$		u16
0x23	$\cos^{-}$		u16
0x24	$\sin^{+}_{\text{lin}}$		i16
0x25	$\sin^{-}_{\text{lin}}$		i16
0x26	$\cos^{+}_{\text{lin}}$		i16
0x27	$\cos^{-}_{\text{lin}}$		i16
0x28	Low-power Reference		u16
0x29	Low-power Counts		u16
Read-Write	**General Settings**		
0x30	System Control		Appendix A.2
0x31	Normal Power Report Rate (ms)		u16
0x32	Low-power Report Rate (ms)		u16
0x33	Movement Timeout (ms)		u16
0x34	Transaction Timeout (ms)		u16
Read-Write	**Conversion Settings**		
0x40	Excitation Frequency		Appendix A.3
0x41	Max Counts		Appendix A.4
0x42	Reserved		u16
0x43	Pin Selection		Appendix A.5
0x44	Differential Polarity		Appendix A.6
0x45	Stabilisation Times		Appendix A.7
0x46	Low-power Reference Sample Skip		Appendix A.8
0x47	Multipliers and Dividers		Appendix A.9
0x48	Compensation		Appendix A.10
0x49	Base		u16
0x4A	Target		u16

Table 8.1: I²C Memory Map (Continued)

Read-Write	DSP Settings		
0x60	General Processing Settings		Appendix A.11
0x61	Events Mask		Appendix A.12
0x62	Movement Threshold		u16
0x63	Betas		Appendix A.13
0x64	Reserved		u16
0x65	Fast Angle Beta Threshold		u16
0x66	Linearisation Multiplier		u16
0x67	Resolution		u16
Read-Write	**Calibration Data**		
0x70	Sin Max		i16
0x71	Sin Min		i16
0x72	Cos Max		i16
0x73	Cos Min		i16
0x74	Cos Offset 0		i16
0x75	Cos Offset 1		i16
0x76	Angle Max		u16
0x77	Angle Min		u16
Read-Write	**Lookup Table**		
0x80	LUT Size		Appendix A.14
0x81 – 0x91	LUT[0] – LUT[16]		u16[17]
Read-Write	**Custom I²C Address**		
0xB0	Reserved		u16
0xB1	I²C Address	0x44	Appendix A.15

9 Ordering Information

9.1 Ordering Code

Table 9.1: Order Code Description

IQS370 zzz ppb

IC NAME				IQS370
CONFIGURATION	zzz	=	000	I^2C inductive slider / rotary encoder
PACKAGE TYPE	pp	=	QF	QFN-20 Package
BULK PACKAGING	b	=	R	QFN-20 Reel (2000 pcs/reel)

9.2 Top Marking

9.2.1 QFN20 Package Marking Options

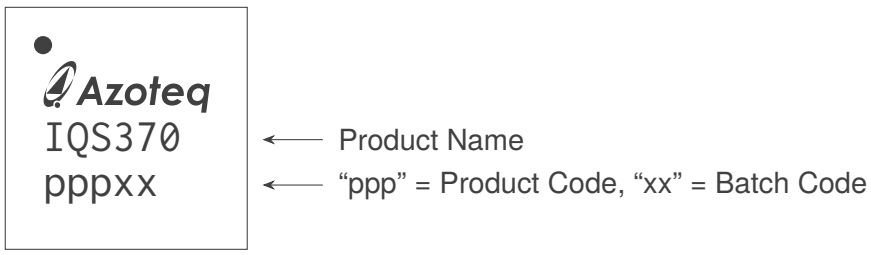


Figure 9.1: IQS370-QFN20 Package Top Marking

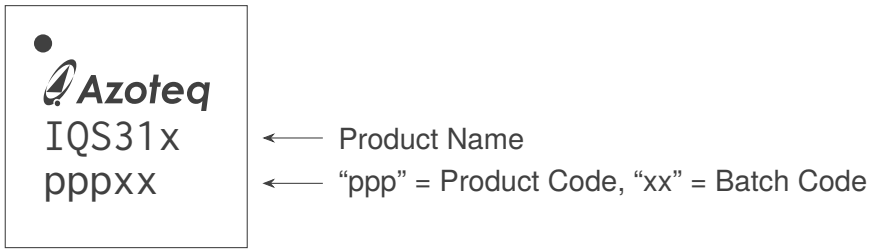


Figure 9.2: IQS31x-QFN20 Package Top Marking

10 Package Specification

10.1 Package Outline Description – QFN20 (QFR)

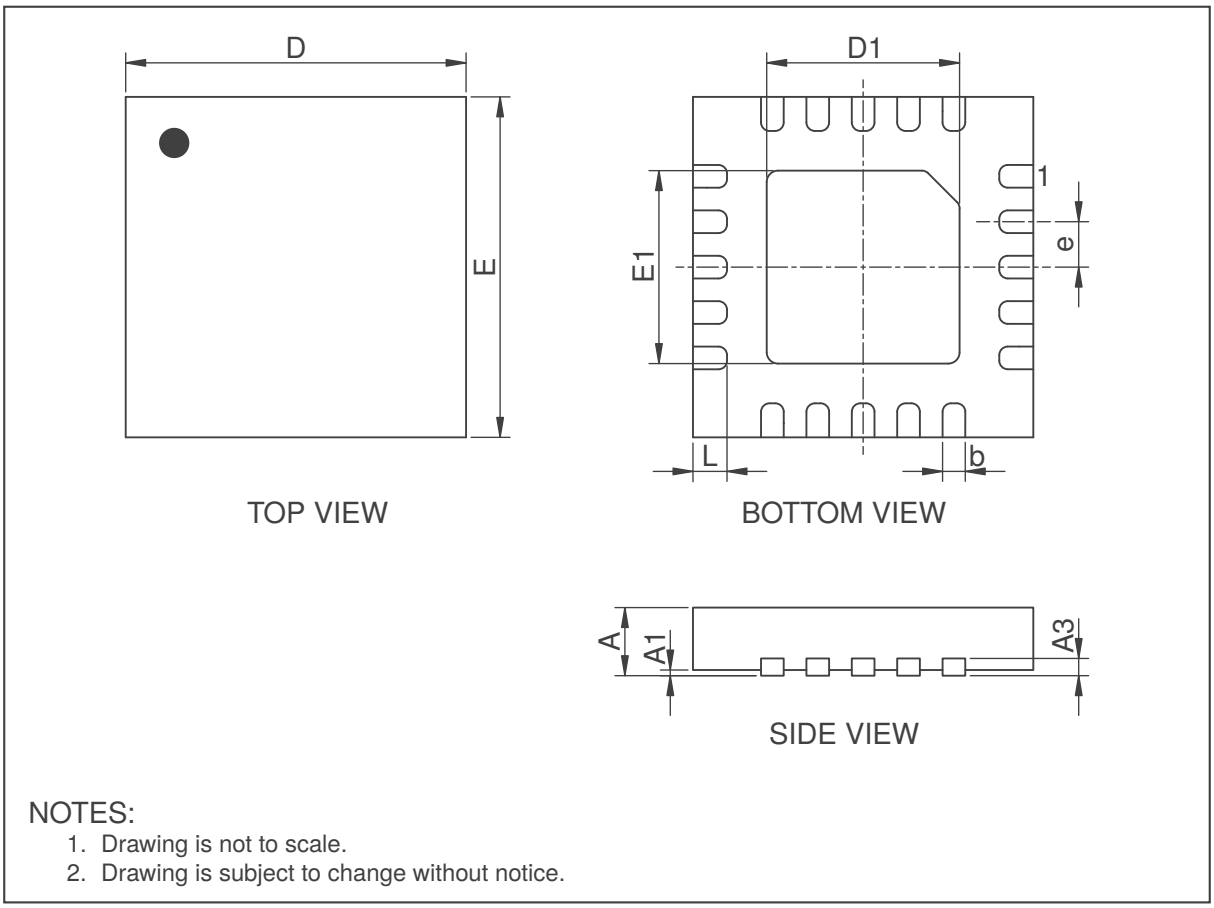
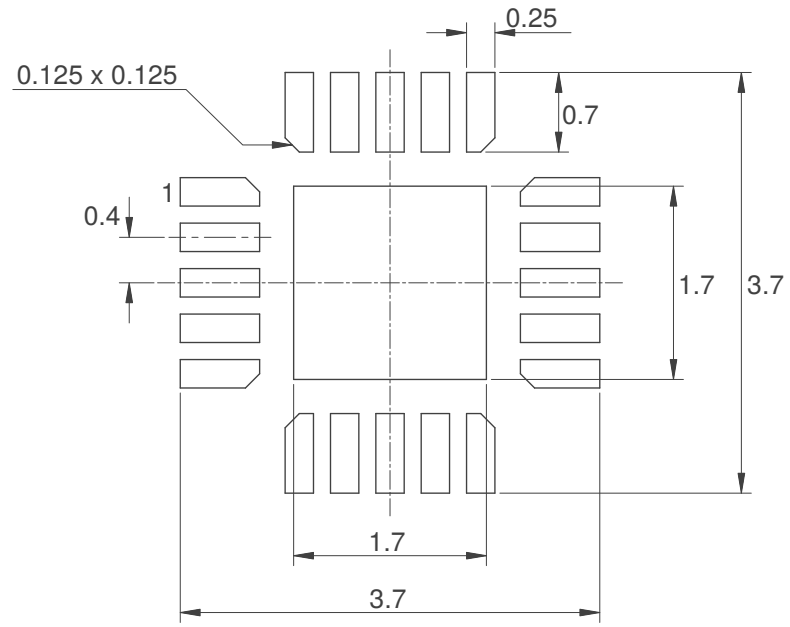


Figure 10.1: QFR (3x3)-20 Package Outline Visual Description

Table 10.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

10.2 Package Footprint Description – QFN20

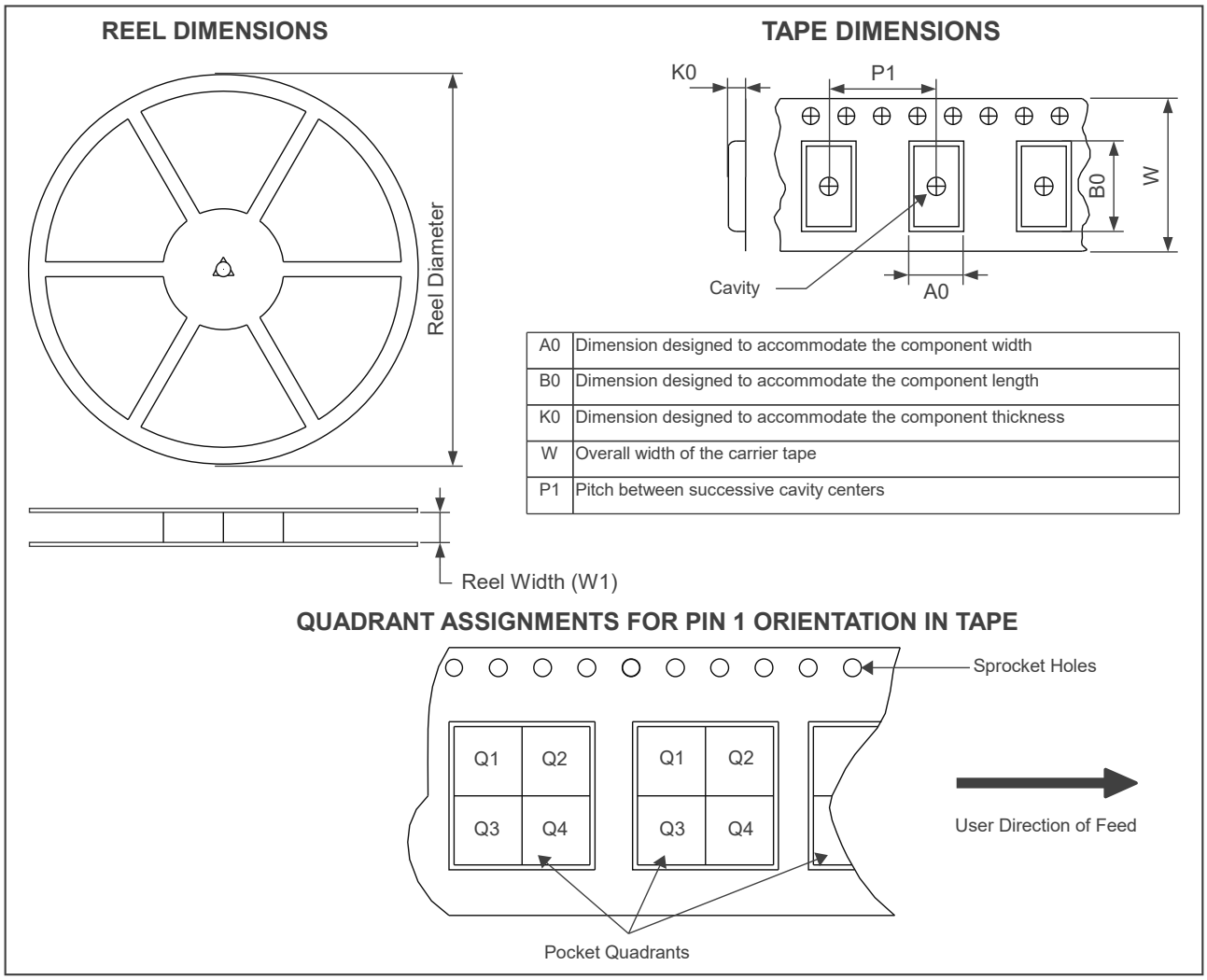


NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 10.2: QFN20 Recommended Footprint

10.3 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 10.3: Tape and Reel Specification

Table 10.2: Tape and reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

A Memory Map Descriptions

A.1 System Status (0x10)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Current Power Mode		Movement	Reserved	Power	Reset

- Bit 4-5: **Current Power Mode**
  - 0: Normal
  - 1: Low
- Bit 3: **Movement**
  - 0: No movement detected
  - 1: Movement detected — threshold defined by *Movement Threshold (0x62)*
- Bit 1: **Power**
  - 0: No automatic power switch occurred
  - 1: Automatic power switch occurred
- Bit 0: **Reset**
  - 0: No reset occured
  - 1: Device reset occured, cleared by Ack Reset (Appendix A.2)

A.2 System Control (0x30)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							Enable Conversions

Bit	7	6	5	4	3	2	1	0
Description	Range Calibration	Differential Counts Calibration	Do ATI	I^2C Interface Type	Power Mode Select		Soft Reset	Ack Reset

- Bit 8: **Enable Conversions**
  - 0: Disabled
  - 1: Enabled
- Bit 7: **Range Calibration**
  - 0: Disabled
  - 1: Enabled
- Bit 6: **Differential Counts Calibration**
  - 0: Disabled
  - 1: Enabled
- Bit 5: **Do ATI**
  - 0: Do Not Perform ATI
  - 1: Perform ATI (cleared on completion)
- Bit 4: **I^2C Interface Type**
  - 0: I^2C Streaming — communicate after every sample
  - 1: I^2C Event — communicate on detected movement only
- Bit 2-3: **Power Mode Select**
  - 0: Normal
  - 1: Low (Forced)
  - 2: Automatic
- Bit 1: **Soft Reset**

- 0: Do not perform a software device reset
- 1: Perform a software device reset

› Bit 0: **Ack Reset**
- 0: Do not acknowledge reset event
- 1: Clear/acknowledge reset event (see Appendix A.1)

A.3 Excitation Frequency (0x40)

Bit	15	14	13	12	11	10	9	8
Description	Excitation Frequency							

Bit	7	6	5	4	3	2	1	0
Description	Reserved							

› Bit 8-15: **Excitation Frequency**
- 1: 3.50 MHz
- 2: 2.33 MHz
- 3: 1.75 MHz
- 4: 1.40 MHz
- 6: 1.00 MHz

A.4 Max Counts (0x41)

Bit	15	14	13	12	11	10	9	8
Description	0x12							

Bit	7	6	5	4	3	2	1	0
Description	Max Counts		0x35					

› Bit 6-7: **Max Counts**
- 0: 1023
- 1: 2047
- 2: 4095
- 3: 16383

A.5 Pin Selection (0x43)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							Rx Pin Select

Bit	7	6	5	4	3	2	1	0
Description	Reserved		TxC		TxB		TxA	

› Bit 8: **Rx Pin Select**
- 0: RxA – Sin / RxB – Cos
- 1: RxA – Cos / RxB – Sin

› Bit 4-5: **TxC**
- 0: Inactive
- 1: Vb
- 2: Tx+
- 3: Tx-

› Bit 2-3: **TxB**
- 0: Inactive

- 1: Vb
- 2: Tx+
- 3: Tx-

› Bit 0-1: **TxA**
- 0: Inactive
- 1: Vb
- 2: Tx+
- 3: Tx-

A.6 Differential Polarity (0x44)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							Cos Polarity

Bit	7	6	5	4	3	2	1	0
Description	Reserved							Sin Polarity

› Bit 8: **Cos Polarity**
- 0: Inverted
- 1: Not inverted

› Bit 0: **Sin Polarity**
- 0: Inverted
- 1: Not inverted

A.7 Stabilisation Time (0x45)

Bit	15	14	13	12	11	10	9	8
Description	Fine							

Bit	7	6	5	4	3	2	1	0
Description	Coarse							

› Bit 8-15: **Fine**
- The number of microseconds divided by 10

› Bit 0-7: **Coarse**
- Stabilisation time in milliseconds (max 200)

A.8 Low-power Reference Sample Skip (0x46)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Low-power Temp Track Sample Skip							

› Bit 0-7: **Low-power Reference Sample Skip**
- 8-bit value

A.9 Multipliers and Dividers (0x47)

Bit	15	14	13	12	11	10	9	8
Description	P-Multiplier		P-Divider					N-Multiplier

Bit	7	6	5	4	3	2	1	0
Description	N-Multiplier			N-Divider				

- Bit 14-15: **Fine Multiplier**
  - 2-bit value
- Bit 9-13: **Fine Divider**
  - 5-bit value
- Bit 5-8: **Coarse Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Divider**
  - 5-bit value

A.10 Compensation (0x48)

Bit	15	14	13	12	11	10	9	8
Description	Divider					Reserved	Select	

Bit	7	6	5	4	3	2	1	0
Description	Select							

- Bit 11-15: **Divider**
  - 5-bit value
- Bit 0-9: **Select**
  - 10-bit value

A.11 General Processing Settings (0x60)

Bit	15	14	13	12	11	10	9	8
Description	Wake Up Threshold							

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Enable Lookup Table	Oversampling		Linearise	Reserved

- Bit 8-15: **Wake Up Threshold**
  - 8-bit value
- Bit 4: **Enable Lookup Table**
  - 0: LUT bypassed
  - 1: LUT enabled
- Bit 2-3: **Oversampling**
  - 0: 1x (None)
  - 1: 2x
  - 2: 4x
  - 3: 8x
- Bit 1: **Linearise**
  - 0: Raw counts used directly
  - 1: $1/x$ linearisation applied to raw counts

A.12 Events Mask (0x61)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Power	Reserved

- Bit 1: **Power**
  - 0: Power events do not open communication windows in I²C event mode
  - 1: Power events open communication windows in I²C event mode

A.13 Betas (0x63)

Bit	15	14	13	12	11	10	9	8
Description	Fast Beta							

Bit	7	6	5	4	3	2	1	0
Description	Slow Beta							

- Bit 8-15: **Fast Beta**
  - 8-bit value
- Bit 0-7: **Slow Beta**
  - 8-bit value

A.14 LUT Size (0x80)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	LUT Size							

- Bit 0-7: **LUT Size**
  - 0: 2 Points
  - 1: 3 Points
  - 2: 5 Points
  - 3: 9 Points
  - 4: 17 Points

A.15 I²C Address (0xB1)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved	I²C Address						

- Bit 0-6: 7-bit I²C address

Contact Information

	South Africa (Headquarters)	China
Physical Address	1 Bergsig Avenue Paarl 7646 South Africa	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC
Tel	+27 21 863 0033	+86 755 8303 5294 ext 808
Email	info@azoteq.com	info@azoteq.com

	USA	Taiwan
Physical Address	7000 North Mopac Expressway Suite 200 Austin TX 78731 USA	Xintai 5th Road, Sec. 1 No. 99, 9F-12C Xizhi District 221001 New Taipei City Taiwan
Tel	+1 512 538 1995	+886 932 219 444
Email	info@azoteq.com	info@azoteq.com

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