IQS9342 Datasheet

Multi-Channel Inductive Sensing Device Aimed at Analog Keyboard Applications with Multi-Level Detection of Numerous Keys

1 Device Overview

The IQS9342 ProxSense® IC is a multi-channel inductive sensing device that supports up to 42 channels per device and up to 16 kHz sampling rate. The IC also supports on-chip environmental compensation.

1.1 Main Features

- Up to 42 channels with single-pin measurement
- Up to 21 channels with dual-pin measurement
- Up to 16 kHz sampling rate
- Environmental tracking
- Configurable power states
- Fully configurable via SPI interface
- 16-bit raw data per channel
- SPI communication interface up to 20 MHz
- Designed for multiplexed device array
- QFN64 (8×8×0.75 mm) – 0.4 mm pitch
- Wide input voltage supply range: 2.4 V to 3.6 V
- Wide operating temperature range: –20 °C to +85 °C

Figure 1.1: IQS9342 QFN64 Package

1.2 Applications

- Analog keyboards for gaming/productivity
- Contactless button applications for industrial/white goods
- Musical equipments
- Forcepads

Contents

2 QFN64 Pinout

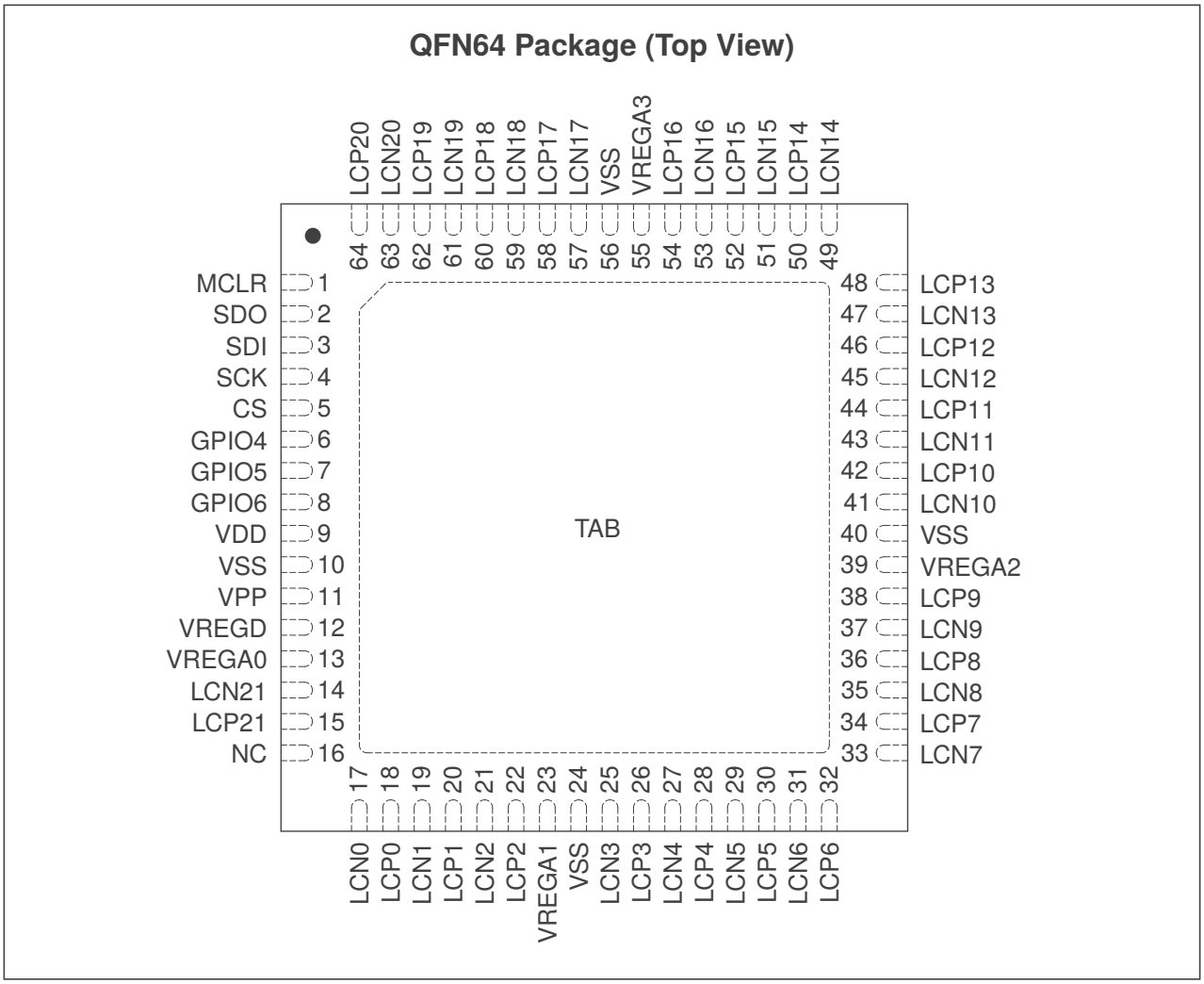

Figure 2.1: QFN64 Pinout

Table 2.1: QFN64 Pin Descriptions

Pin	Name	Type[i]	Function	Description
1	MCLR	I	nReset	Device reset request
2	SDO	O	SPI	SPI serial data out
3	SDI	I	SPI	SPI serial data in
4	SCK	I	SPI	SPI port clock
5	CS	I	SPI	SPI enable / chip-select
6	GPIO4	I/O	GPIO	General purpose pin or external reference clock input
7	GPIO5	I/O	GPIO	General purpose pin
8	GPIO6	I/O	GPIO	General purpose pin
9	VDD	P	Power	Power supply input voltage
10	VSS	P	Power	Analog/digital ground
11	VPP	P	Power	Fuse programming voltage

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Table 2.1: QFN64 Pin Descriptions (Continued)

Pin	Name	Type[i]	Function	Description
12	VREGD	P	Power	Internally-regulated digital supply voltage
13	VREGA0	P	Power	Internally-regulated analog supply voltage
14	LCN21	I/O	Analog	LC oscillator 21 negative terminal
15	LCP21	I/O	Analog	LC oscillator 21 positive terminal
16	NC	-	-	Not Connected
17	LCN0	I/O	Analog	LC oscillator 0 negative terminal
18	LCP0	I/O	Analog	LC oscillator 0 positive terminal
19	LCN1	I/O	Analog	LC oscillator 1 negative terminal
20	LCP1	I/O	Analog	LC oscillator 1 positive terminal
21	LCN2	I/O	Analog	LC oscillator 2 negative terminal
22	LCP2	I/O	Analog	LC oscillator 2 positive terminal
23	VREGA1	P	Power	Internally-regulated analog supply voltage
24	VSS	P	Power	Analog/digital ground
25	LCN3	I/O	Analog	LC oscillator 3 negative terminal
26	LCP3	I/O	Analog	LC oscillator 3 positive terminal
27	LCN4	I/O	Analog	LC oscillator 4 negative terminal
28	LCP4	I/O	Analog	LC oscillator 4 positive terminal
29	LCN5	I/O	Analog	LC oscillator 5 negative terminal
30	LCP5	I/O	Analog	LC oscillator 5 positive terminal
31	LCN6	I/O	Analog	LC oscillator 6 negative terminal
32	LCP6	I/O	Analog	LC oscillator 6 positive terminal
33	LCN7	I/O	Analog	LC oscillator 7 negative terminal
34	LCP7	I/O	Analog	LC oscillator 7 positive terminal
35	LCN8	I/O	Analog	LC oscillator 8 negative terminal
36	LCP8	I/O	Analog	LC oscillator 8 positive terminal
37	LCN9	I/O	Analog	LC oscillator 9 negative terminal
38	LCP9	I/O	Analog	LC oscillator 9 positive terminal
39	VREGA2	P	Power	Internally-regulated analog supply voltage
40	VSS	P	Power	Analog/digital ground
41	LCN10	I/O	Analog	LC oscillator 10 negative terminal
42	LCP10	I/O	Analog	LC oscillator 10 positive terminal
43	LCN11	I/O	Analog	LC oscillator 11 negative terminal
44	LCP11	I/O	Analog	LC oscillator 11 positive terminal
45	LCN12	I/O	Analog	LC oscillator 12 negative terminal
46	LCP12	I/O	Analog	LC oscillator 12 positive terminal
47	LCN13	I/O	Analog	LC oscillator 13 negative terminal
48	LCP13	I/O	Analog	LC oscillator 13 positive terminal
49	LCN14	I/O	Analog	LC oscillator 14 negative terminal
50	LCP14	I/O	Analog	LC oscillator 14 positive terminal
51	LCN15	I/O	Analog	LC oscillator 15 negative terminal
52	LCP15	I/O	Analog	LC oscillator 15 positive terminal
53	LCN16	I/O	Analog	LC oscillator 16 negative terminal

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Table 2.1: QFN64 Pin Descriptions (Continued)

Pin	Name	Type[i]	Function	Description
54	LCP16	I/O	Analog	LC oscillator 16 positive terminal
55	VREGA3	P	Power	Internally-regulated analog supply voltage
56	VSS	P	Power	Analog/digital ground
57	LCN17	I/O	Analog	LC oscillator 17 negative terminal
58	LCP17	I/O	Analog	LC oscillator 17 positive terminal
59	LCN18	I/O	Analog	LC oscillator 18 negative terminal
60	LCP18	I/O	Analog	LC oscillator 18 positive terminal
61	LCN19	I/O	Analog	LC oscillator 19 negative terminal
62	LCP19	I/O	Analog	LC oscillator 19 positive terminal
63	LCN20	I/O	Analog	LC oscillator 20 negative terminal
64	LCP20	I/O	Analog	LC oscillator 20 positive terminal
	TAB	-	-	Thermal pad (floating). It is recommended to connect this to VSS.

[i] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

3 Reference Schematic

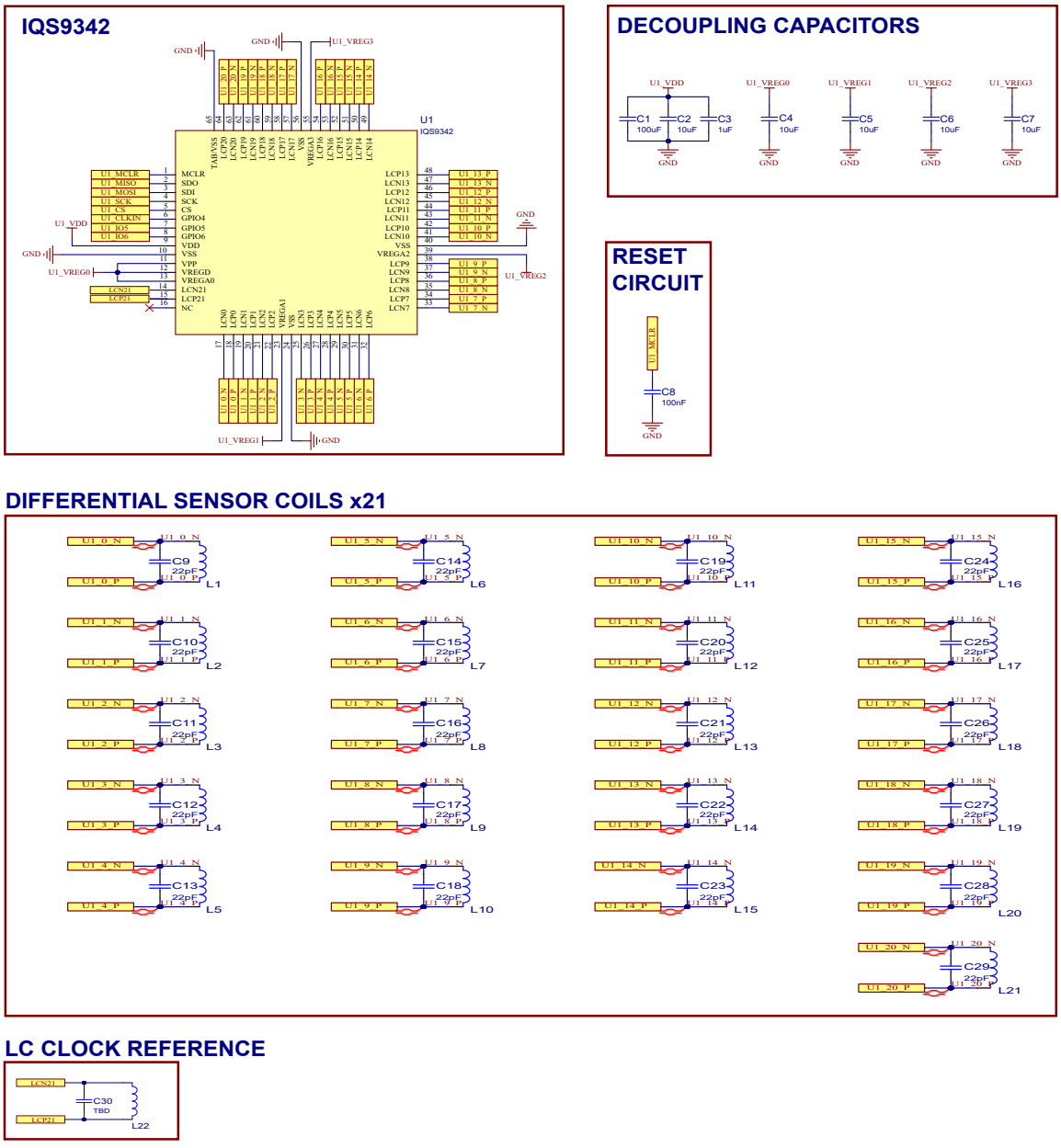


Figure 3.1: Dual-pin Measurement - IQS9342 Single Device Reference Schematic

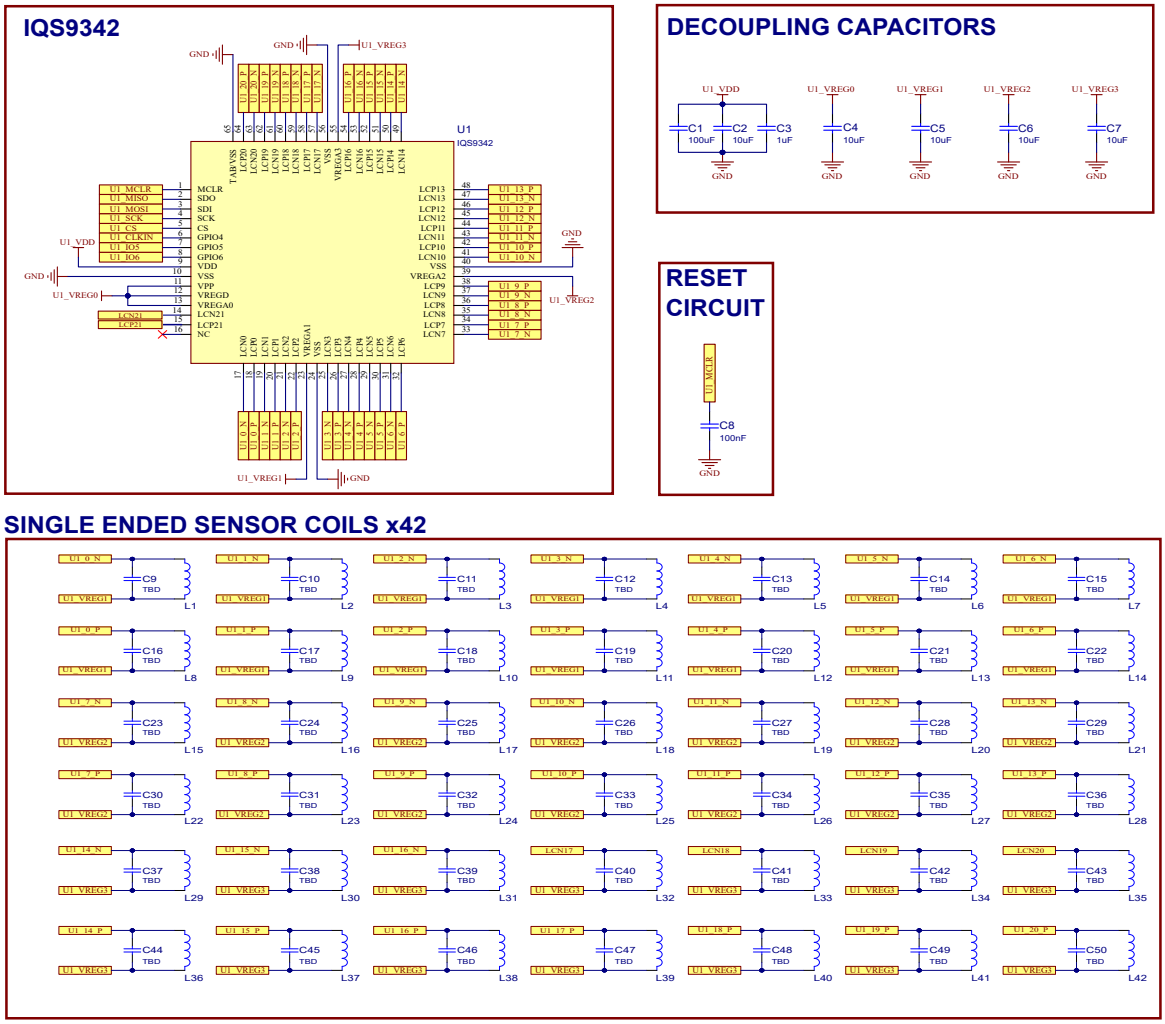


Figure 3.2: Single-pin Measurement - IQS9342 Single Device Reference Schematic

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4.1: Absolute Maximum Ratings

Symbol	Rating	Min	Max	Unit
V_{DD}	Voltage applied at VDD pin (referenced to VSS)	−0.3	3.6	V
V_{IN}	Voltage applied to any analog, VREG, or VPP pin (referenced to VSS)	−0.3	V_{REG}	V
	Voltage applied to any other pin (referenced to VSS)	−0.3	V_{DD} + 0.3 (3.6 V max)	V
T_{stg}	Storage temperature	−40	85	°C

4.2 General Operating Conditions

Table 4.2: General Operating Conditions

Symbol	Parameter	Typ	Unit
f_{RCO}	RC oscillator frequency	18	MHz
V_{REG}	Internally-regulated supply output	1.8	V

4.3 ESD Rating

Table 4.3: ESD Rating

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge voltage	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[i]	±2000	V

[i] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

4.4 Reset Levels

Table 4.4: Reset Levels

Parameter		Min	Max	Unit
V_{DD}	Power-up (Reset trigger) – slope > 500 V/s		1.9	V
	Power-down (Reset trigger) – slope < −500 V/s	0.8		

4.5 MCLR Pin Levels and Characteristics

Table 4.5: MCLR Pin Characteristics

Parameter		Min	Typ	Max	Unit
V_{IL}	MCLR input low level voltage	V_{SS} – 0.3		0.2 × V_{DD}	V
V_{IH}	MCLR input high level voltage	0.8 × V_{DD}		V_{DD} + 0.3	V
R_{PU}	MCLR pull-up equivalent resistor		150		kΩ
t_{Trig}	MCLR input pulse width – ensure trigger	250			ns

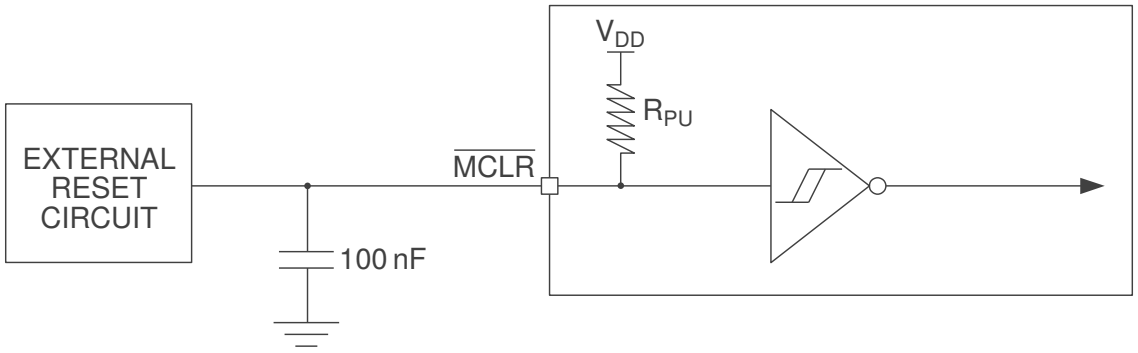


Figure 4.1: MCLR Pin Diagram

4.6 Recommended Operating Conditions

Table 4.6: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage, applied at VDD pin	2.4		3.6	V
T_A	Operating free-air temperature	–20		85	°C
C_{VDD}	Recommended capacitor at VDD		3 × C_{VREGA}		µF
$C_{VREGA[0..3]}$	Recommended external buffer capacitor at VREG (ESR ≤ 200 mΩ)		10		µF

4.7 Digital I/O Characteristics

Table 4.7: Digital I/O Characteristics

Parameter		Test Conditions[i]	Min	Max	Unit
V_{OL}	Output low voltage of GPIO pins	I_{OL} = 10 mA		0.1 × V_{DD}	V
V_{OH}	Output high voltage	I_{OH} = –5 mA	0.9 × V_{DD}		V
V_{IL}	Input low voltage		V_{SS} – 0.3	0.3 × V_{DD}	V
V_{IH}	Input high voltage		0.7 × V_{DD}	V_{DD} + 0.3	V

[i] Standard operating conditions:
V_{DD}: 2.5 V to 3.6 V, unless otherwise stated.
Operating temperature: –20 °C to 85 °C.

4.8 SPI Characteristics

Table 4.8: I²C Characteristics

Parameter[i]		Min	Max	Unit
$f_{c(SCK)}$ $1 / t_{c(SCK)}$	SPI clock frequency[ii]		1.33 × f_{sysclk}	MHz
$t_{su(CS)}$	CS setup time	70		ns
$t_{h(CS)}$	CS hold time	70		ns
$t_{idle(CS)}$	CS idle time	3.1 × t_{sysclk}		ns
$t_{su(SI)}$	SDI input setup time	6		ns
$t_{h(SI)}$	SDI input hold time	2		ns
$t_{v(SO)}$	SDO valid output time (slow mode)		85	ns
	SDO valid output time (fast mode)		20	
$t_{h(SO)}$	SDO output hold time	0		ns
$t_{dis(SO)}$	SDO output disable time	1		ns

[i] Unless otherwise stated, the following characteristics are derived from design specifications and not tested in production. These are applicable under the following conditions:
- V_{DD}: 3.3 V
- Capacitive load: 20 pF
- Operating temperature: −20 °C to 85 °C

[ii] $t_{c(SCK)}$ is additionally limited to a maximum of 2 × ($t_{v(SO)}$ + $t_{su(MI)}$), where $t_{su(MI)}$ is the controller's data input setup time.

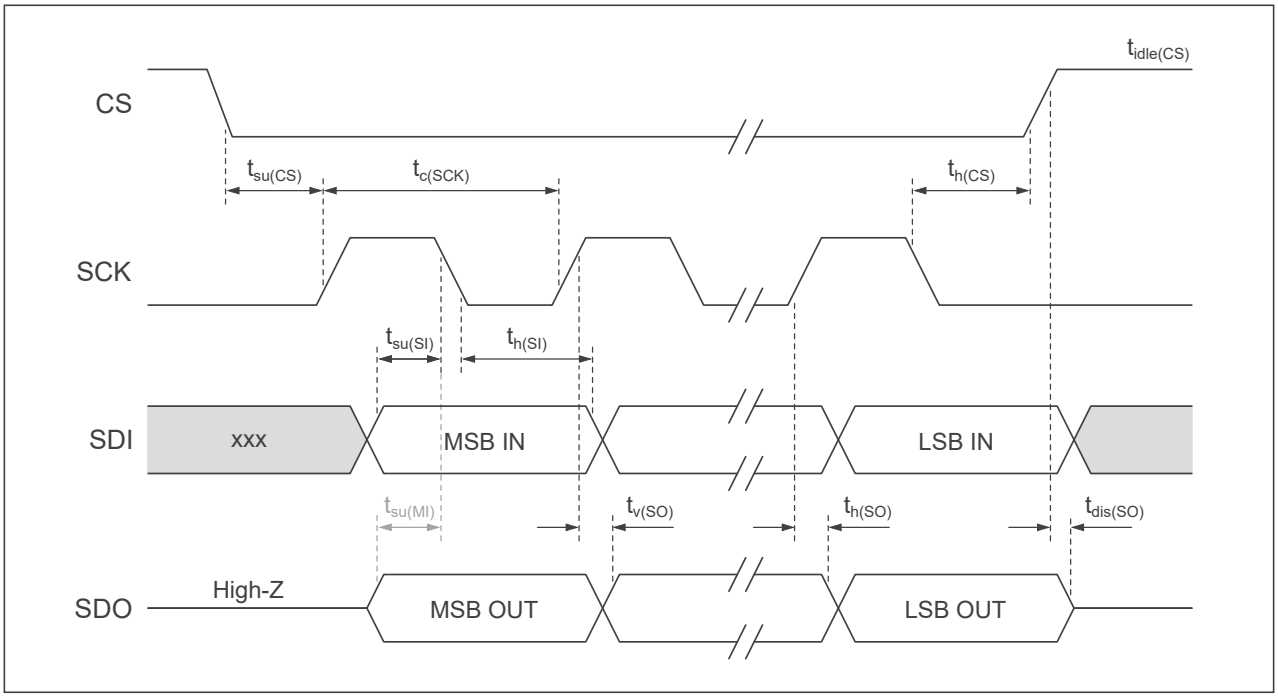


Figure 4.2: SPI Timing Diagram – CPOL = 0, CPHA = 1

5 Ordering Information

5.1 Ordering Code

IQS9342 – zzz ppb

Table 5.1: Order Code Description

IC NAME				IQS9342
CONFIGURATION	zzz	=	000	Default Configuration SPI
PACKAGE TYPE	pp	=	QF	QFN-64 Package
BULK PACKAGING	b	=	R	QFN-64 Reel (3000 pcs/reel)

Example : IQS9342-000QFR

5.2 QFN64 Top Markings

Figure 5.1: IQS9342-QFN64 Package Top Marking

6 QFN64 Package Information

6.1 QFN64 Package Outline

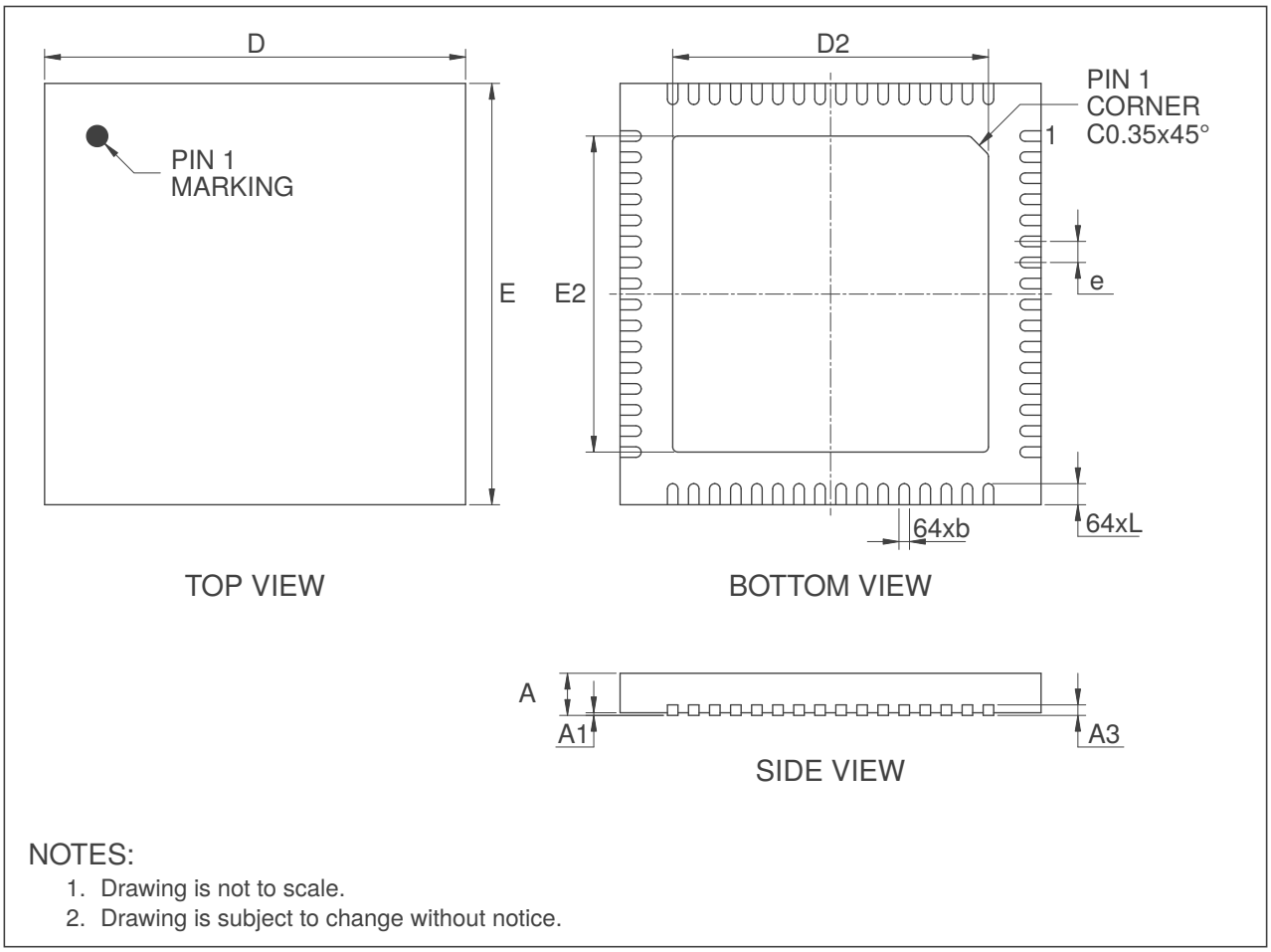
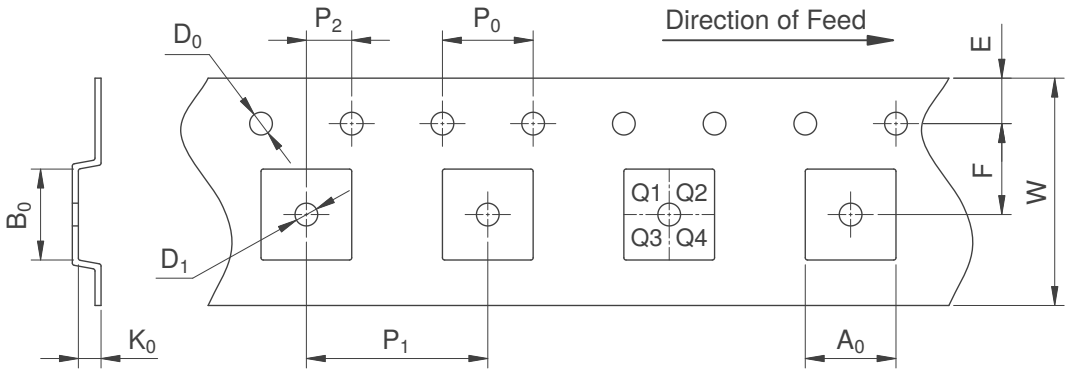


Figure 6.1: QFN64 Package Outline

Table 6.1: QFN64 Package Dimensions [mm]

Dimension	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D		8.00 BSC	
E		8.00 BSC	
D1	5.90	6.00	6.10
E1	5.90	6.00	6.10
e		0.40 BSC	
L	0.30	0.40	0.50

6.2 Tape and Reel Specifications

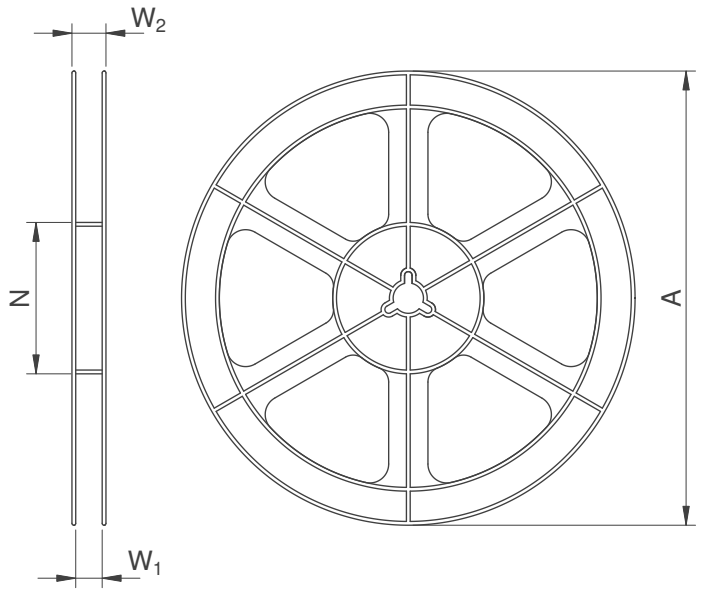


NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 6.2: Carrier Tape Specification

Table 6.2: Carrier Tape Dimensions [mm]

Dimension	Package
	QFN64
A_0	8.30
B_0	8.30
K_0	1.10
D_0	1.50
D_1	1.50
E	1.75
F	7.50
P_0	4.00
P_1	12.00
P_2	2.00
W	16.00
Pin 1 Quadrant	Q2



NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 6.3: Reel Specification

Table 6.3: Reel Dimensions [mm]

Dimension	Package
	QFN64
A	330
N	100
W_1	16.4
W_2 (Max)	22.4

7 Memory Map

7.1 Memory Map

Table 7.1: SPI Memory Map

Address	Length	Description	Default	Notes
Read-Write		**Port 1 Digital Input/Output**		
0x0022	2	SPI Pin Configuration	0	Section 7.2.1
0x0024	2	PIO4 Pin Configuration	0x0004	Section 7.2.2
0x0026	2	PIO5 Pin Configuration	0	Section 7.2.3
0x0028	2	PIO6 Pin Configuration	0	Section 7.2.4
Read-Write		**Fuse Control**		
0x0040	2	Programming Control	0	Section 7.2.5
0x0042	2	Address	0	u16
0x0044	2	Read Data Out	–	u16
Read-Write		**Sequencer**		
0x0050	2	Control and Status	0	Section 7.2.6
0x0054	2	Instruction and Report Address Offsets	0	Section 7.2.7
Read-Write		**System Identification**		
0x0080	2	Device ID	0x0305	u16
0x0082	2	Device Hardware Version	0xF000	u16
Read-Write		**Hardware Configuration**		
0x0090	2	IREF Trim	0	u16
0x0092	2	VREG Trim	0	u16
0x0094	2	RC Oscillator Trim	0	u16
0x0096	2	PLL Loop Filter	0x0003	Section 7.2.8
0x0098	2	PLL Configuration	0x00B1	Section 7.2.9
0x009A	2	Device Configuration	0x0012	Section 7.2.10
0x009C	2	Power Control	0x0001	Section 7.2.11
Read-Write		**Device Status**		
0x00F0	4	Hardware Status	0x0088	Section 7.2.12
0x00F4	2	Regulator Status	–	Section 7.2.13
Read-Write		**Sensor**		
0x0200	44	Configuration 0	0	Section 7.2.14 [22]
0x0240	44	Configuration 1	0	Section 7.2.15 [22]
0x02B0	2	Global Configuration 0	0	Section 7.2.16
0x02B4	4	Oscillator Enable	0	u32
0x02B8	4	Start Measurement	0	u32
0x02BC	4	Continuous Measurement Enable	0	u32
0x02C0	44	Output	0	u16 [22]
0x02F0	2	Control and Status	0	Section 7.2.17
0x02F2	2	Timer Period	0	u16
0x02F4	4	Error Flags	0	u32
0x02F8	4	Amplitude Flags	0	u32

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Table 7.1: SPI Memory Map (Continued)

0x02FC	4	Overflow Flags	0	u32
Read-Write		**Sequencer Memory**		
0x0800	512	Report Memory	0	u16 [256]
0x0A00	512	Instruction Memory	0	u16 [256]

7.2 Register Bit Descriptions

7.2.1 SPI Pin Configuration (0x0022)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Disable CS Filter	Disable IO Filter

- Bit 0: **Disable IO Filter**
  - 0: Spike filter enabled for SCK and SDI
  - 1: Spike filter disabled
- Bit 1: **Disable CS Filter**
  - 0: Spike filter enabled for CS
  - 1: Spike filter disabled

7.2.2 PIO4 Pin Configuration (0x0024)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Disable Spike Filter	Enable Analog Output to Pin	Enable Input Path	Drive State Select	

- Bit 0-1: **Drive State Select**
  - 0: High-impedance input
  - 1: PLL reference clock
  - 2: Drive low
  - 3: Drive high
- Bit 2: **Enable Input Path**
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Enable Analog Output to Pin**
  - 0: Disabled
  - 1: Enabled
- Bit 4: **Disable Spike Filter**
  - 0: Filter enabled
  - 1: Filter disabled

7.2.3 PIO5 Pin Configuration (0x0026)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Disable Spike Filter	Enable Analog Output to Pin	Enable Open-Drain Operation	Drive State Select			

- Bit 0-3: **Drive State Select**
  - 0: High-impedance input
  - 1: PLL reference clock
  - 2: Drive low
  - 3: Drive high
  - 4: PLL lock indicator
  - 5: Indicator for measurement timeout, channel error or not busy
  - 6: Indicate sequencer wait-event state
  - 7: Indicate sequencer halt state
  - 8: LC oscillator ready and sequencer wait-event state
  - 9: LC oscillator not busy indicator
  - 10: PLL feedback clock
  - 11: System clock
  - 12: LC oscillator clock
  - 13: LC oscillator amplitude high indicator
- Bit 4: **Enable Open-Drain Operation**
  - 0: Disabled
  - 1: Enabled
- Bit 5: **Enable Analog Output to Pin**
  - 0: Disabled
  - 1: Enabled
- Bit 6: **Disable Spike Filter**
  - 0: Filter enabled
  - 1: Filter disabled

7.2.4 PIO6 Pin Configuration (0x0028)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Disable Spike Filter	Enable Analog Output to Pin	Enable Open-Drain Operation	Drive State Select			

- Bit 0-3: **Drive State Select**
  - 0: High-impedance input
  - 1: PLL reference clock
  - 2: Drive low
  - 3: Drive high
  - 4: PLL lock indicator
  - 5: Indicator for measurement timeout, channel error or not busy
  - 6: Indicate sequencer wait-event state
  - 7: Indicate sequencer halt state
  - 8: LC oscillator ready and sequencer wait-event state
  - 9: LC oscillator not busy indicator
  - 10: PLL feedback clock
  - 11: System clock
  - 12: LC oscillator clock
  - 13: LC oscillator amplitude high indicator
- Bit 4: **Enable Open-Drain Operation**
  - 0: Disabled
  - 1: Enabled
- Bit 5: **Enable Analog Output to Pin**
  - 0: Disabled
  - 1: Enabled
- Bit 6: **Disable Spike Filter**
  - 0: Filter enabled
  - 1: Filter disabled

7.2.5 Programming Control (0x0040)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved					Enable Fuse Reset Control	Enable Programming Pin	Enable Fuse Module

- Bit 0: **Enable Fuse Module**
  - 0: Disabled
  - 1: Enabled
- Bit 1: **Enable Programming Pin**
  - 0: Disabled
  - 1: Enabled
- Bit 2: **Enable Fuse Reset Control**
  - 0: Disabled
  - 1: Enabled
  - Hold reset control to fuse until low

7.2.6 Sequencer Control and Status (0x0050)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved				Single Step Go	Single Step	State Select	Run Sequencer

- Bit 0: **Run Sequencer**
  - 0: Disabled
  - 1: Enabled
  - Set bit to start the sequencer
  - Auto-clear on invalid sequencer state
- Bit 1: **State Select**
  - 0: Default State
  - 1: Alternative State
  - Used for sequence instruction execution to select execution branch
- Bit 2: **Single Step**
  - 0: Disabled
  - 1: Enabled
  - Set in hardware on invalid instruction or halt condition
- Bit 3: **Single Step Go**
  - 0: Disabled
  - 1: Enabled
  - Start next instruction and auto-clear bit

7.2.7 Instruction and Report Address Offsets (0x0054)

Bit	15	14	13	12	11	10	9	8
Description	Report Address Pointer							

Bit	7	6	5	4	3	2	1	0
Description	Instruction Address Pointer							

- Bit 0-7: **Instruction Address Pointer**
  - Range: 0 - 255
  - Generally pointing to the next word
- Bit 8-15: **Report Address Pointer**
  - Range: 0 - 255
  - Points to SRAM destination address

7.2.8 PLL Loop Filter (0x0096)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Disable Loop Filter	Lock Detection	Increase Loop Gain	Loop Filter Gain		

- Bit 0-3: **Loop Filter Gain**
  - Range: 0 - 15
- Bit 4: **Increase Loop Gain**
  - 0: Disabled
  - 1: Enabled
  - Set to increase PLL loop filter gain by about 60%
- Bit 5: **Lock Detection**
  - 0: Disabled
  - 1: Enabled
  - Must be set for lock detect when LC oscillator not in use
- Bit 6: **Disable Loop Filter**
  - 0: Loop filter not disabled
  - 1: Loop filter disabled
  - Disable loop filter which disables the phase feedback

7.2.9 PLL M and N Factors (0x0098)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Enable all Phases	PLL Enable	PLL Reference Source		N Factor	

Bit	7	6	5	4	3	2	1	0
Description	N Factor				M Factor			

- Bit 0-3: **M Factor**
  - Range: 0 - 15
  - PLL reference clock pre-scaler
- Bit 4-9: **N Factor**
  - Range: 3 - 63
  - VCO output divider
- Bit 10-11: **PLL Reference Source**
  - 0: Internal RC oscillator
  - 1: External clock source
  - 2: External LC oscillator
- Bit 12: **PLL Enable**
  - 0: Disabled
  - 1: Enabled
- Bit 13: **Enable all Phases**
  - 0: Disabled
  - 1: Enabled

7.2.10 Device Configuration (0x009A)

Bit	15	14	13	12	11	10	9	8
Description	Reserved			Select LCO Reference Clock				

Bit	7	6	5	4	3	2	1	0
Description	Measure Phase	Reserved	SRAM Test Select		System Clock Select		PLL Divider Selection	

- Bit 0-1: **PLL Divider Selection**
  - 0: Divide by 2
  - 1: Divide by 3
  - 2: Divide by 4
  - 3: Divide by 5
  - Divide only applies to PLL output for system clock
- Bit 2-3: **System Clock Select**
  - 0: Internal RC oscillator
  - 1: External clock
  - 2: External LC oscillator
  - 3: PLL output
- Bit 4-5: **SRAM Test Select**
  - 0: None - Do not test SRAM on warm-boot
  - 1: Zero - Zero SRAM on warm-boot
  - 2: Partial - Zero and single pass SRAM test on warm-boot
  - 3: Full - Zero and multiple pass SRAM test on warm-boot
- Bit 7: **Measure Phase**
  - 0: Disabled
  - 1: Enabled
  - Generate and measure phases from RC oscillator
- Bit 8-12: **Select LCO Reference Clock**
  - Range: 0 - 22
  - Select LCO engine for clock output to IO5 and IO6

7.2.11 Power Control (0x009C)

Bit	15	14	13	12	11	10	9	8
Description	Reserved			Enable Pad Latch	POR Request	Turn off RC Oscillator	Reserved	Clock Power Control

Bit	7	6	5	4	3	2	1	0
Description	Disable Voltage Regulator Soft-Start	Enable Regulator Status Latch	Disable Voltage Regulators Globally	Enable Trim Latch	Enable Top Voltage Regulator	Enable Right Voltage Regulator	Enable Bottom Voltage Regulator	Enable Left Voltage Regulator

- Bit 0: **Enable Left Voltage Regulator**
  - 0: Disabled
  - 1: Enabled
- Bit 1: **Enable Bottom Voltage Regulator**
  - 0: Disabled
  - 1: Enabled
- Bit 2: **Enable Right Voltage Regulator**
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Enable Top Voltage Regulator**
  - 0: Disabled
  - 1: Enabled
- Bit 4: **Enable Trim Latch**
  - 0: Disabled
  - 1: Enabled
- Bit 5: **Disable Voltage Regulators Globally**
  - 0: Voltage regulators may be enabled individually
  - 1: Voltage regulators disabled
- Bit 6: **Set Regulator Status Latch**
  - 0: No event
  - 1: Set latch in *Regulator Status* register
  - Auto-cleared after latch is set
- Bit 7: **Disable Voltage Regulator Soft-Start**
  - 0: Voltage regulator soft-start enabled
  - 1: Voltage regulator soft-start disabled
- Bit 8: **Clock Power Control**
  - 0: Do not send clock signal to power control logic circuit
  - 1: Send clock signal to power control logic circuit
  - Will automatically clear after state has been updated
- Bit 10: **Disable RC Oscillator**
  - 0: RC Oscillator enabled
  - 1: RC Oscillator disabled
- Bit 11: **Power-on-Reset Request**
  - 0: Do not reset
  - 1: Reset request
- Bit 12: **Enable Pad Latch**
  - 0: Disabled
  - 1: Enabled

7.2.12 Hardware Status (0x00F0)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						LC Oscillator Clock Detect	SRAM Busy

Bit	7	6	5	4	3	2	1	0
Description	Cold Boot Indicator	Reserved	System Clock Source		RC Oscillator Enabled	PLL Locked	PLL Enabled	SRAM Failure

- Bit 0: **SRAM Failure**
  - 0: SRAM test success
  - 1: SRAM test failure
- Bit 1: **PLL Enabled**
  - 0: Disabled
  - 1: Enabled
- Bit 2: **PLL Locked**
  - 0: Not Locked - Not Stable/Enabled
  - 1: Locked - Stable
- Bit 3: **RC Oscillator Enabled**
  - 0: Disabled
  - 1: Enabled
- Bit 4-5: **System Clock Source**
  - 0: Internal RC oscillator
  - 1: External clock
  - 2: External LC oscillator
  - 3: PLL output
- Bit 7: **Cold Boot Indicator**
  - 0: Warm boot
  - 1: Cold boot
  - Cleared when *Clock Power Control* bit is set in *Power Control* register.
- Bit 8: **SRAM Busy**
  - 0: SRAM test active
  - 1: SRAM test inactive
- Bit 9: **LC Oscillator Clock Detect**
  - 0: No LC oscillator clock source detected
  - 1: LC oscillator clock source detected

7.2.13 Regulator Status (0x00F4)

Bit	15	14	13	12	11	10	9	8
Description	Top too High	Top too Low	Top OK Latch	Top OK	Right too High	Right too Low	Right OK Latch	Right OK

Bit	7	6	5	4	3	2	1	0
Description	Bottom too High	Bottom too Low	Bottom OK Latch	Bottom OK	Left too High	Left too Low	Left OK Latch	Left OK

- Bit 0,4,8,12: **OK**
  - 0: Regulator outside band
  - 1: Regulator within band
- Bit 1,5,9,13: **OK Latch**
  - Retain state of OK bit when *Set Regulator Status Latch* bit is set in *Power Control* register.
  - Cleared when OK bit is cleared
  - Indicate when regulator exits band
- Bit 2,6,10,14: **Too Low**
  - 0: Regulator voltage not too low
  - 1: Regulator voltage too low
- Bit 3,7,11,15: **Too High**
  - 0: Regulator voltage not too high
  - 1: Regulator voltage too high

7.2.14 Sensor Configuration 0 (0x0200)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Disable Startup Delay	Enable Common Mode Voltage	Trimming Capacitor			

Bit	7	6	5	4	3	2	1	0
Description	Pad Control		Bias Current					

- Bit 0-5: **Bias Current**
  - Range: 0 - 63
- Bit 6-7: **Pad Control**
  - 0: Dual-pin
  - 1: Single-pin positive
  - 2: Single-pin negative
  - 3: Alternate
- Bit 8-11: **Trimming Capacitor**
  - Range: 0 - 15
- Bit 12: **Enable Common Mode Voltage**
  - 0: Disabled
  - 1: Enabled
- Bit 13: **Disable Startup Delay**
  - 0: Startup delay enabled
  - 1: Startup delay disabled

7.2.15 Sensor Configuration 1 (0x0240)

Bit	15	14	13	12	11	10	9	8
Description	Enable Additional Right Shift	Reserved	Over-sample Factor		Divider			

Bit	7	6	5	4	3	2	1	0
Description	Divider							

- Bit 0-11: **Divider**
  - Range: 1 - 4095
  - LCO clock divider
- Bit 12-13: **Over-sample Factor**
  - 0: 1x
  - 1: 4x
  - 2: 32x
  - 3: 64x
- Bit 15: **Enable Additional Right Shift**
  - 0: Shift right by 1
  - 1: Shift right by 2

7.2.16 Sensor Global Configuration 0 (0x02B0)

Bit	15	14	13	12	11	10	9	8
Description	Map Timer to Count Address	Enable Stretch Start	Number of Phases		Enable Timeout	Startup Delay		

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Enable Amplitude Detection	Amplitude Level			

- Bit 0-3: **Amplitude Level**
  - Range: 0 - 15
  - Threshold selection for amplitude detection circuit
- Bit 4: **Enable Amplitude Detection**
  - 0: Disabled
  - 1: Enabled
- Bit 8-10: **Startup Delay**
  - 0: 16
  - 1: 32
  - 2: 64
  - 3: 96
  - 4: 128
  - 5: 192
  - 6: 256
  - 7: 512
  - Number of system clock pulses before measurement start
  - Timeout starts after writing to *Start Measurement* register
- Bit 11: **Enable Timeout**
  - 0: Disabled
  - 1: Enabled
  - Start timer independent of *Start Measurement* register
- Bit 12-13: **Number of Phases**
  - 0: 2 Phases
  - 1: 4 Phases
  - 2: 8 Phases
- Bit 14: **Enable Stretch Start**
  - 0: Disabled
  - 1: Enabled
  - Enables a longer start pulse to LC oscillator
- Bit 15: **Map Timer to Count Address**
  - 0: Disabled
  - 1: Enabled

7.2.17 Sensor Control and Status (0x02F0)

Bit	15	14	13	12	11	10	9	8
Description	Report Buffer							

Bit	7	6	5	4	3	2	1	0
Description	Hard Reset	Global Enable	Sequencer Halt State	Sequencer Wait State	Error	Timeout	Overflow	Busy

- Bit 0: **Busy**
  - 0: No bits set in *Start Measurement* register. No active sample
  - 1: Sensor is busy. Bits are set in *Start Measurement* register without being set in *Enable Continuous Measurement* register.
- Bit 1: **Overflow**
  - 0: Latest measurement output within 16-bit range
  - 1: Latest measurement output exceeds 16-bit range
  - Only the least-significant word is available in the *Sensor Output* register
- Bit 2: **Timeout**
  - 0: Latest measurement did not trigger a timeout event
  - 1: Latest measurement did trigger a timeout event
- Bit 3: **Error**
  - 0: Latest measurement did not trigger an error event
  - 1: Latest measurement did trigger an error event
- Bit 4: **Sequencer Wait State**
  - 0: Sequencer inactive, or executing other operation
  - 1: Sequencer awaiting event
- Bit 5: **Sequencer Halt State**
  - 0: Sequencer inactive, or executing other operation
  - 1: Sequencer operation has halted
- Bit 6: **Global Sensor Enable**
  - 0: All sensors are disabled
  - 1: Sensors may be configured for measurement
- Bit 7: **Reset**
  - 0: Do not modify engine configuration
  - 1: Clear engine configuration
  - Does not auto-clear after engines have been reset
- Bit 8-15: **Report Address Pointer**
  - Range: 0 - 255
  - Same value as in *Instruction and Report Address Offsets* register

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