IQS7222C DATASHEET

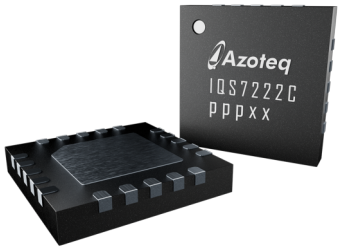
10 Channel Mutual / 8 Channel Self-Capacitive and Inductive Touch and Proximity Controller With I²C Communications Interface, Configurable Outputs and Low Power Options

1 Device Overview

The IQS7222C ProxFusion® IC is a sensor fusion device for various multi-channel sensing structures from button arrays to sliders and wear detection pairs. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) / 8 (WLCSP)external sensor pad connections
- Configure up to 10[i] Channels using the external connections
- External sensor options:
  - Up to 8 self capacitive buttons
  - Up to 4 self capacitive wear detection pairs (with physical reference)
  - Up to 10 mutual capacitive touch/proximity sensors
  - Up to 4 inductive sensor elements for metal detection
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Differential measurements (reference channels)
  - Debounce & Hysteresis
  - Dual direction trigger indication
- Built-in Signal processing options:
  - Slider output
  - Wheel output
  - Up to 4 elements per slider/wheel
  - Up to 2 sliders/wheels simultaneously
  - Slider/wheel gestures to be calculated on host processor
- Design simplicity
  - PC Software for debugging and obtaining optimal settings and performance
  - One-time programmable settings for custom power-on IC configuration
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I²C communication interface with IRQ/RDY(up to fast plus -1MHz)
- Event and streaming modes
- Customizable user interface due to programmable memory
- Supply Voltage 1.8V(-5%)to 3.5V
- Small packages
  - WLCSP18 (1.62 x 1.62 x 0.525 mm) - interleaved 0.4mm x 0.6mm ball pitch
  - QFN20 (3.00 x 3.00 x 0.55 mm) - 0.40mm pitch



QFN20 Package

WLCSP18 Package

[i] WLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured are less than QFN20 package.

1.2 Applications

- SAR Compliance in Mobile devices.
- Wear Detection.
- User interfaces:
  - Capacitive sliders
  - Capacitive buttons
  - Inductive buttons
  - Can be made waterproof
- Low power wake-up on proximity or touch.

1.3 Block Diagram

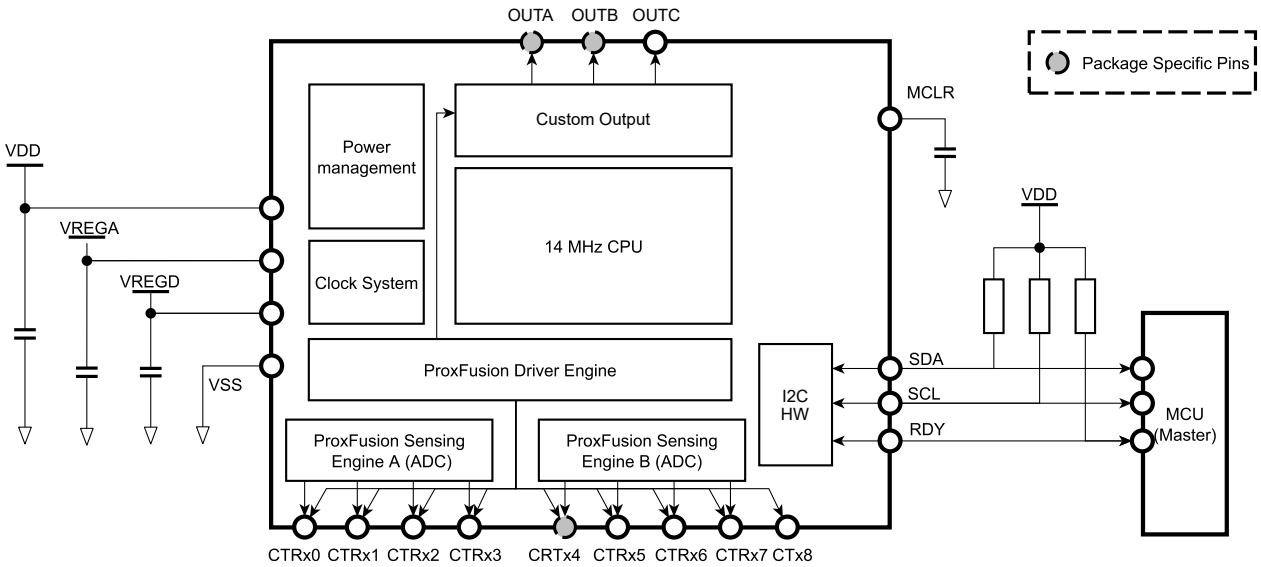


Figure 1.3: Functional Block Diagram[ii]

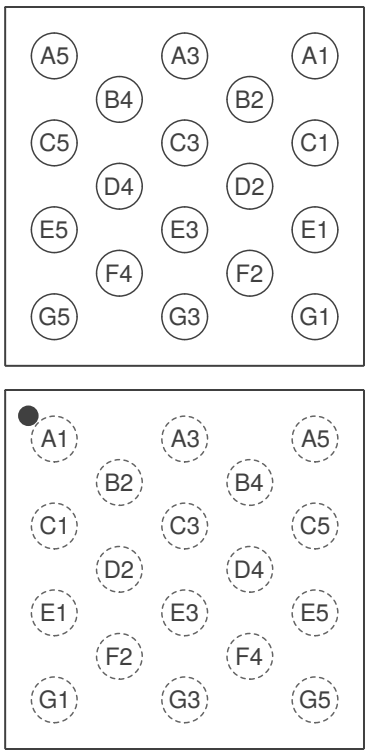
[ii] WLCSP18 packages do not have a CRx4 pin.

Contents

2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

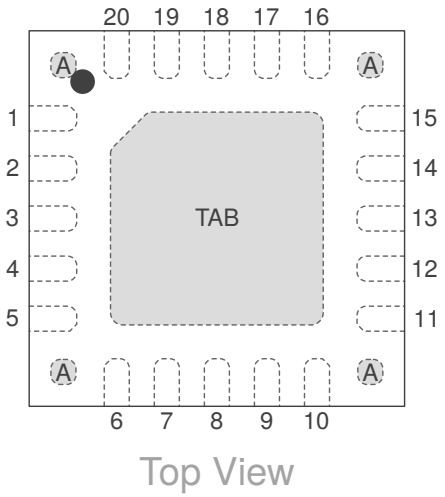
Table 2.1: 18-pin WLCSP18 Package



Pin no.	Signal
A1	OUTA/OUTB[i]
A3	SCL
A5	MCLR
B2	OUTC
B4	SDA
C1	CTx8/Vbias
C3	RDY
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CRx6/CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CRx5/CTx5
F4	CRx0/CTx0
G1	CRx7/CTx7
G3	CRx3/CTx3
G5	VREGA

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8/Vbias
4	VREGA	14	OUTA
5	CRx0/CTx0	15	OUTB
6	CRx1/CTx1	16	OUTC
7	CRx2/CTx2	17	RDY
8	CRx3/CTx3	18	SCL
9	CRx4/CTx4	19	SDA
10	CRx5/CTx5	20	MCLR

Area name	Signal name
TAB[ii]	Thermal pad (floating)
A[iii]	Thermal pad (floating)

[i] WLCSP18 package shares the OUTA and OUTB functions on the same pin. OUTA and OUTB functions should not be enabled at the same time.
[ii] It is recommended to connect the thermal pad (TAB) to VSS.

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8/Vbias	Analog		VREGA
A1	14	OUTA	Digital		VDD
B4	19	SDA	Digital		VDD
A3	18	SCL	Digital		VDD
A1	15	OUTB	Digital		VDD
B2	16	OUTC	Digital		VDD
C3	17	RDY	Digital		VDD
A5	20	MCLR	Digital		VDD

[iii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iv]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CRx4/CTx4	-	9	IO	
	CRx5/CTx5	F2	10	IO	
	CRx6/CTx6	E1	11	IO	
	CRx7/CTx7	G1	12	IO	
	CTx8/Vbias	C1	13	O	CTx8/Vbias pad
GPIO	OUTA	A1	14	O	OUTA pad
	OUTB	A1	15	O	OUTB pad
	OUTC	B2	16	O	OUTC pad
	RDY	C3	17	O	RDY pad
	MCLR	A5	20	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA	B4	19	IO	I^2C data
	SCL	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[iv] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.5 Reference Schematic

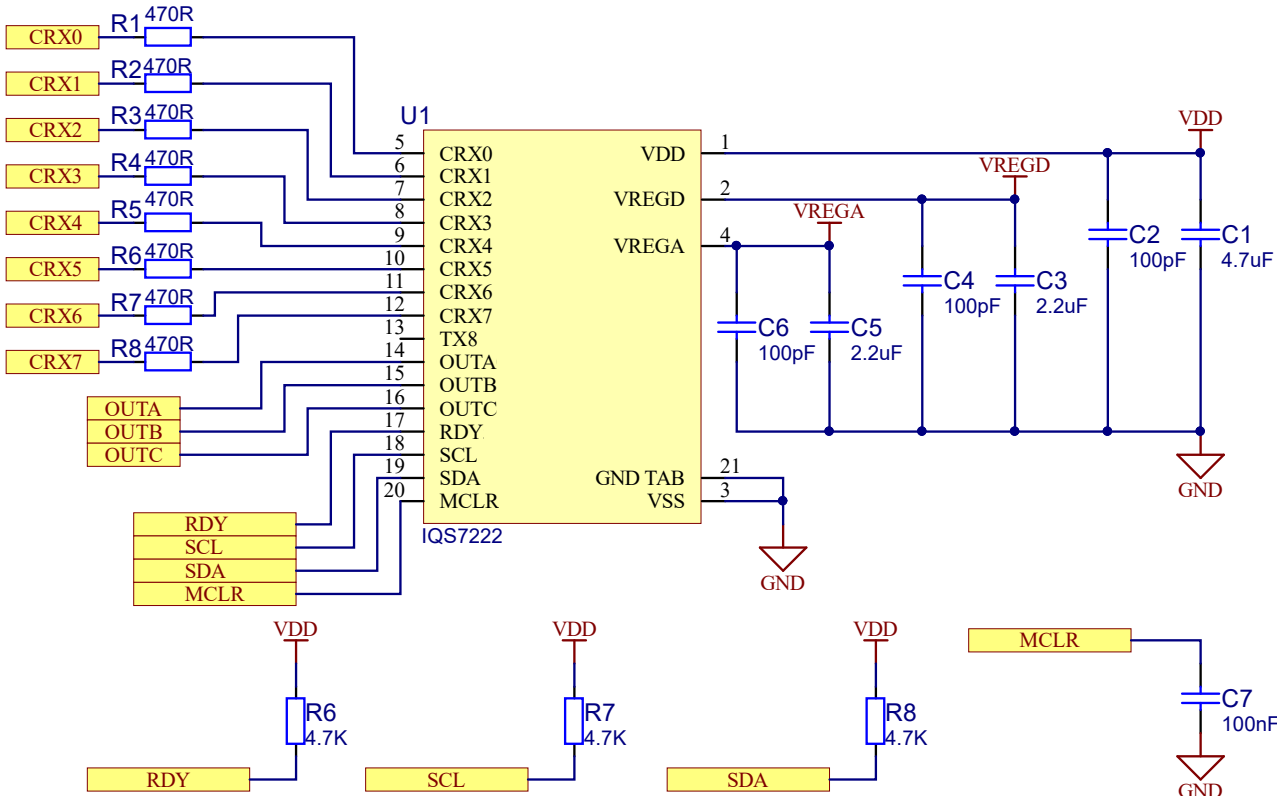


Figure 2.1: 8 Button Self Capacitance Reference Schematic

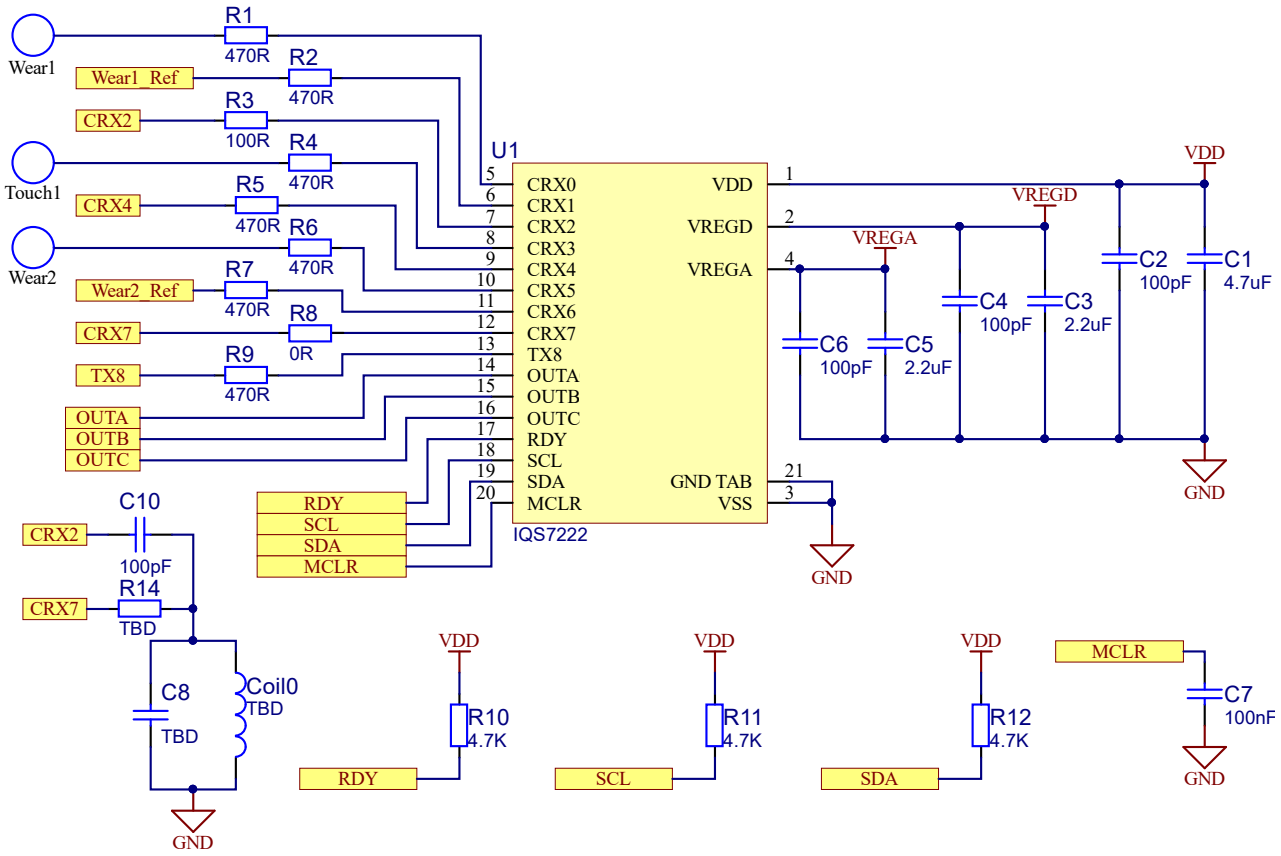


Figure 2.2: Wear, Reference and Inductive Sensing Reference Schematic

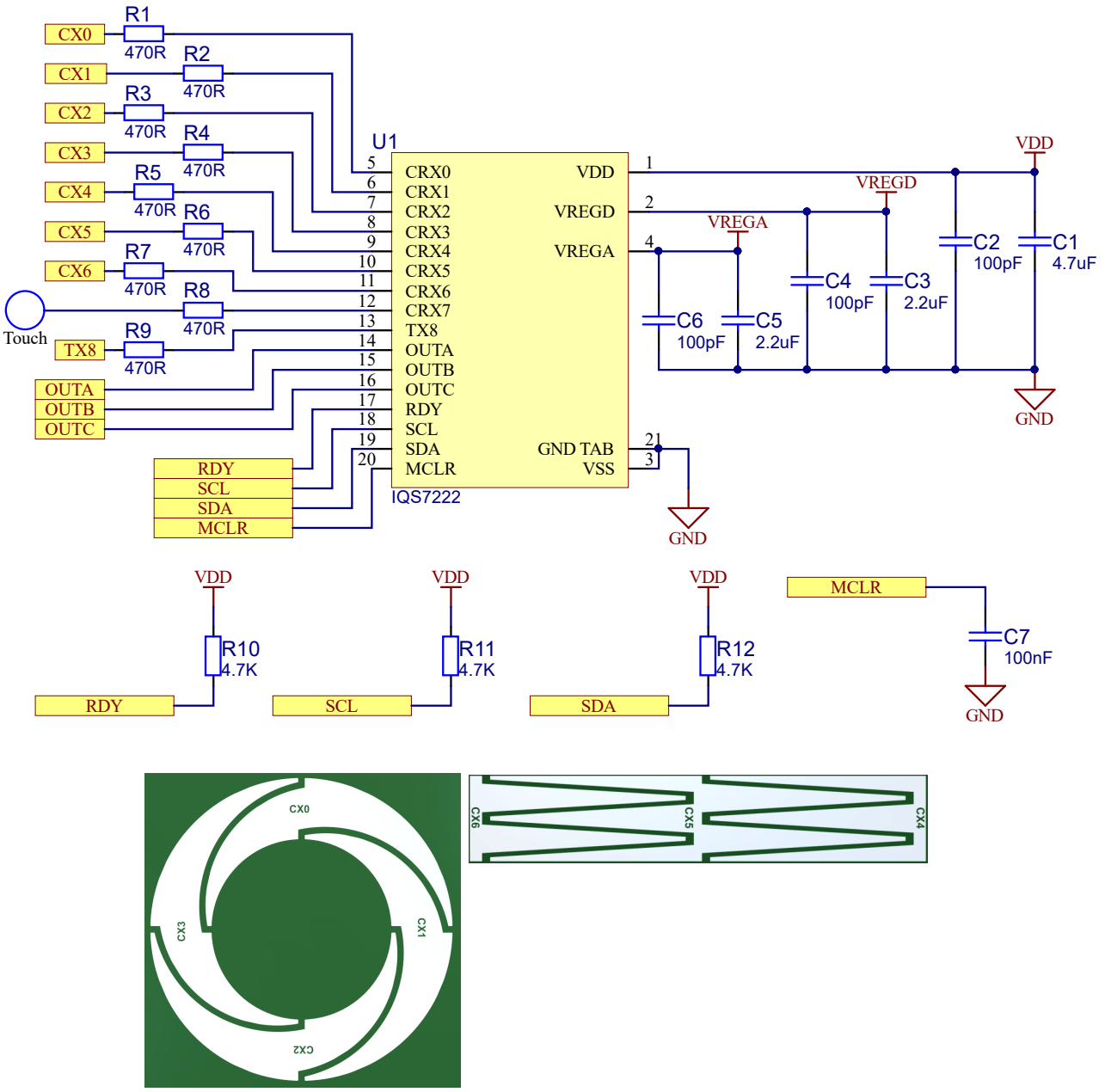
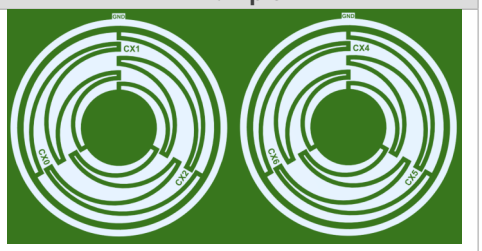
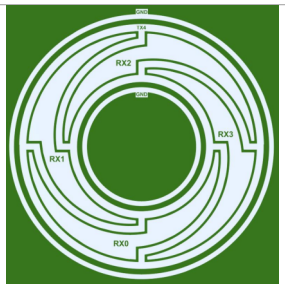


Figure 2.3: 3 Channel Slider, 4 Channel Wheel with Touch Sensor Reference Schematic[v]

[v] Refer to section 2.5.1 for more slider/wheel combinations

2.5.1 Possible Slider/Wheel Combinations

		Example
3 channel self-capacitive wheel	3 channel self-capacitive wheel	
4 channel mutual wheel	-	

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	–40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: f_{OSC} = 14 MHz	1.71		3.6	V
VREGA	Internal regulated supply output for analog domain: f_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: f_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREGA}$	$3\times C_{VREGA}$		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{CTx–CRx}$	Capacitance between receiving and transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{CRx–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode at f_{xfer} = 1 MHz)			100[ii]	pF
$\frac{Cp_{CRx–VSS}}{Cm_{CTx–CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

3.4 Current Consumption

Setup - Self-Capacitive: ATI Target = 512, f_{xfer} = 500 kHz, 16 Auto Mode Update Cycles
Interface Selection: Event mode

Table 3.4: Typical Current Consumption for IQS7222C101

Power mode	Active channels	Report rate (Sampling rate) [ms]	Typical Current [µA]	
			1.8 V	3.3 V
NP	2 Distributed wake up channels, 4 Buttons and 4 Channel Slider (Self-capacitive)	16	367	370
LP		60	96	96
ULP		150	7.6	8.2

Table 3.5: Typical Current Consumption for IQS7222C201[vi]

Power mode	Active channels	Report rate (Sampling rate) [ms]	Typical Current [µA]	
			1.8 V	3.3 V
NP	2 Distributed wake up channels, 4 Buttons and 4 Channel Slider (Self-capacitive)	16	353	355
LP		60	90	91
ULP		150	10.3	10.8

i Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.
ii RCx = 0 Ω.
iii Please note that the maximum values for Cp and Cm are subject to this ratio.
iv Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.
v Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times f_{xfer})}$ where C is the pin capacitance to VSS.
vi JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.
vi Please refer to product information notice PIN-230172 for more details

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

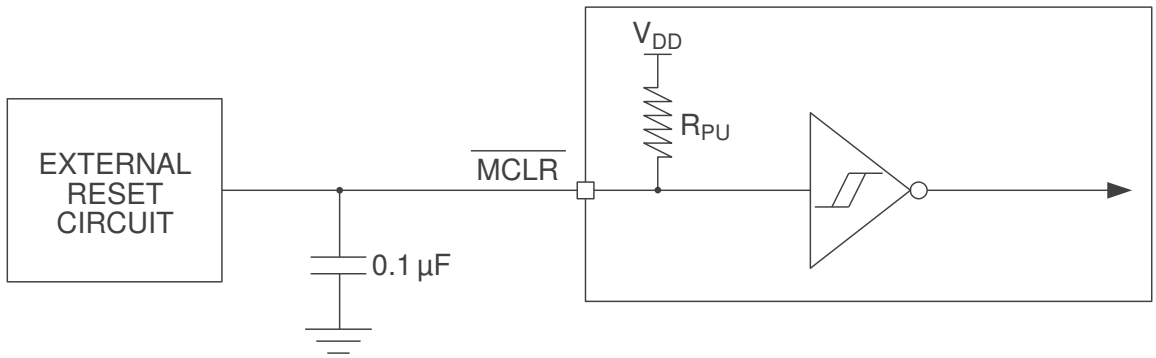


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	55	500 – 1500	7000	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions[i]	Min	Max	Unit
V_{OL}	Output low voltage of SDA and SCL pins	I_{OL} = 20 mA $V_{DD} > 2$ V		0.4	V
		I_{OL} = 20 mA $V_{DD} \leq 2$ V		0.2 V_{DD}	
	Output low voltage of SDA and SCL pins in GPIO output mode	I_{OL} = 10 mA		0.1 V_{DD}	
	Output low voltage of MCLR	I_{OL} = 5 mA			
	Output low voltage of any other GPIO pin	I_{OL} = 10 mA			
V_{OH}	Output high voltage	I_{OH} = −5 mA	0.9 V_{DD}		V
V_{IL}	Input low voltage		V_{SS} − 0.3	0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}	V_{DD} + 0.3	V
C_b	SDA and SCL bus capacitance			550	pF

[i] Standard operating conditions:
V_{DD}: 1.8 V to 3.6 V, unless otherwise stated.
Operating temperature: −20 °C to 80 °C.

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

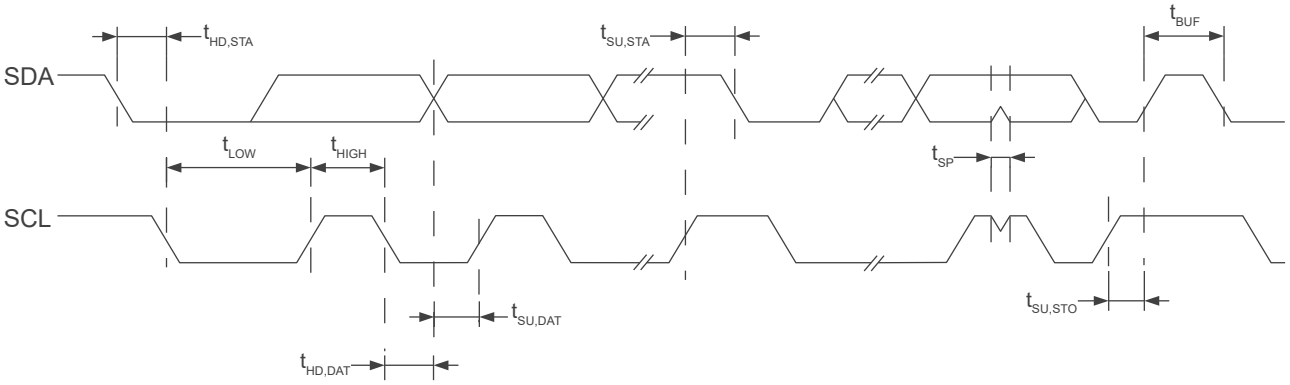


Figure 4.2: I^2C Mode Timing Diagram

4.6 Power-On I²C Timing

4.6.1 Power-On Communication Timing With No I²C

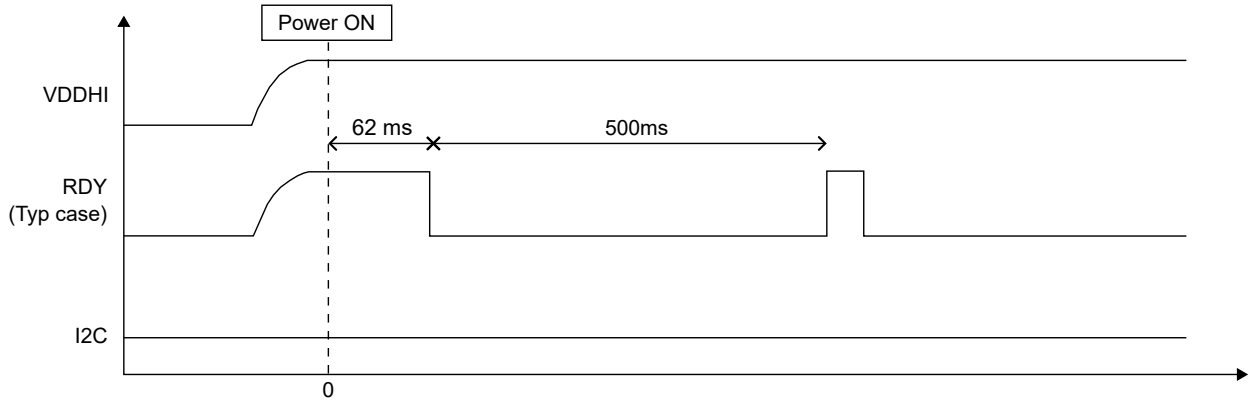


Figure 4.3: Power-On Communications Window Timing With No I²C Initiated

Table 4.6: Communication Window Availability After Power-On

	Min	Typ	Max	Unit
Delay before first communication window after power on (RDY high)	50	62	75	ms
Duration of first communication window (RDY low)	425	500	575	ms

4.6.2 Power-On Communication Timing With I²C

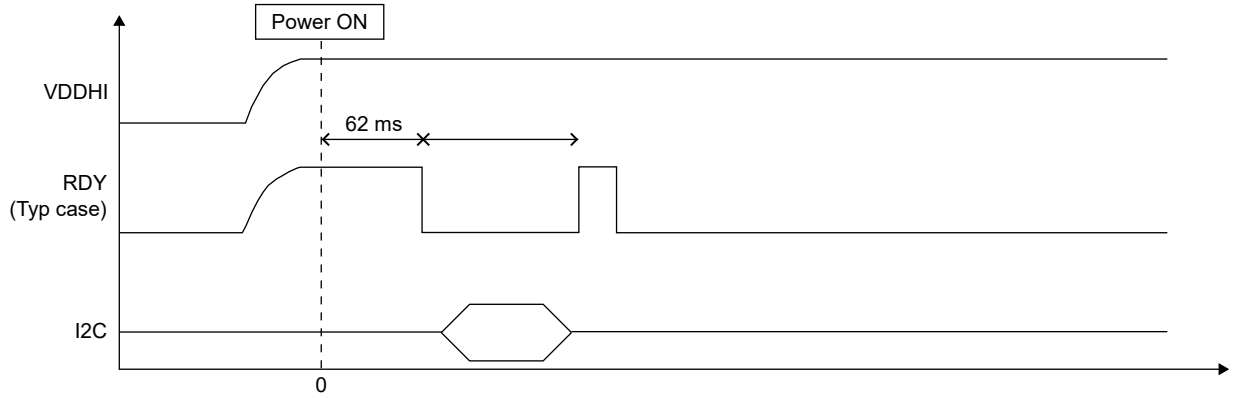


Figure 4.4: Power-On Communications Window Timing With I²C Initiated and Closed

5 ProxFusion® Module

The IQS7222C contains dual ProxFusion® modules which use patented technology to measure and process relative changes in capacitive and inductive sensors. It supports up to 10 sensing channels. The two modules allow for simultaneous sensing of two channels at a time, ensuring a rapid response from multi-channel implementations. Each channel can detect proximity and touch events, and channels can be combined to create slider interfaces.

5.1 Overview

Self-capacitance, mutual capacitance, reference tracking and inductive designs are possible with the IQS7222C.

Please refer to the following application notes for more information:

- AZD004: Azoteq Sensing Technology
- AZD125: Capacitive Sensing Design Guide
- AZD036: Mutual Capacitance Button Layout Guide
- AZD115: Inductive Sensing Design Guide
- AZD137: User Interfaces Application Note

5.2 Counts

Each ProxFusion module reports a sensing measurement as a relative, unit-less value referred to as “Counts”, which are stored as *16-bit values*. These counts report the number of charge transfer cycles necessary to charge an internal sampling capacitor, and are typically inversely proportional to the signal measured on the external sensor. Count values are thus inversely proportional to capacitance/inductance. All further outputs are derived from these counts values.

User interaction is detected by comparing the measured count values to some reference value. The reference value, known as the *Long-Term Average* (LTA), is slowly updated using a low-pass filter to track changes in the environment. Detected proximity and touch events are then reported for each channel in the *Proximity* and *Touch* Event registers.

5.3 Cycle and Channel Relationship

The IQS7222C has 2 Prox engines, A and B, that perform sensing simultaneously. Sensing is performed across 5 time slots, labelled cycle 0 to cycle 4, where each cycle is associated with two channels, one for each Prox engine. The relationship between the cycles and channels is shown in Table 5.1 below.

Table 5.1: Cycle and Channel Relationship

Cycle	Channel on Prox Engine A	Channel on Prox Engine B
Cycle 0	Channel 0	Channel 5
Cycle 1	Channel 1	Channel 6
Cycle 2	Channel 2	Channel 7
Cycle 3	Channel 3	Channel 8
Cycle 4	Channel 4	Channel 9

ProxFusion sensing settings can be either channel-specific or cycle-specific (i.e. applies to both channels in the same cycle). It is important to note that both channels of a particular cycle must use the

same sensing mode (self-capacitance, inductive, etc). Refer to Section 5.7.1 for a list of cycle-specific settings, and Section 5.7.2 for a list of channel-specific settings.

5.4 ProxFusion Hardware Settings

5.4.1 Sensing Mode

Each channel can be independently enabled via the *Channel Enable* bit of the respective channel's *General Channel Setup* register. Additionally, the sensing mode (or *PXS Mode*) of the channel must be specified for the associated cycle in the *Cycle Setup 1* register. Cycle and channel associations are given in Table 5.1.

5.4.2 Rx and Tx Selection

Each sensor must have an associated Rx and Tx selected. Tx pins are assigned per cycle in the *Cycle Setup 1* register, while Rx pins are assigned per channel in the *CRX Select* register.

While any pin may be used as Tx for either prox engine, only certian pins may be used as Rx for each prox engine, as shown in Table 5.2

Table 5.2: Rx Prox Engine Relationship

CRx	Prox Engine A	Prox Engine B
CRx0	✓	-
CRx1	✓	-
CRx2	✓	-
CRx3	✓	-
CRx4	-	✓
CRx5	-	✓
CRx6	-	✓
CRx7	-	✓

Additional notes:

- For self-capacitive sensors, both Rx and Tx must be assigned to the same pin.

5.4.3 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}), also known as the conversion frequency, is set using the *Conversion Frequency Fraction* and *Conversion Frequency Period* fields in the *Cycle Setup 0* register. This frequency is derived from the system clock, f_{OSC}.

For capacitive sensing, a lower frequency allows the capacitive electrode to charge and discharge completely. For inductive sensing, this frequency should be selected based on the resonant frequency of the LC circuit, unless *FOSC Tx Frequency* is used. Lower frequencies may provide more stable measurements, but increase sensing duration and current consumption.

It is recommended to always set the *Conversion Frequency Fraction* to '127' and to select the conversion frequency with the *Conversion Frequency Period*. Please refer to Tables A.7 and A.8 to select suitable *Conversion Frequency Period* values for the desired conversion frequency.

The *Dead Time Enable* option in the *Cycle Setup 1* register must be considered when setting the conversion frequency. Dead time should always be enabled for capacitance measurements, and disabled for inductive measurements.

5.4.4 FOSC Tx Frequency

The *FOSC Tx Frequency* setting in the *Cycle Setup 1* register enables f_{OSC} (14 MHz) as output on the associated Tx pins during sensing.

This can be used to excite resonated inductive sensors at a frequency higher than can be achieved using the charge transfer frequency. This is beneficial for certain inductive sensing applications, but is not supported for capacitive sensing.

5.4.5 Maximum Counts

The *Maximum Counts* setting in the *Global Cycle Setup* register sets the maximum counts value that the Proxfusion engine will allow a particular measurement or channel to reach. This acts as a timeout, stopping the measurement early if the sensing takes too long to complete. The resulting counts stored for that measurement will be set to the maximum counts value. Available values are:

- 1023 counts
- 2047 counts
- 4095 counts
- 16383 counts

The maximum counts should be increased if a high target value is used on a particular channel. (For example, 2047 or 4095 should be used for a channel with a target of 1000). However, this may (situationally) increase current consumption and increase ATI duration.

5.4.6 Cs Size

The *Cs Size* setting in the *CRX Select and General Channel Setup* register sets the size of the internal sampling capacitor to either 40 pF or 80 pF. It is recommended to use the 80 pF capacitor wherever possible. However, the 40 pF capacitor requires only half the amount of charge to reach its threshold voltage, and may therefore be used in designs where the load/signal is very small.

The effective size of the internal sampling capacitor may be further reduced by enabling *Vref 0.5 V Enable* in the *CRX Select and General Channel Setup* register. This setting lowers the threshold voltage on the sampling capacitor. It is recommended to keep this disabled.

5.5 ProxFusion UI Settings

5.5.1 Filtering

Raw counts obtained from the ProxFusion engines are filtered using a low-pass IIR filter to reduce the high-frequency noise in the measurement. The response of the filter can be adjusted with the *Filter Beta* values. Higher beta values result in a slower filter response, with less noise on the measurement. Note that the selected filter beta values apply to all channels.

Separate beta values are used for normal power and lower power modes. It may be beneficial to use a lower beta value for low power modes, which have lower sampling rates, in order to maintain responsiveness to user inputs.

Each beta setting is a 4-bit value, with a range of '0' – '15', where '0' is no filtering, and '15' is maximum filtering. Counts filtering typically uses low values, under '3', to ensure responsiveness.

5.5.2 Long Term Average

The *Long Term Average* (LTA) is derived from the *filtered counts*, and acts as a stable reference value. While the channel is not in activation, the LTA is slowly updated to track changes in the environment using a low-pass filter. During activation, the LTA is kept fixed (halted). The LTA filter response is controlled by the *LTA Beta* values. LTA beta values should typically be '8' or higher.

The difference between the filtered counts and the LTA is stored as the Delta value. The IQS7222C uses this delta value to detect proximity and touch activations.

$$\text{Delta} = \text{LTA} - \text{Counts} \tag{1}$$

5.5.3 Reseed

The *Reseed* function of the device will replace the filtered counts and the LTA value of the channel with the latest sampled raw counts value to reset the environmental reference of the channel. This may be necessary in certain instances when a channel gets incorrectly stuck in an activation.

The *Reseed* command can be given manually by setting the corresponding bit in the *Control Settings* register.

5.5.4 Proximity Event

A proximity event occurs on a channel when the *Delta* exceeds the *Proximity Threshold*, which is set in the *Button Setup 0* register.

To reduce jitter and false events, debouncing is applied to the channel when the delta initially crosses the proximity threshold. Debouncing forces the IQS7222C to perform a number of quick measurements, checking that all measurements exceed the threshold. The number of high-frequency measurements that are executed during debouncing is controlled by the *Button Setup 0* register, and can be configured independently for entering or exiting proximity events. Setting the debounce values to '0' or '1' will disable debouncing.

The proximity threshold and debouncing settings can be configured separately for each channel. An active proximity activation is indicated in the *Proximity Event States* register.

5.5.5 Touch Event

A touch event occurs on a channel when the delta exceeds the touch threshold. The touch threshold is calculated on-chip as a function of the LTA and an 8-bit *Touch Threshold* value stored in the *Button Setup 1* register.

$$\text{T}_{\text{counts}} = \frac{\text{T}_{\text{reg}} \times \text{LTA}}{256} \tag{2}$$

where

- T_{reg} is the 8-bit value stored in the *Touch Threshold* setting, and

- T_{counts} is the resulting threshold value in counts (rounded down).

Touch enter and exit events are not debounced. However, hysteresis is applied on touch release in order to reduce jitter. The size of the hysteresis is controlled by the *Hysteresis* setting in the *Button Setup 1* register, and its value in counts (H_{counts}) is calculated as

$$H_{counts} = \frac{H_{reg} \times T_{counts}}{256} \tag{3}$$

where T_{counts} is obtained from Equation (2), and H_{reg} is the 8-bit *Hysteresis* setting value.

Therefore, taking on-chip integer division into account, the touch "exit" threshold can be calculated as

$$\text{Exit Threshold (counts)} = \text{floor}\left(\frac{\text{LTA} \times \left(T_{reg} - \text{floor}\left(\frac{T_{reg} \times H_{reg}}{256}\right)\right)}{256}\right). \tag{4}$$

For example, assume an LTA value of 500, threshold setting of '20', and a hysteresis setting of '50'. The touch enter threshold in counts is calculated as

$$T_{enter(counts)} = \text{floor}\left(\frac{20 \times 500}{256}\right) = 39 \text{ counts},$$

and the exit threshold is calculated as

$$T_{exit(counts)} = \text{floor}\left(\frac{500 \times \left(20 - \text{floor}\left(\frac{20 \times 50}{256}\right)\right)}{256}\right) = 33 \text{ counts}.$$

5.5.6 Event Direction

Negative delta values are typically ignored, as they typically indicate an unexpected decrease in signal. This can occur due to sudden environmental changes, or due to the user releasing the sensor after the sensor was calibrated while in a touch state. Proximity and touch events are therefore only registered if the delta is positive, or

$$\text{Counts} < \text{LTA} - \text{Threshold}. \tag{5}$$

When a large negative delta is detected, the IQS7222C switches the LTA filter beta to the Fast LTA beta, which can be configured to track the counts more quickly to exit the negative delta state.

This behavior can be modified with the following settings from the *CRX Select and General Channel Setup* register:

- The *Invert* bit changes the sign of the delta, so events are set when

$$\text{Counts} > \text{LTA} + \text{Threshold}. \tag{6}$$

  This is required for mutual capacitive sensing and inductive sensing.
- Bi-directional sensing ignores the sign of the delta, so that events are detected for either positive or negative deltas. The Fast LTA beta is never used.

5.5.7 Event Timeouts

In order to prevent stuck states where a channel is incorrectly stuck in a proximity or touch event (when the LTA filter is halted), the IQS7222C provides timeouts for proximity and touch events. The duration of these timeouts are controlled by the *Proximity Event Timeout* and *Touch Event Timeout* values in the *Button Setup 2* register, and can be set in 500 ms increments. Once the timeout duration expires, the channel is automatically reseeded.

Event timeouts can be configured per-channel. A timeout may be disabled by setting the register value to '0'. Disabling the timeout may be necessary for follower and reference channels, and are required for ULP entry channels retaining an active state in ULP.

5.5.8 Global Halt

The global halt feature provides functionality to halt the LTA filters of certain channels if any of them are in activation.

Global halt can be enabled for any channel by setting the *Global Halt* bit in the channel's *General Channel Setup* register.

If any global-halt-enabled channels are in activation, the *Global Halt* flag in the *System Status* register is set. Once Global Halt is set, all channels that have global halt enabled will keep their LTA values static until all the relevant channels exit activation.

5.6 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in ProxFusion devices to allow optimal performance of the devices for a wide range of sensing electrode designs, without modification to external components. The ATI functionality ensures that sensor sensitivity is not affected by external influences such as temperature, parasitic capacitance, and ground reference changes.

In order for the ProxFusion engine to handle a wide range of capacitive loads and input signals, the IQS7222C provides two mechanisms to condition the input signal for a desired working counts range: gain and DC subtraction. Gain scales the sensor input to a desired range. The amount of gain is controlled by the *Multipliers and Dividers* register. After the gain stage, DC subtraction is performed to compensate for DC offsets and increase sensitivity to changes in the input signal. DC subtraction is controlled by the *Compensation* register. Multipliers, dividers, and compensation are adjusted on a per-channel basis.

The working range of each channel of the IQS7222C can be calibrated automatically using the on-chip ATI feature, which adjusts the *Multiplier and Divider* and *Compensation* registers until the reported counts from the sensor reaches a set of target counts values. These targets are known as the *ATI Base* and *ATI Target*.

The *ATI Base* value sets the desired nominal counts of a channel after the gain stage, and thus controls the amount of gain applied to the input signal. The *ATI Target* value sets the desired raw counts after both the gain and DC subtraction stages. The ATI algorithm first calibrates the multipliers to reach the Base counts, then calibrates the compensation to reach the target counts. Since counts are inversely proportional to signal strength, using DC subtraction will cause an increase in counts. Therefore the Target should always be higher than the Base value if compensation is required. Typical values for the Base value lie between 100 and 500 counts, while the Target is typically set to between 500 and 1000 counts.

Note that the Base value in counts is calculated from the 5-bit register value as Base counts $=$ $16 \times$ *Base Register Value*. The target value in counts is calculated from its 8-bit register value as Target counts $= 8 \times$ *Target Register Value*. Base and target selection also allows for fine adjustment of the sensitivity of the sensor to user interaction, following the relationship

$$\text{Sensitivity} \propto \frac{\text{Target}}{\text{Base}}.$$

Sensitivity can thus be increased by either increasing the Target value or decreasing the Base value. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility.

Compensation is typically not recommended for inductive sensing. Compensation may be disabled by setting Base $\geq$ Target.

ATI can be triggered manually by setting the *ATI* bit in the *Control Settings* register. ATI may also be triggered automatically under certain conditions, described in Section 5.6.3.

5.6.1 ATI Modes

The ATI functionality can be set to one of the following modes:

- Full ATI
- ATI From Coarse Fractional Divider
- ATI From Fine Fractional Divider
- ATI From Compensation Divider
- ATI From Compensation Only
- ATI Disabled

"Full ATI" will calibrate all the *Multipliers and Dividers* and the *Compensation*. "ATI From Compensation Divider" will only calibrate the Compensation register. This allows an application to use a fixed set of Multipliers for all devices across production. "ATI Disabled" will never allow the channel to perform an ATI calibration, even if an ATI command is given.

5.6.2 ATI Error

After the ATI algorithm has completed, a check is performed to verify that no errors occurred during the ATI execution. An *ATI Error* is reported in the *System Status* register if one of the following conditions occur for any channel:

- ATI Compensation = 0 (mininum value)
- ATI Compensation = 1023 (maximum value)
- Reported counts value is outside the Re-ATI range upon completion of the ATI

The *ATI Error* status is only updated the next time ATI executes.

5.6.3 Automatic Re-ATI

The Automatic Re-ATI feature allows for easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor, and can also automatically recalibrate the sensor if environmental drift is detected. It is always recommended to have the automatic Re-ATI functionality enabled. When a Re-ATI is performed on the IQS7222C, a status bit will be momentarily set to indicate that this has occurred.

A Re-ATI is automatically triggered under the following conditions:

- If an ATI Error occurs.
- When the reference of a channel drifts outside of the acceptable range around the ATI Target.

The threshold to trigger an ATI due to reference drift is controlled by the *ATI Band* setting, which is specified as a fraction of the ATI target. The band can be set to one of the following values in the *CRX Select and General Channel Setup* register:

- 1/2
- 1/4
- 1/8
- 1/16

The boundaries around the ATI Target where re-ATI occurs is calculated as $\pm(\text{ATI Target} \times \text{ATI Band})$.

For example, for an ATI Target of 800 counts and an ATI band of 1/8, the boundary value is $800 \times \frac{1}{8} = 100$ counts. If Re-ATI is enabled, the ATI algorithm will be triggered under the following conditions:

$$\text{Reference} < 700 \quad \text{or} \quad \text{Reference} > 900$$

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI Error Timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. The ATI Error Timeout is specified in increments of 0.5 seconds. An ATI error should, however, not occur under normal circumstances.

5.7 Summary of ProxFusion® Settings

5.7.1 Summary of Cycle Settings

Cycle settings apply to both channels associated with that cycle. A list of settings related to cycle setup is given in Table 5.3 below.

Table 5.3: Cycle Settings

Setting	Description
PXS Mode	Sets the sensing mode for the cycle. See Table A.9.
Conversion Frequency Fraction	Sets the conversion frequency. See Section 5.4.3.
Conversion Frequency Period	
Dead Time Enable	Enable for capacitive sensing, disable for inductive sensing. See Section 5.4.3.
F_{OSC} Tx Frequency	Recommended for inductive sensing only. See Section 5.4.4.
Tx Selection	CTx0 to CTx8. See Section 5.4.2.
Maximum Counts	See Section 5.4.5.
Ground Inactive Rx's	Ground or float unused Rx pins. It is always recommended to ground inactive Rxs.
V_{bias} Enable	Enable V_{bias} (constant voltage drive onto CTx8) for resonant inductive sensing. Recommend keeping disabled.

5.7.2 Summary of Channel Settings

Settings related to channel setup are shown in Table 5.4 below.

Table 5.4: Channel Settings

Setting	Description
Channel Enable	Enables sensing on the channel.
Rx Selection	CRx0 to CRx7. See Section 5.4.2.
Cs Size	80 pF recommended. See Section 5.4.6.
Vref 0.5 V Enable	Recommend keeping this disabled. See Section 5.4.6.
Projected Bias Select	Selection of bias current for mutual capacitive mode. Set to 10 µA. See Table A.17.
Proximity Threshold	See Section 5.5.4.
Touch Threshold	See Section 5.5.5.
Proximity Enter Debounce	Section 5.5.4.
Proximity Exit Debounce	Section 5.5.4.
Touch Hysteresis	See Section 5.5.5.
Proximity Event Timeout	Section 5.5.7.
Touch Event Timeout	Section 5.5.7.
ATI Mode	Auto Tuning Implementation mode. See Section 5.6.1.
ATI Base	See Section 5.6.
ATI Target	See Section 5.6.
ATI Band	See Section 5.6.3.
Invert Direction	See Section 5.5.6.
Bi-directional Sensing	See Section 5.5.6.
Global Halt	See Section 5.5.8.

5.7.3 Summary of Global Settings

Global UI settings are listed in Table 5.5 below.

Table 5.5: Global Settings

Setting	Description
Counts Filter Beta	See Section 5.5.1.
Counts Low Power Filter Beta	
LTA Filter Beta	See Section 5.5.2.
LTA Low Power Filter Beta	

LTA Fast Filter Beta	See Section 5.5.6.
LTA Low Power Fast Filter Beta	

5.7.4 Summary of ProxFusion Outputs

ProxFusion sensor output registers are listed in Table 5.6 below.

Table 5.6: ProxFusion Sensor Outputs

Setting	Description
Proximity Event States	Shows proximity state of each channel.
Touch Event States	Shows touch state of each channel.
Channel X Counts	Filtered counts value of each channel.
Channel X LTA	Reference value of each channel.

6 Slider User Interface

The IQS7222C is capable of processing up to two sliders or wheels simultaneously, which report the position of a touch on the slider/wheel. The slider/wheel UI allows for the following combinations:

- 2 x 3 element mutual capacitive sliders
- 2 x 4 element self-capacitive sliders
- 1 x 4 element mutual capacitive slider

The position of the touch on the slider is reported in the *Slider/Wheel Output* register.

6.1 Slider Setup

The slider is enabled by setting the *Total Channels* field in the *Slider Setup 0* register to a valid value and enabling the slider channels by setting the *Channel X Enable* bits in the *Slider Enable Mask* register.

The *Enable Status Link* register must be linked to touch. This activates the slider when any of the enabled channels are in touch.

The *Delta Link* registers, from Delta Link 0 to Delta Link 3, determine the order in which the enabled channels are processed. For example, if channel 1 is the first element in the slider, the *Delta Link 0* register must be set to the appropriate value. Refer to Table A.30 for specific values.

The *Slider Resolution* value defines the output range of the slider position. The touch position ranges from 0 to the *Slider Resolution*, where 0 is the start of the first slider element and the *Slider Resolution* is the end of the last slider element.

The *Upper Calibration Value* field in the *Slider Calibration and Bottom Speed* register and the *Lower Calibration Value* field in the *Slider Setup and Calibration* register are used to offset the end-points of the slider position so that they match the end-points of the physical slider.

The slider output position is dynamically filtered based on the *Slow/Static Beta* in the *Slider Setup and Calibration* register, the *Bottom Speed* field in the *Slider Calibration and Bottom Speed* register, and the value in the *Slider Top Speed* register. The *Slider Top Speed* and *Bottom Speed* are specified in pixels per sample period. Therefore, giving an indication of finger movement speed, i.e. how much the slider output (in pixels) has changed in a sampling period. Figure 6.1 shows the behaviour of the dynamic filter.

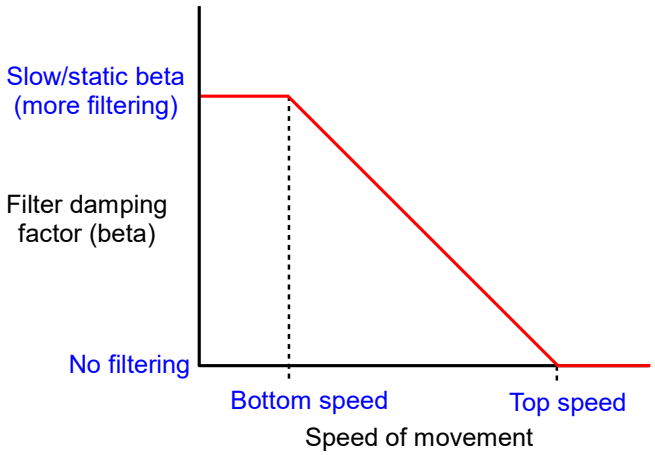


Figure 6.1: Slider Filtering When the Static Filter Bit is Not Set

Bottom and top speed parameters ensure stronger filtering when changes in slider position are in the region of the bottom speed, while ensuring no filtering when the slider position changes rapidly as defined in the top speed parameter. This has value in precise slider applications with very fine adjustment requirements while not losing reactivity when larger movements are made.

If the *Static Filter* bit in the *Slider Setup and Calibration* register is set, the *Slow/Static Beta* is used to filter the slider position regardless of the touch's movement speed.

7 Sensing Modes

7.1 Power Mode and Mode Timeout

The IQS7222C offers 3 power modes:

- Normal power mode (NP)
  - Flexible key scan rate
- Lower power mode (LP)
  - Flexible key scan rate
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimised firmware setup.
  - Intended for rapid wake-up on a single channel (e.g., distributed proximity event), enabling immediate button response for an approaching user.
  - The wake-up channels are sampled at the ULP report rate. These channels are updated at the rate calculated by ULP-RR $\times$ AUTO Mode Register Value.
  - The other sensors are sampled at the rate specified in the normal power update rate in the ultra-low power register.

To optimise power consumption and performance, power modes are "stepped" by default to move to power-efficient modes when no interaction has been detected for a certain (configurable) time known as the "mode timeout". The value for the power mode to never timeout (i.e, the current power mode will never progress to a lower power mode) is 0x00.

7.1.1 Ultra-Low Power Mode

In ULP mode, only Cycle 0 (Channels 0 and 5) are sampled. These channels should be used as wake-up channels, allowing the IQS7222C to wake up and switch to a higher power mode when detecting any user interaction.

CH0 and CH5 are sampled at the *ULP report rate*. LTA and filter values for CH0 and CH5 are not processed every cycle, but are processed once every N cycles, based on the *Auto Mode* setting in *Global Cycle Setup*.

The IQS7222C will also wake up periodically to perform a full “Normal Power” cycle. Here, all channels are sampled, and their respective LTAs updated, in order to maintain consistent environmental tracking. The rate at which the IQS7222C performs these “Normal Power” cycles is controlled by the *Normal Power Update Rate in ULP* parameter, also known as the *ULP Timeout*. After this cycle, the IQS7222C returns to ULP mode.

8 Additional Features

8.1 Debug and Display Software (GUI)

The Azoteq IQS7222C GUI can be utilised to configure the optimal settings required for a specific hardware setup or application. The device performance can be easily monitored and evaluated in the graphical environment until the optimal device configuration is obtained.

Once the IQS7222C is configured in the GUI as desired, a C header file (*.h* file) can be exported that stores the values of all the read-write registers of the IQS7222C. The *.h* file displays the start address of each block of data, with each address containing two bytes in little endian order. An example of the *.h* file exported by the GUI is shown below.

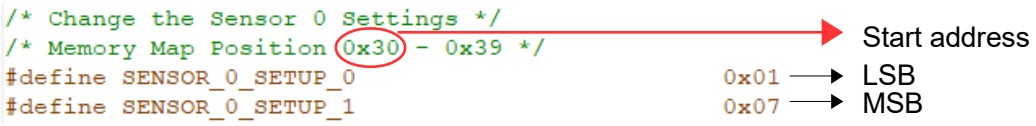


Figure 8.1: Example of an H file Exported by the GUI

8.2 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (Low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.
- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.
- The default, fixed value of the watchdog timer is 1500 ms.

8.3 RF Immunity

The IQS7222C has immunity to high-power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100 pF in parallel with the 2.2 µF ceramic on V_{REG}. Place a 4.7 µF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470 Ω – 1 kΩ. PCB ground planes also improve noise immunity.

8.4 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*. If it becomes set again, the master will know a reset has occurred and can react appropriately.

While the *Reset* bit remains set:

- The device will not be able to enter into I²C Event mode operation (i.e. streaming communication behavior will be maintained until the Reset bit is cleared).
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in much longer time to finish the ATI routine.

8.5 Software Reset

The IQS7222C can be reset by means of an I²C command (*Soft Reset*).

9 Program Flow Diagram

The program flow for event mode communication is shown in Figure 9.1.

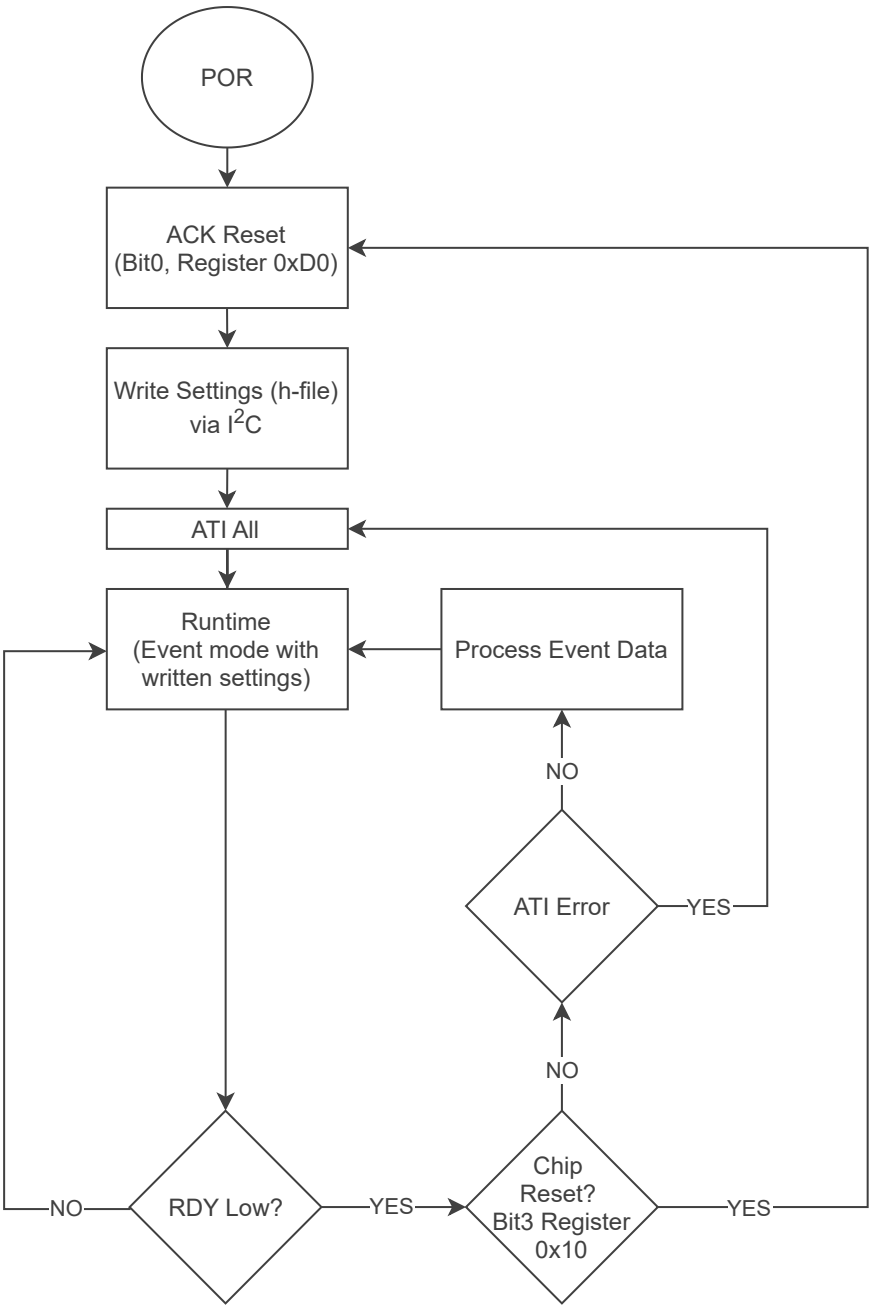


Figure 9.1: Program Flow Diagram

10 I²C Interface

10.1 I²C Module Specification

The device features a standard two-wire I²C interface, complemented by a RDY (ready interrupt) line, supporting a maximum bit rate of up to 1 Mbit/s. The IQS7222C implements a combination of 8-bit addressing and 16-bit addressing, with 2 data bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes, stored at each address in little-endian order, will be referred to as “byte 0” (least significant byte) and “byte 1” (most significant byte).

Features:

- Standard two-wire interface with RDY interrupt line
- *Fast-Mode Plus* I²C with up to 1 Mbit/s bit rate
- 7-bit device address
- Combination of 8-bit and 16-bit register addressing
- Two data bytes stored per register address, in little-endian order
- Streaming and Event modes

10.2 I²C Address

The 7-bit device address for order codes 101 and 201 is 0x44 (0b1000100), while the 7-bit device address for order codes 102 and 202 is 0x45 (0b1000101). The full address byte for address 0x44 will thus be 0x89 (read) or 0x88 (write), and the full address byte for address 0x45 will be 0x8B (read) or 0x8A (write).

Other address options exist on special request. Please contact Azoteq.

10.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

10.4 Memory Map Addressing

10.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement a 16-bit addressing scheme.

10.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to address each block as an 8-bit address and then continue to clock into the next address locations. Figure 10.1 depicts a hypothetical procedure to read data from address 0xE000 to 0xE003 by sending 0xE0 as the register address.

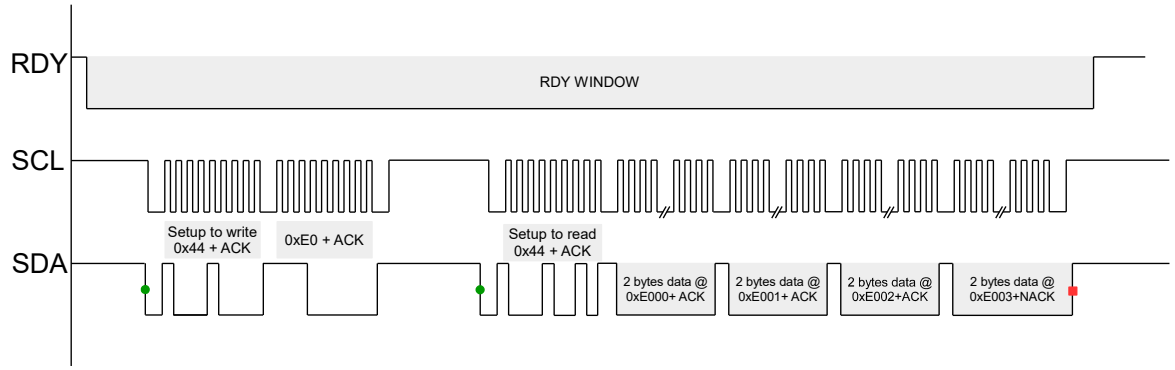


Figure 10.1: Extended 16-bit Addressing for Continuous Block

However, in order to address specific bytes in the extended memory map space, the full 16-bit address must be sent in big endian order (most significant byte first). Below is an example of reading data bytes from register 0xE003.

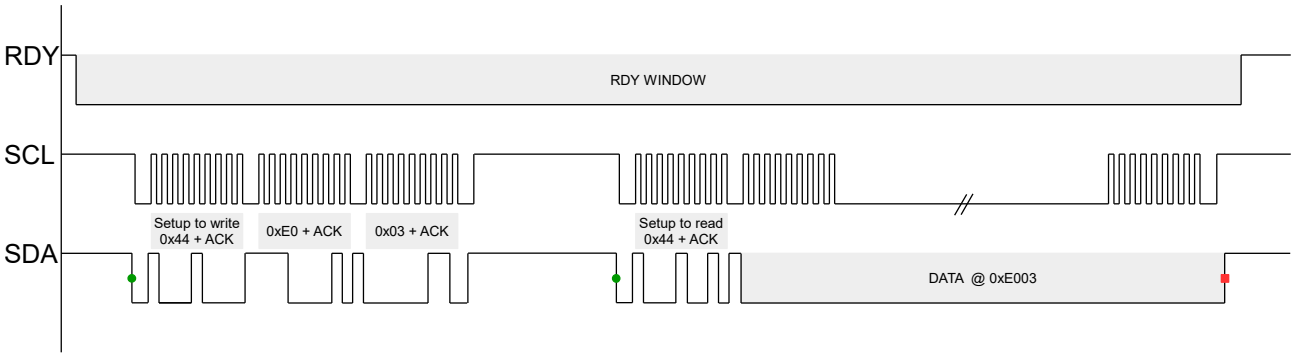


Figure 10.2: Extended 16-bit Addressing for a Specific Register

Note that extended 16-bit addresses are sent in big endian order, but data from those addresses is stored in little endian format.

10.5 Memory Map Data

Data is stored in 16-bit words, meaning that each address contains two bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11. The 16-bit data is sent in little endian byte order (least significant byte first).

10.6 RDY/IRQ

The IQS7222C has an open-drain active low RDY signal to inform the master that updated data is available. The IQS7222C will pull the RDY line low to indicate that it has opened a communications window, or “RDY window”, for the master to read the new updated data. While the master can communicate with the device at any time according to the *Force Communication Method*, it is recommended to use the RDY signal for optimal power consumption. Integrating the RDY signal as an interrupt input allows the master MCU to read and write data efficiently.

The IQS7222C will open a communication window when new data is available, and will typically close the window after an I^2C stop event is detected.

10.7 I²C Interface Modes

The IQS7222C has three *I²C interface options*:

- **Streaming Mode**: The IQS7222C opens a communication window (by pulling the RDY pin low) after every sensing cycle to report new data. This mode is useful for evaluation and debugging.
- **Event Mode**: A communication window is opened only if an enabled event occurs, and activity is detected. This reduces the amount of unnecessary I²C traffic and RDY interrupts, and is the recommended mode for normal operation.
- **Stream in Touch Mode**: Stream in Touch is a hybrid between Streaming Mode and Event Mode. The device follows the Event Mode I²C protocol. When a touch is registered on any channel, the device enters Streaming Mode until the touch is released. This mode is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

10.8 Event Mode Communication

Event Mode bypasses the communication window when no activity is sensed. This is usually enabled since the master does not need to be interrupted unnecessarily during every cycle if no activity occurs. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

Event Mode can only be entered if the following requirements are met:

- Events must be serviced by reading from the *Events* register to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every cycle, similar to streaming mode.
- The *Device Reset* bit in the *System Status* register has been cleared by setting the *Acknowledge Reset* bit in *Control Settings*.

10.8.1 Events

Numerous events can be individually enabled to trigger communication in Event Mode. Bit definitions can be found in Tables A.2 and A.3:

- Power mode change
- Prox or touch event
- ATI event

10.8.2 Force Communication

In Streaming Mode, the IQS7222C I²C will provide communication windows at regular intervals specified by the relevant power mode report rate. This will provide the master with regular opportunities to perform I²C communication as necessary.

If the device is placed in Event Mode, the IQS7222C will not open RDY windows unless certain conditions are met. A new RDY window can be requested by writing 0xFF over I²C, followed by a stop condition. After a short delay, the IQS7222C will pull the RDY line low and open a new communication window. This is shown in Figure 10.3.

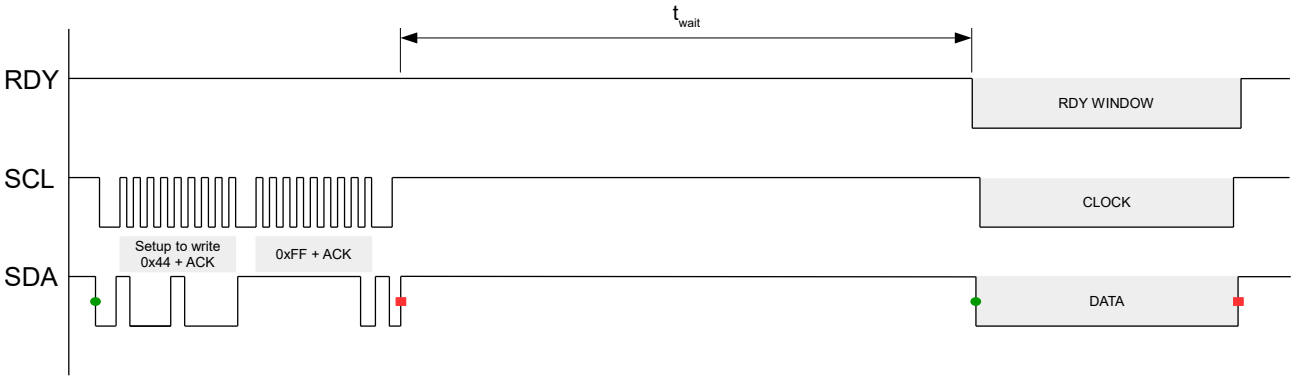


Figure 10.3: Force Communication Sequence

The time between the communication request and the opening of a RDY window (t_{wait}) is dependent on the specific application. Once the communication request is received, the IQS7222C wakes up from sleep mode, performs sampling and processing on all channels, and then opens a communication window. As a result, t_{wait} is dependent on channel and cycle settings, and may be on the order of 10 ms for a full 10-channel device.

Note: The IQS7222C may clock stretch (hold the SCL line low) for up to 400 µs after the 0xFF byte if the force communication command is received while the IQS7222C is in an internal sleep mode.

A force communication request should be avoided while RDY is held low, as the STOP condition after the 0xFF byte will cause an existing communication window to close immediately.

10.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside a communication window (while RDY is high).

10.10 I²C Timeout

If the communication window is not serviced within the *Communication Timeout* period (in milliseconds), the session is ended (RDY goes high), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be lost, so this should be avoided. The default I²C timeout period is set to 500 ms.

10.11 Terminate Communication

By default, a standard I²C STOP will end the current communication window. If multiple I²C transactions need to be performed within a single communication window, they should be strung together using repeated START conditions, with only the last transaction ending with a STOP. Allowing an I²C STOP to terminate the communication window is recommended.

However, for I²C controllers that cannot support repeated START conditions, the IQS7222C provides an option to ignore the STOP condition and keep the window open. This behaviour can be enabled by setting the *Stop Bit Disabled* bit in the *I²C Communication* register.

In this case, the communication window can be terminated as desired using one of the following methods:

- Writing a single 0xFF byte will close the communication window, as illustrated in Figure 10.4.

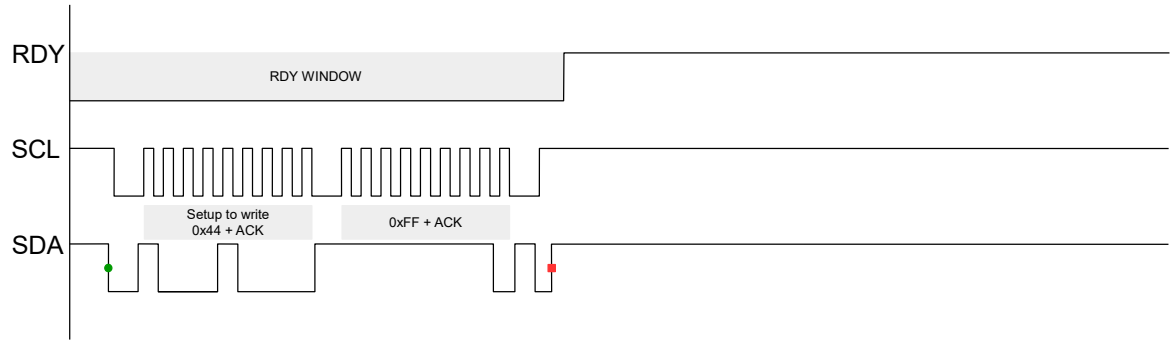


Figure 10.4: Force Stop Communication Sequence

- Alternatively, in each communication window, the stop bit check may be disabled in the first transaction, followed by normal I²C transactions. The window can be closed by re-enabling the check as the final transaction, followed by a STOP.

10.12 Summary of I²C Settings

Table 10.1: I²C Module Settings

Setting	Description
Interface selection	Enable Streaming or Event Mode. See Section 10.7.
Event Mask	Sets which system events should open a communication window if in Event mode. See Section 10.8.1.
Stop Bit Disabled	See Section 10.11.
RW Check Disabled	See Table A.36.
I²C Communication Timeout	See Section 10.10.

11 GPIO Output

The IQS7222C provides three general-purpose output pins, labelled OUTA, OUTB, and OUTC. Each of these pins can be assigned to one (or more) output "channels", which are called *Output 0*, *Output 1*, and *Output 2*. The output channel can either assign the output pins to be used as general purpose outputs or to represent the Proximity or Touch state of specific channels. Essentially, each output channel maps a register state to a particular output pin.

11.1 Initial Setup

To enable a specific GPIO output channel (Output X), the *Enable* bit in the corresponding *Output X Control* register needs to be set. The *Output X Control* register also selects which of the OUTx pins is assigned to that particular output channel by setting the corresponding OUTx bit. Any/all of the OUTx bits can be set, allowing the output to be reported on multiple pins. Finally, each output channel supports either push-pull active-high mode or open-drain active-low mode, which can be selected in the *Output X Control* register.

11.2 ProxFusion State Output

Each GPIO output channel can assign any number of ProxFusion channel (CH0 – CH9) states to one or more of the OUTx pins. The output channel needs to be set to Proximity or Touch mode by setting the output *Status Link* to either 'Prox' or 'Touch' in the corresponding *Status Link Control* register. This "links" either the *Proximity Event States* or the *Touch Event States* register to the output channel. The *Output X Enable Mask* then sets which bits (sensing channels) are used to determine the output pin state.

As an example, consider the following application requirements for Output 0:

- Report the Touch state of ProxFusion Channel 3,
- Output pin: OUTC
- Pin mode: Active-high (push-pull)

In other words, if CH3 experiences a touch event, OUTC pin will be high for the duration of the touch event, and low otherwise. The necessary settings to meet these requirements are:

1. Enable the output by setting the *Enable* and *OUTC* bits in the *Output 0 Control* register.
2. Clear the *Output Configuration* bit in the *Output 0 Control* register to set the pin to active-high.
3. Set Touch control mode in the *Output 0 Status Link* register.
4. Set the *CH3* bit in the *Output 0 Enable Mask* register.

It is possible to report the Prox or Touch state of multiple prox channels on a single output channel by setting all the required channel bits in the *Output X Enable Mask* register. For the example above, if both CH3 and CH9 bits are set then if either of those channels has an active touch event, the state will be reported on the OUTC pin. Similarly, by setting both the OUTB and OUTC bits in the *Output 0 Control* register, both pins will then report the Touch event state of CH3 simultaneously.

11.3 General Purpose Output

Each GPIO output channel can assign a direct state (low or high) to one or more of the output pins (OUTx). To enable a output channel as a direct output, the channel needs to be set to *Direct* mode by setting the 'Direct' output value in the corresponding *Status Link Control* register. This "links" the *GPIO Direct Output Control* register to the output channel.

Additionally, in the *Output X Enable Mask* register, the bit corresponding to the Output channel number must be set. For example, if Output 1 is being used, bit 1 must be set.

The output state of the channel can then be controlled by modifying the corresponding bit in the *GPIO Direct Output Control* register.

For example, to use Output 0 to directly control OUTB in active-high (push-pull) mode, the setup procedure is as follows:

1. Enable the output by setting the *Enable* and *OUTB* bits in the *Output 0 Control* register.
2. Clear the *Output Configuration* bit in the *Output 0 Control* register to set the pin to active-high.
3. Set bit 0 in the *Output 0 Enable Mask* register.
4. Use bit 0 in the *GPIO Direct Output Control* register to control the state of the Output 0 (OUTB) pin.

12 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address	Data (16bit)	Default	Notes
0x00 - 0x09	Version details		See Table A.1
Read Only			
0x10	System Status		See Table A.2
0x11	Events		See Table A.3
0x12	Prox event States		See Table A.4
0x13	Touch event States		See Table A.5
0x14	Slider/Wheel 0 Output		16-bit value
0x15	Slider/Wheel 1 Output		
Read Only	**Channel Counts**		
0x20	Channel 0 Counts		16-bit value
0x21	Channel 1 Counts		
0x22	Channel 2 Counts		
0x23	Channel 3 Counts		
0x24	Channel 4 Counts		
0x25	Channel 5 Counts		
0x26	Channel 6 Counts		
0x27	Channel 7 Counts		
0x28	Channel 8 Counts		
0x29	Channel 9 Counts		
Read Only	**Channel LTA**		
0x30	Channel 0 LTA		16-bit value
0x31	Channel 1 LTA		
0x32	Channel 2 LTA		
0x33	Channel 3 LTA		
0x34	Channel 4 LTA		
0x35	Channel 5 LTA		
0x36	Channel 6 LTA		
0x37	Channel 7 LTA		
0x38	Channel 8 LTA		
0x39	Channel 9 LTA		
Read-Write	**Cycle Setup**		
0x8000	Cycle Setup 0	0x0C7F	See Table A.6
0x8001		0x7FE1	See Table A.9
0x8002		0x0000	See Table A.10
0x8100	Cycle Setup 1	0x0C7F	See Table A.6
0x8101		0x08E1	See Table A.9
0x8102		0x0000	See Table A.10
0x8200	Cycle Setup 2	0x0C7F	See Table A.6
0x8201		0x1161	See Table A.9
0x8202		0x0000	See Table A.10
0x8300	Cycle Setup 3	0x0C7F	See Table A.6
0x8301		0x2261	See Table A.9
0x8302		0x0000	See Table A.10
0x8400	Cycle Setup 4	0x0C7F	See Table A.6
0x8401		0x4461	See Table A.9
0x8402		0x0000	See Table A.10
0x8500	Global Cycle Setup	0x2B8B	See Table A.11

0x8501	Coarse and Fine Divider Preloads	0x3010	See Table A.12
0x8502	Compensation Preload	0x0200	See Table A.13
Read-Write	**Button Setup - Thresholds, Hysteresis and Debounce**		
0x9000	Button Setup 0	0x120A	See Table A.14
0x9001		0x0019	See Table A.15
0x9002		0x2808	See Table A.16
0x9100	Button Setup 1	0x120A	See Table A.14
0x9101		0x0019	See Table A.15
0x9102		0x2808	See Table A.16
0x9200	Button Setup 2	0x120A	See Table A.14
0x9201		0x0019	See Table A.15
0x9202		0x2808	See Table A.16
0x9300	Button Setup 3	0x120A	See Table A.14
0x9301		0x0019	See Table A.15
0x9302		0x2808	See Table A.16
0x9400	Button Setup 4	0x120A	See Table A.14
0x9401		0x0019	See Table A.15
0x9402		0x2808	See Table A.16
0x9500	Button Setup 5	0x120A	See Table A.14
0x9501		0x0019	See Table A.15
0x9502		0x2808	See Table A.16
0x9600	Button Setup 6	0x120A	See Table A.14
0x9601		0x0019	See Table A.15
0x9602		0x2808	See Table A.16
0x9700	Button Setup 7	0x120A	See Table A.14
0x9701		0x0019	See Table A.15
0x9702		0x2808	See Table A.16
0x9800	Button Setup 8	0x120A	See Table A.14
0x9801		0x0019	See Table A.15
0x9802		0x2808	See Table A.16
0x9900	Button Setup 9	0x120A	See Table A.14
0x9901		0x0019	See Table A.15
0x9902		0x2808	See Table A.16
Read-Write	**Channel Setup- ATI Parameters, Reference Channel and Rx Select**		
	Channel 0		
0xA000	CRX Select and General Channel Setup	0x11F3	See Table A.17
0xA001	ATI Base and Target	0x643D	See Table A.19
0xA002	Fine and Coarse Multipliers	0x3028	See Table A.20
0xA003	ATI Compensation	0x59DA	See Table A.21
0xA004	Reference Channel Settings 0	0x0000	See Table A.22
0xA005	Reference Channel Settings 1	0x0000	See Table A.23
	Channel 1		
0xA100	CRX Select and General Channel Setup	0x1113	See Table A.17
0xA101	ATI Base and Target	0x3E3D	See Table A.19
0xA102	Fine and Coarse Multipliers	0x332A	See Table A.20
0xA103	ATI Compensation	0x61D9	See Table A.21
0xA104	Reference Channel Settings 0	0x046C	See Table A.22
0xA105	Reference Channel Settings 1	0x0100	See Table A.23
	Channel 2		
0xA200	CRX Select and General Channel Setup	0x1123	See Table A.17

0xA201	ATI Base and Target	0x3E3D	See Table A.19
0xA202	Fine and Coarse Multipliers	0x312B	See Table A.20
0xA203	ATI Compensation	0x69FD	See Table A.21
0xA204	Reference Channel Settings 0	0x0694	See Table A.22
0xA205	Reference Channel Settings 1	0x0002	See Table A.23
	Channel 3		
0xA300	CRX Select and General Channel Setup	0x1143	See Table A.17
0xA301	ATI Base and Target	0x3E3D	See Table A.19
0xA302	Fine and Coarse Multipliers	0x2F08	See Table A.20
0xA303	ATI Compensation	0x61E3	See Table A.21
0xA304	Reference Channel Settings 0	0x04C0	See Table A.22
0xA305	Reference Channel Settings 1	0x0100	See Table A.23
	Channel 4		
0xA400	CRX Select and General Channel Setup	0x1183	See Table A.17
0xA401	ATI Base and Target	0x3E3D	See Table A.19
0xA402	Fine and Coarse Multipliers	0x332A	See Table A.20
0xA403	ATI Compensation	0x61DC	See Table A.21
0xA404	Reference Channel Settings 0	0x0694	See Table A.22
0xA405	Reference Channel Settings 1	0x0008	See Table A.23
	Channel 5		
0xA500	CRX Select and General Channel Setup	0x11F3	See Table A.18
0xA501	ATI Base and Target	0x643D	See Table A.19
0xA502	Fine and Coarse Multipliers	0x3026	See Table A.20
0xA503	ATI Compensation	0x59DB	See Table A.21
0xA504	Reference Channel Settings 0	0x0000	See Table A.22
0xA505	Reference Channel Settings 1	0x0000	See Table A.23
	Channel 6		
0xA600	CRX Select and General Channel Setup	0x1113	See Table A.18
0xA601	ATI Base and Target	0x3E3D	See Table A.19
0xA602	Fine and Coarse Multipliers	0x31B0	See Table A.20
0xA603	ATI Compensation	0x69F1	See Table A.21
0xA604	Reference Channel Settings 0	0x053E	See Table A.22
0xA605	Reference Channel Settings 1	0x0100	See Table A.23
	Channel 7		
0xA700	CRX Select and General Channel Setup	0x1123	See Table A.18
0xA701	ATI Base and Target	0x3E3D	See Table A.19
0xA702	Fine and Coarse Multipliers	0x31EB	See Table A.20
0xA703	ATI Compensation	0x69FA	See Table A.21
0xA704	Reference Channel Settings 0	0x0694	See Table A.22
0xA705	Reference Channel Settings 1	0x0040	See Table A.23
	Channel 8		
0xA800	CRX Select and General Channel Setup	0x1143	See Table A.18
0xA801	ATI Base and Target	0x3E3D	See Table A.19
0xA802	Fine and Coarse Multipliers	0x33AA	See Table A.20
0xA803	ATI Compensation	0x61DC	See Table A.21
0xA804	Reference Channel Settings 0	0x0592	See Table A.22
0xA805	Reference Channel Settings 1	0x0100	See Table A.23
	Channel 9		
0xA900	CRX Select and General Channel Setup	0x1183	See Table A.18
0xA901	ATI Base and Target	0x3E3D	See Table A.19
0xA902	Fine and Coarse Multipliers	0x3149	See Table A.20

0xA903	ATI Compensation	0x6A00	See Table A.21
0xA904	Reference Channel Settings 0	0x0694	See Table A.22
0xA905	Reference Channel Settings 1	0x0100	See Table A.23
Read-Write	**Filter Betas**		
0xAA00	Filter Beta	0x7812	See Table A.24
0xAA01	Fast Filter Beta	0x0034	See Table A.25
Read-Write	**Slider 0 Setup**		
0xB000	Slider 0 Setup and Calibration	0x3C53	See Table A.26
0xB001	Slider 0 Calibration and Bottom Speed	0x0146	See Table A.27
0xB002	Top Speed	0x00C8	16-bit value
0xB003	Resolution	0x07D0	
0xB004	Enable Mask	0x0000	See Table A.28
0xB005	Enable Status Link	0x0696	See Table A.29
0xB006	Delta Link 0	0x048C	See Table A.30
0xB007	Delta Link 1	0x04B6	See Table A.30
0xB008	Delta Link 2	0x04E0	See Table A.30
0xB009	Delta Link 3	0x0000	See Table A.30
Read-Write	**Slider 1 Setup**		
0xB100	Slider 1 Setup and Calibration	0x005C	See Table A.26
0xB101	Slider 1 Calibration and Bottom Speed	0x0100	See Table A.27
0xB102	Top Speed	0x00C8	16-bit value
0xB103	Resolution	0x07D0	
0xB104	Enable Mask	0x0000	See Table A.28
0xB105	Enable Status Link	0x0000	See Table A.29
0xB106	Delta Link 0	0x0534	See Table A.30
0xB107	Delta Link 1	0x055E	See Table A.30
0xB108	Delta Link 2	0x0588	See Table A.30
0xB109	Delta Link 3	0x05B2	See Table A.30
Read-Write	**GPIO Settings**		
0xC000	Output 0 Control	0x0005	See Table A.31
0xC001	Output 0 Enable Mask	0x0021	See Table A.32
0xC002	Output 0 Status Link	0x0696	See Table A.33
0xC100	Output 1 Control	0x0000	See Table A.31
0xC101	Output 1 Enable Mask	0x0000	See Table A.32
0xC102	Output 1 Status Link	0x0000	See Table A.33
0xC200	Output 2 Control	0x0000	See Table A.31
0xC201	Output 2 Enable Mask	0x0000	See Table A.32
0xC202	Output 2 Status Link	0x0000	See Table A.33
Read-Write	**PMU and System Settings**		
0xD0	Control settings	0x0030	See Table A.34
0xD1	ATI Error Timeout	0x0002	16-bit value * 0.5 (s)
0xD2	ATI Report Rate	0x0000	16-bit value (ms)
0xD3	Normal Power Mode Timeout	0x1388	16-bit value (ms)
0xD4	Normal Power Mode Report Rate	0x0010	16-bit value (ms) Range: 0 - 3000
0xD5	Low Power Mode Timeout	0x1388	16-bit value (ms)
0xD6	Low Power Mode Report Rate	0x003C	16-bit value (ms) Range: 0 - 3000
0xD7	Normal Power Update rate in Ultra-low Power Mode	0x2710	16-bit value (ms)
0xD8	Ultra-low Power Mode Report Rate	0x0096	16-bit value (ms) Range: 0 - 3000

0xD9	Event Enable	0xFFFF	See Table A.35
0xDA	I^2C Communication	0x000C	See Table A.36
0xDB	GPIO Direct Output Control	0x0000	See Table A.37
0xDC	Communication Timeout	0x01F4	See Table A.38

13 Implementation and Layout

13.1 Layout Fundamentals

Note: Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

13.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

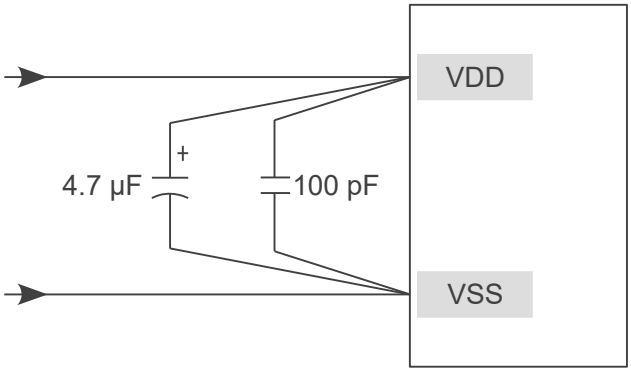


Figure 13.1: Recommended Power Supply Decoupling

13.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. Figure 13.2 below shows an example placement of the VREG capacitors.

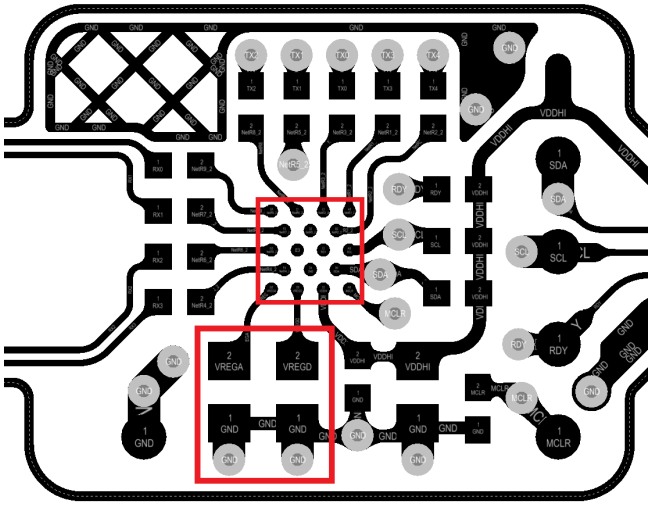


Figure 13.2: VREG Capacitor Placement Close to IC

13.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

14 Ordering Information

14.1 Ordering Code

IQS7222C zzz ppb

Figure 14.1: Order Code Description

IC NAME			IQS7222C
POWER-ON CONFIGURATION	zzz	=	001 Reserved 101 8-button self-capacitance startup, configurable via I²C.[i] 102 8-button self-capacitance startup, configurable via I²C.[ii] 201[iii] 8-button self-capacitance startup, configurable via I²C.[i] 202[iii] 8-button self-capacitance startup, configurable via I²C.[ii]
PACKAGE TYPE	pp	=	CS WLCSP-18 package QN QFN-20 package QF QFN-20 package
BULK PACKAGING	b	=	R WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Example : IQS7222C101QFR

14.2 Top Marking

14.2.1 WLCSP18 Package Marking

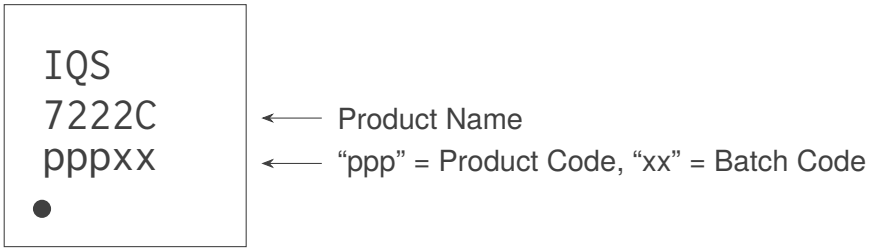


Figure 14.2: IQS7222C-WLCSP18 Package Top Marking

[i] I²C address = 0x44
[ii] I²C address = 0x45
[iii] Please refer to product information notice PIN-230172 for more details

14.2.2 QFN20 Package Marking Option (IQS7222CzzzQNR)

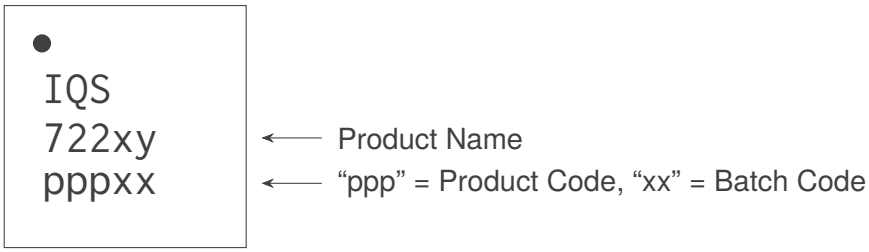


Figure 14.3: IQS722xy-QFN20 Package Top Marking

14.2.3 QFN20 Package Marking Option (IQS7222CzzzQFR)

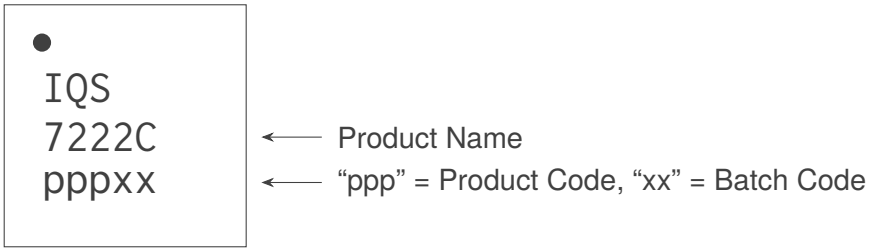


Figure 14.4: IQS7222C-QFN20 Package Top Marking

15 Package Specification

15.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

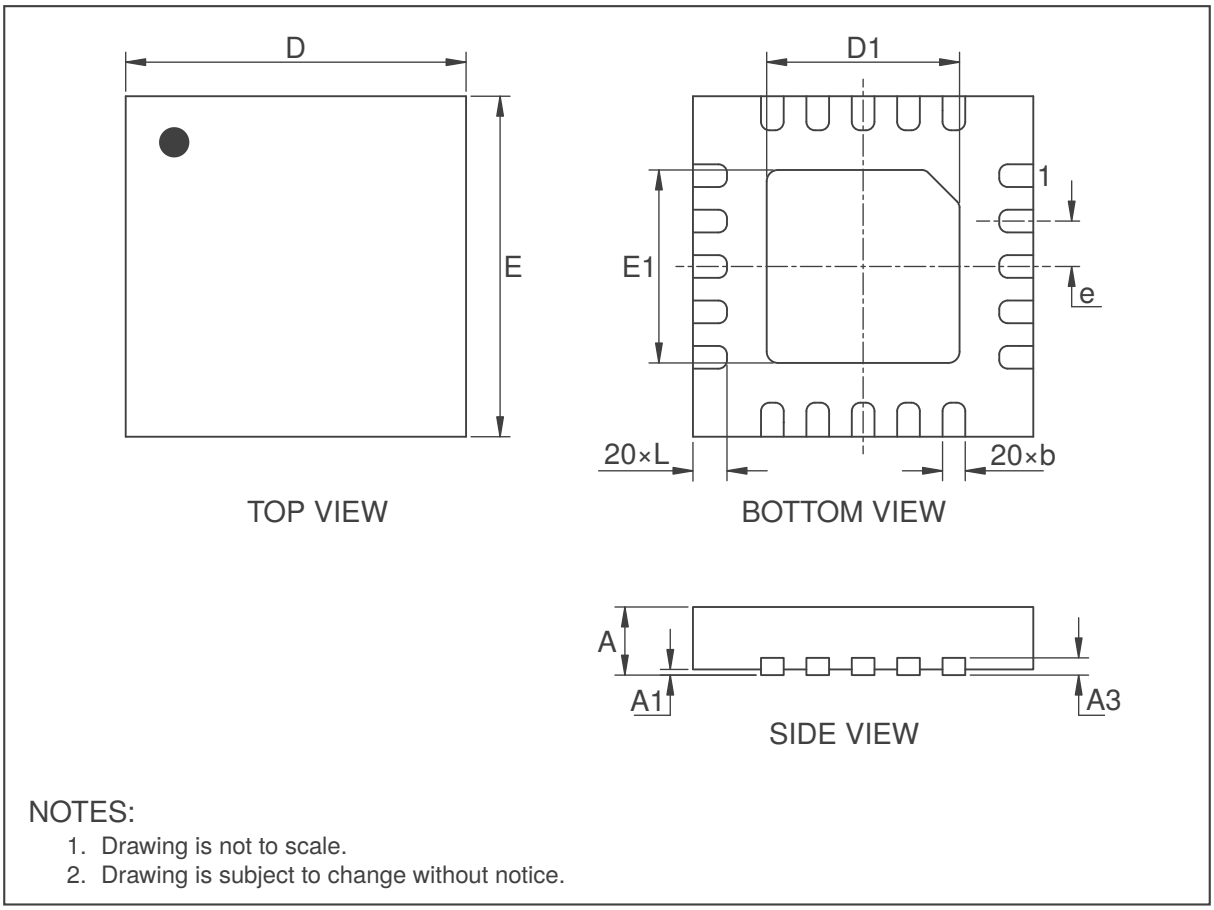
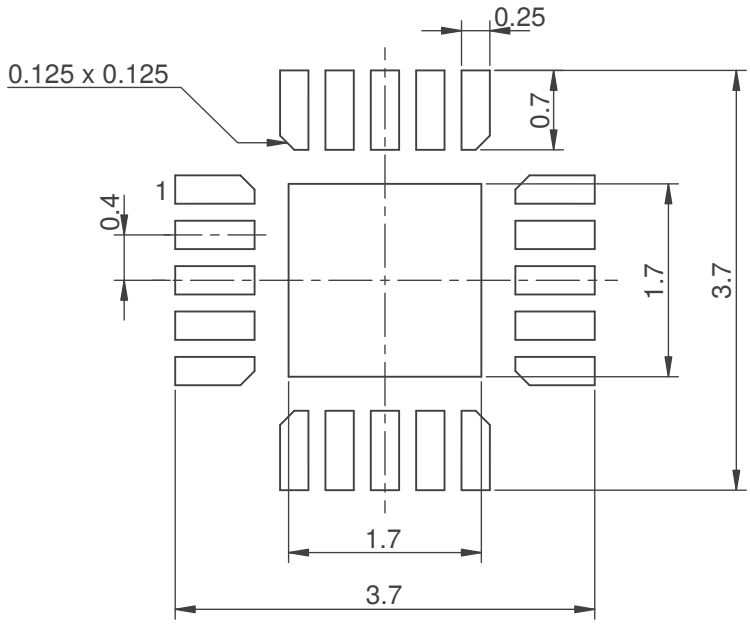


Figure 15.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

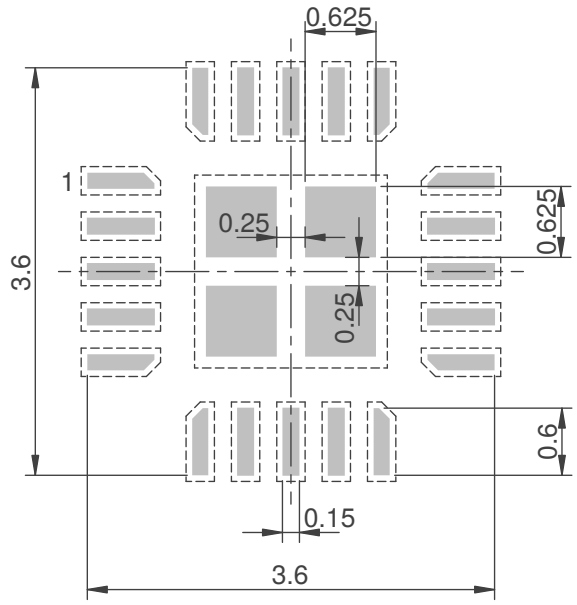
Table 15.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

15.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 15.2: QFN (3x3)-20 (QFR) Recommended Footprint

15.3 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

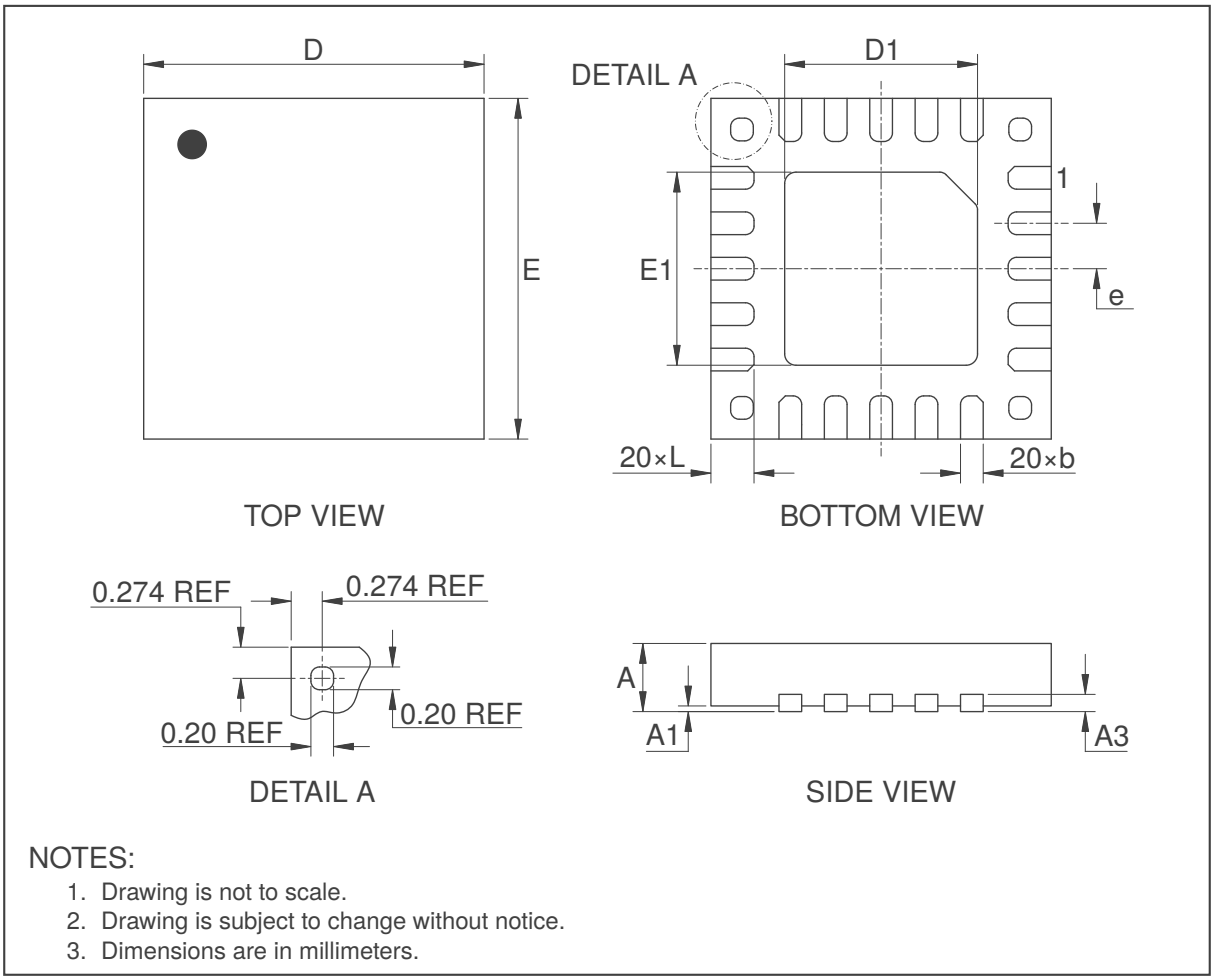
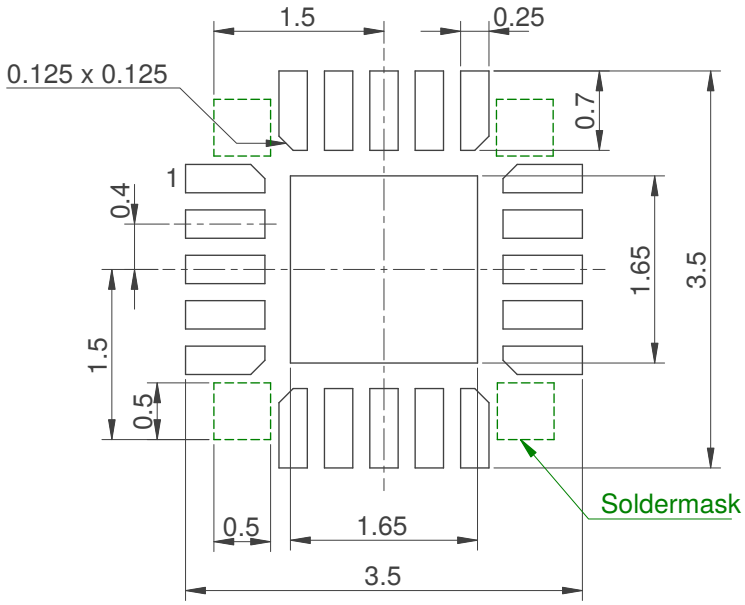


Figure 15.3: QFN (3x3)-20 (QNR) Package Outline Visual Description

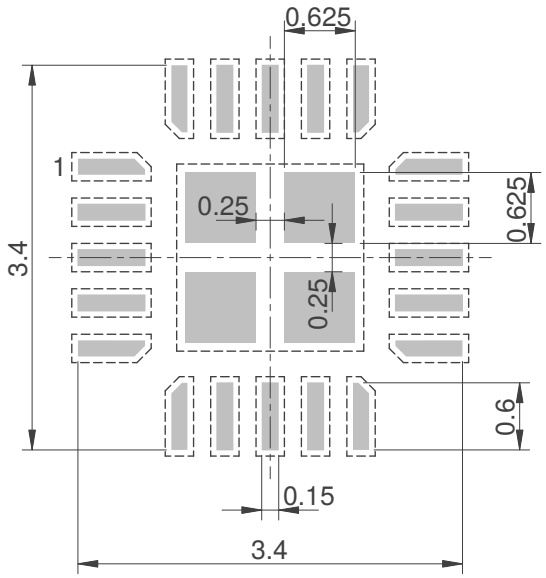
Table 15.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

15.4 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 15.4: QFN (3x3)-20 (QNR) Recommended Footprint

15.5 Package Outline Description – WLCSP18

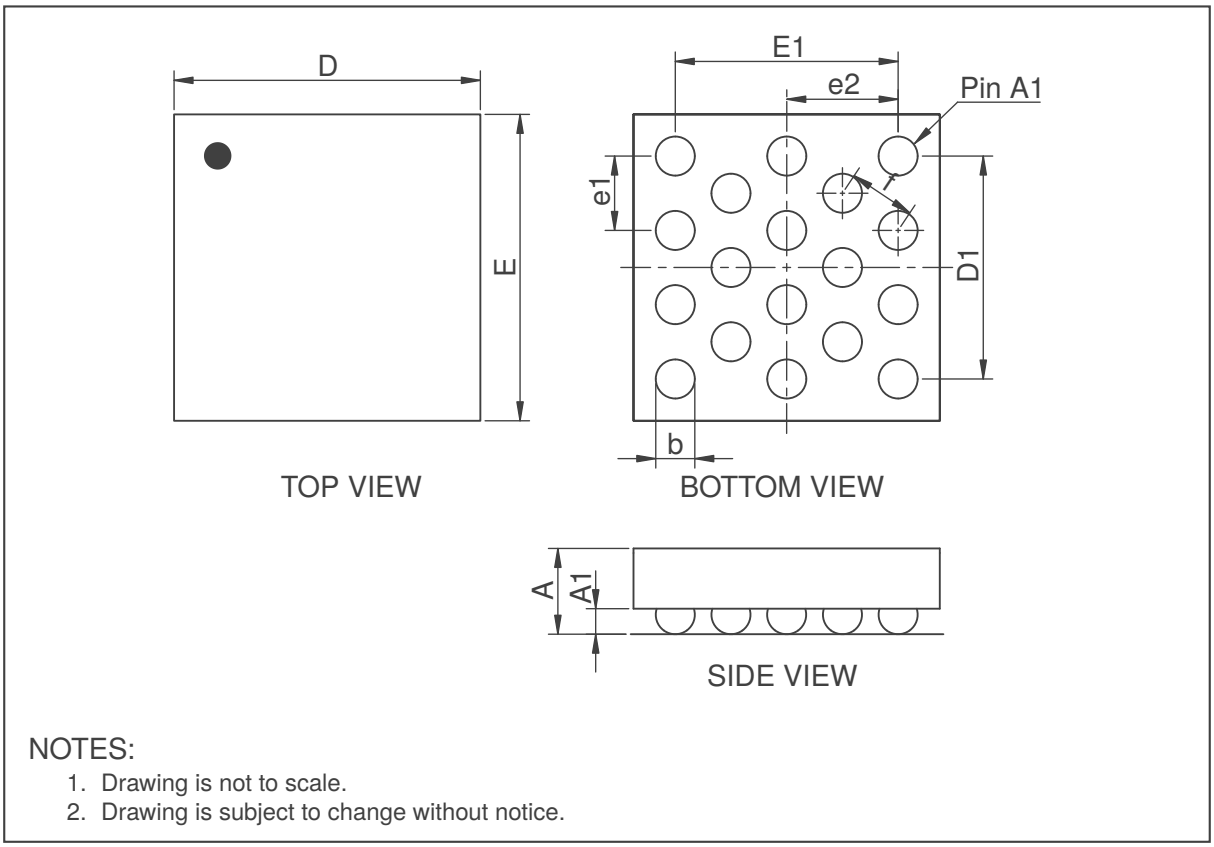
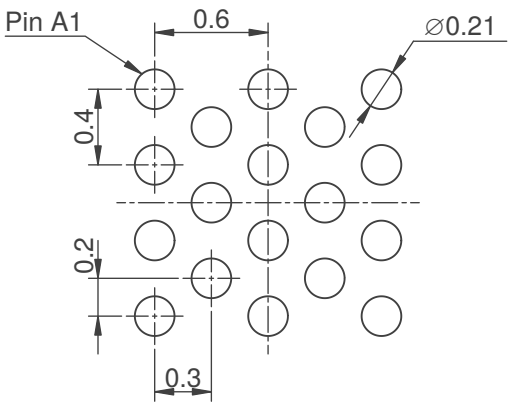


Figure 15.5: WLCSP (1.62x1.62)-18 Package Outline Visual Description

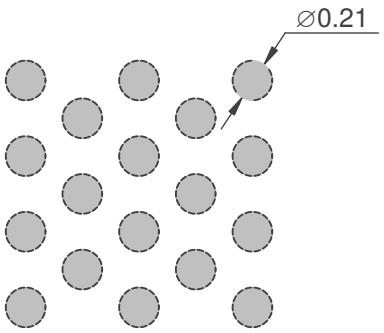
Table 15.3: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1	1.200 BSC		
E1	1.200 BSC		
e1	0.400 BSC		
e2	0.600 BSC		
f	0.360 REF		

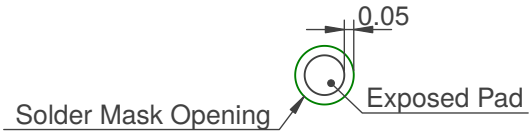
15.6 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



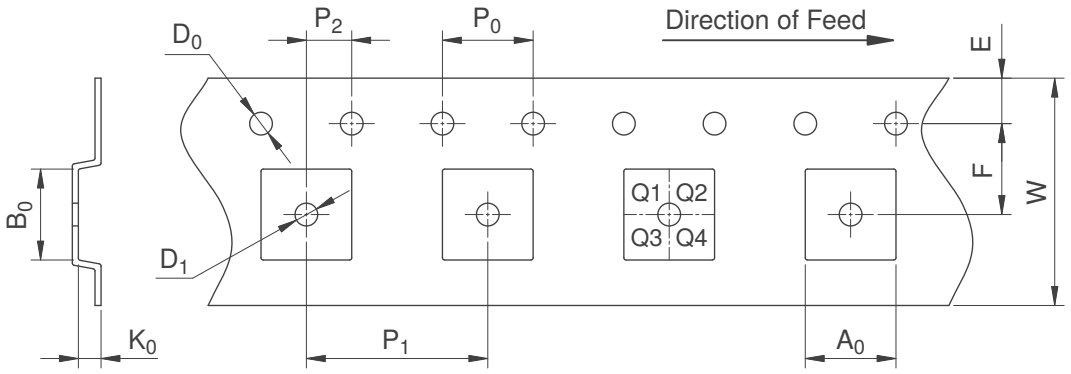
SOLDER MASK BACK-OFF

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 15.6: WLCSP18 Recommended Footprint

15.7 Tape and Reel Specifications

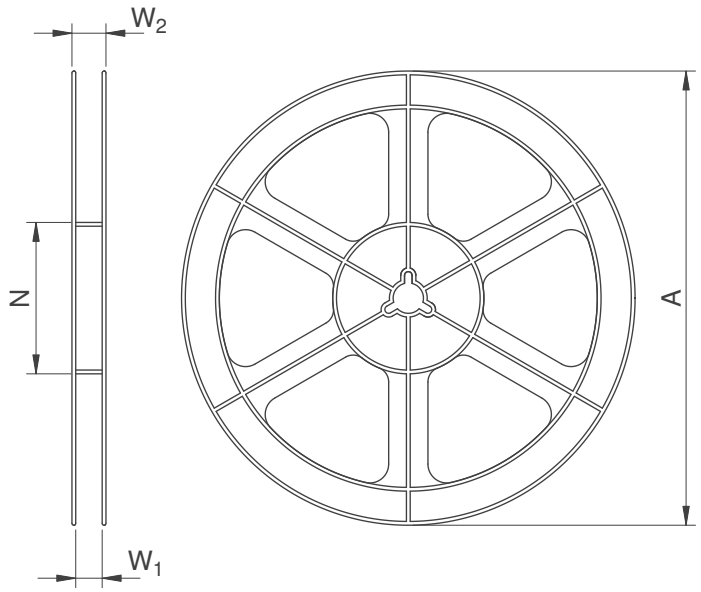


NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 15.7: Carrier Tape Specification

Table 15.4: Carrier Tape Dimensions [mm]

Dimension	Package		
	WLCSP18	QFN20 (QFR)	QFN20 (QNR)
A_0	1.78	3.30	3.30
B_0	1.78	3.30	3.30
K_0	0.69	0.75	0.80
D_0	1.50	1.50	1.55
D_1	0.50	1.55	1.50
E	1.75	1.75	1.75
F	3.50	5.50	5.50
P_0	4.00	4.00	4.00
P_1	4.00	8.00	8.00
P_2	2.00	2.00	2.00
W	8.00	12.00	12.00
Pin 1 Quadrant	Q1	Q2	Q2



NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 15.8: Reel Specification

Table 15.5: Reel Dimensions [mm]

Dimension	Package		
	WLCSP18	QFN20 (QFR)	QFN20 (QNR)
A	179	178	180
N	55	60	60
W_1	8.4	12.4	12.4
W_2 (Max)	14.4	18.4	18.4

15.8 Moisture Sensitivity Levels

Table 15.6: Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

15.9 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Please note: The value of all Read-write bits marked as Reserved, unless otherwise specified, can be set to 0 or 1 depending on customer's preference.

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Catergory	Name	Value		Order Code	
0x00	Application Version Info	Product Number	863			16-bit value
0x01		Major Version	1	2		
0x02		Minor Version	13		001	
				6	101/102[i]	
				23	101/102[i]	
				27	101/102[i]	
				32	201[ii]	
				33	202[ii]	
0x03		Patch Number (commit hash)	Reserved			
0x04						
0x05	ROM Library Version Info	Library Number	Reserved			
0x06		Major Version	Reserved			
0x07		Minor Version	Reserved			
0x08		Patch Number (commit hash)	Reserved			
0x09						

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	NP up-date	Power mode		Reset	Res	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global Halt not active
  - 1: Global Halt active
- Bit 6: **Normal Power Update**
  - 0: No Normal Power Update occured
  - 1: Normal Power update occured
- Bit 4-5: **Current Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.3: Events

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Event	ATI Event	Reserved										Touch Event	Prox Event

- Bit 13: **Power Event**
  - 0: No Power Event occurred

[i] Please refer to PCN-PR560-IQS7222C Product Change Note v2.2
[ii] Please refer to product information notice PIN-230172 for more details

- 1: Power Event occurred

- Bit 12: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

Table A.4: Proximity Event States

Register: 0x12

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Prox Event**
  - 0: No prox event occurred on channel
  - 1: Prox event occurred on channel

Table A.5: Touch Event States

Register: 0x13

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.6: Cycle Setup 0

Register: 0x8000, 0x8100, 0x8200, 0x8300, 0x8400

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 8-15: **Conversion Frequency Period**
  - Range: 0 - 127
- Bit 0-7: **Conversion Frequency Fraction**
  - Fix to 127

It is recommended to fix the *Fraction* value to 127. For capacitive sensing, please refer to the following table to determine the *Period* value for the desired conversion frequency. The *Dead Time* setting must be enabled.

Table A.7: Supported Conversion Frequency Parameters for Capacitive Sensing

FRACTION	PERIOD	Conversion Frequency f_{xfer}
127	2	1.75 MHz
	3	1.40 MHz
	5	1.00 MHz
	7	778 kHz
	12	500 kHz
	16	389 kHz
	23	280 kHz

* The maximum recommended conversion frequency for self-capacitive sensing is 1 MHz. The maximum recommended conversion frequency for mutual-capacitive sensing is 2 MHz.

For inductive sensing, please refer to the following table to determine the *Period* value for the desired conversion frequency. The *Dead Time* setting must be disabled.

Table A.8: Supported Conversion Frequency Parameters for Inductive Sensing

FRACTION	PERIOD	Conversion Frequency f_{xfer}
127	0	7.00 MHz
	1	3.50 MHz
	2	2.33 MHz
	3	1.75 MHz
	4	1.40 MHz
	6	1.00 MHz
	8	778 kHz
	13	500 kHz

Table A.9: Cycle Setup 1

Register: 0x8001, 0x8101, 0x8201, 0x8301, 0x8401

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1	CTX0	Ground inactive Rxs	Dead time enabled	FOSC TX Freq	Vbias enable	PXS Mode		

- Bit 15: **CTx8**
  - 0: CTx8 disabled
  - 1: CTx8 enabled
- Bit 14: **CTx7**
  - 0: CTx7 disabled
  - 1: CTx7 enabled
- Bit 13: **CTx6**
  - 0: CTx6 disabled
  - 1: CTx6 enabled
- Bit 12: **CTx5**
  - 0: CTx5 disabled
  - 1: CTx5 enabled
- Bit 11: **CTx4**
  - 0: CTx4 disabled
  - 1: CTx4 enabled
- Bit 10: **CTx3**
  - 0: CTx3 disabled
  - 1: CTx3 enabled
- Bit 9: **CTx2**
  - 0: CTx2 disabled
  - 1: CTx2 enabled
- Bit 8: **CTx1**
  - 0: CTx1 disabled
  - 1: CTx1 enabled
- Bit 7: **CTx0**
  - 0: CTx0 disabled
  - 1: CTx0 enabled
- Bit 6: **Ground Inactive Rx's**
  - 0: Inactive Rx floating
  - 1: Inactive Rx Grounded
- Bit 5: **Dead Time Enabled**
  - Functionality used to avoid transient effect.
  - 0: Deadtime disabled
  - 1: Deadtime enabled

- Bit 4: **FOSC TX Frequency**
  - 0: Disabled - Tx frequency set to the value of charge transfer frequency selected with the combination of charge transfer frequency fractio and period values
  - 1: Enabled - Tx frequency set to the value of F_{OSC}
- Bit 3: **Vbias Enabled**
  - Creates a constant voltage output on Tx8 to offset input voltage.
  - Enable in biased resonant inductive sensing if the voltage swing on the selected CRx is small.
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-2: **PXS Mode**
  - 000: None
  - 001: Self-capacitive
  - 010: Mutual capacitive[i]
  - 011: Mutual inductance

Table A.10: Cycle Setup 2

Register: 0x8002, 0x8102, 0x8202, 0x8302, 0x8402

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved					Current Reference Enable	Current Reference Output		Current Reference Level				Current Reference Trim			

- Bit 10: **Current Reference Enable**
  - 0: Disable current reference
  - 1: Enable current reference
- Bit 8-9: **Current Reference Output**
  - 00: Disabled
  - 10: Self-inductance to pads
- Bit 4-7: **Current Reference Level**
  - 4 bit value to scale current output
  - Higher values will result in a higher output current
- Bit 0-3: **Current Reference Trim**
  - 4 bit value to adjust current supply output
  - Higher values will result in a higher output current

Table A.11: Global Cycle Setup

Register: 0x8500

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	Maximum counts		0	1	0	1	1	1	1	0	0	Auto Mode		1	1

- Bit 13-14: **Maximum counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16383
- Bit 2-3: **Auto Mode Update**
  - Number of conversions created before each interrupt is generated
  - 00: 4
  - 01: 8
  - 10: 16
  - 11: 32

Table A.12: Coarse and Fine Multipliers Preload

Register: 0x8501

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Divider Preload					Reserved				Coarse Divider Preload				

[i] Please note that the maximum allowed charge transfer frequency (see Table A.6) for mutual capacitive mode is 1MHz i.e frequency period ≥ 5

- Bit 0-4: **Coarse Divider Preload**
  - 5-bit coarse divider preload value
- Bit 9-13: **Fine Divider Preload**
  - 5-bit fine divider preload value

Table A.13: ATI Compensation Preload

Register: 0x8502

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						ATI Compensation Preload									

- Bit 0-9: **ATI Compensation Preload**
  - 10-bit preload value

Table A.14: Button Setup 0

Register: 0x9000, 0x9100, 0x9200, 0x9300, 0x9400, 0x9500, 0x9600, 0x9700, 0x9800, 0x9900

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit				Enter				Proximity Threshold							

- Bit 12-15: **Exit Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 8-11: **Enter Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 0-6: **Proximity Threshold**
  - 7-bit value

Table A.15: Button Setup 1

Register: 0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501, 0x9601, 0x9701, 0x9801, 0x9901

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 8-15: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
  - $\frac{\text{LTA} * \text{Threshold bit value}}{2^8} - \frac{\text{Threshold bit value} * \text{Hysteresis bit value} * \text{LTA}}{2^{16}}$
- Bit 0-7: **Touch Threshold**
  - $\frac{LTA}{256} * 8\text{bit value}$

Table A.16: Button Setup 2

Register: 0x9002, 0x9101, 0x9202, 0x9302, 0x9402, 0x9502, 0x9602, 0x9702, 0x9802, 0x9902

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Event Timeout								Prox Event Timeout							

- Bit 8-15: **Touch Event Timeout**
  - 8-bit value * 500ms where a reseed of the LTA is forced. If the LTA is outside of the LTA ATI band a re-ATI event will occur if ATI is not disabled
  - 0: Never timeout (recommended for use with follower and reference channels)
- Bit 0-7: **Prox Event Timeout**
  - 8-bit value * 500ms where a reseed of the LTA is forced. If the LTA is outside of the LTA ATI band a re-ATI event will occur if ATI is not disabled
  - 0: Never timeout (recommended for use with follower and reference channels)

Table A.17: CRX Select and General Channel Setup(CH0-CH4)

Register: 0xA000, 0xA100, 0xA200, 0xA300, 0xA400

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode		ATI Band		Global halt	Invert	Dual	Enabled	CRX3	CRX2	CRX1	CRX0	Cs Size	Vref 0.5V	Proj Bias Select	

- Bit 14-15: **Channel Mode**
  - 00: Independent
  - 01: Reference
  - 10: Follower
- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a prox/touch state. The function is aimed at slider/ wheel applications
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional sensing**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx3**
  - 0: CRx3 disabled
  - 1: CRx3 enabled
- Bit 6: **CRx2**
  - 0: CRx2 disabled
  - 1: CRx2 enabled
- Bit 5: **CRx1**
  - 0: CRx1 disabled
  - 1: CRx1 enabled
- Bit 4: **CRx0**
  - 0: CRx0 disabled
  - 1: CRx0 enabled
- Bit 3: **Cs Size**
  - 0: 40pF - use when external load is very small
  - 1: 80pF
- Bit 2: **Vref 0.5V Enable**
  - Decrease internal sampling capacitor size
  - 0: Vref 0.5V disabled - C_s = Value chosen in Cs 80pF bit (40pF/80pF)
  - 1: Vref 0.5V enabled - C_s = Half of the value chosen in Cs 80pF bit (40pF/80pF)
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.18: CRX Select and General Channel Setup(CH5-CH9)

Register: 0xA500, 0xA600, 0xA700, 0xA800, 0xA900

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mode		ATI Band		Global halt	Invert	Dual	Enabled	CRX7	CRX6	CRX5	CRX4	Cs 80pF	Vref 0.5V	Proj Bias Select	

- Bit 14-15: **Mode**
  - 00: Independent
  - 01: Reference
  - 10: Follower

- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with global halt enabled, is in a prox/touch state. The function is aimed at slider/ wheel applications
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional Sensing**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx7**
  - 0: CRx7 disabled
  - 1: CRx7 enabled
- Bit 6: **CRx6**
  - 0: CRx6 disabled
  - 1: CRx6 enabled
- Bit 5: **CRx5**
  - 0: CRx5 disabled
  - 1: CRx5 enabled
- Bit 4: **CRx4**
  - 0: CRx4 disabled
  - 1: CRx4 enabled
- Bit 3: **Cs Size**
  - 0: 40pF - use when external load is very small
  - 1: 80pF
- Bit 2: **Vref 0.5V Enable**
  - Decrease internal sampling capacitor size
  - 0: Vref 0.5V disabled - C_s = Value chosen in Cs 80pF bit (40pF/80pF)
  - 1: Vref 0.5V enabled - C_s = Half of the value chosen in Cs 80pF bit (40pF/80pF)
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.19: ATI Base and Target

Register: 0xA001, 0xA101, 0xA201, 0xA301, 0xA401, 0xA501, 0xA601, 0xA701, 0xA801, 0xA901

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target								ATI Base					ATI Mode		

- Bit 8-15: **ATI Target**
  - 8-bit value * 8
- Bit 3-7: **ATI Base**
  - 5-bit value * 16
- Bit 0-2: **ATI Mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider

- 100: ATI from coarse fractional divider
- 101: Full ATI

Table A.20: Fine and Coarse Multipliers

Register:	0xA002, 0xA102, 0xA202, 0xA302, 0xA402, 0xA502, 0xA602, 0xA702, 0xA802, 0xA902														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.21: ATI Compensation

Register:	0xA003, 0xA103, 0xA203, 0xA303, 0xA403, 0xA503, 0xA603, 0xA703, 0xA803, 0xA903														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.22: Reference Channel Settings 0

Register:	0xA004, 0xA104, 0xA204, 0xA304, 0xA404, 0xA504, 0xA604, 0xA704, 0xA804, 0xA904														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reference Follower Mask Pointer/ Sensor Mask															

- Please note that the register value is used for either Follower Mask Link Ptr or Reference Sensor Ptr based on the mode selected in Table A.17 / A.18, bit 14-15
- **Reference Follower Mask Pointer** - Mode = Reference
  - 0x694 (decimal = 1684): Prox
  - 0x696 (decimal = 1686): Touch
- **Sensor Mask** - Mode = Follower
  - 0x000 (decimal = 0): None
  - 0x418 (decimal = 1048): Channel 0
  - 0x442 (decimal = 1090): Channel 1
  - 0x46C (decimal = 1132): Channel 2
  - 0x496 (decimal = 1174): Channel 3
  - 0x4C0 (decimal = 1216): Channel 4
  - 0x4EA (decimal = 1258): Channel 5
  - 0x514 (decimal = 1300): Channel 6
  - 0x53E (decimal = 1342): Channel 7
  - 0x568 (decimal = 1384): Channel 8
  - 0x592 (decimal = 1426): Channel 9

Table A.23: Reference Channel Settings 1

Register:	0xA005, 0xA105, 0xA205, 0xA305, 0xA405, 0xA505, 0xA605, 0xA705, 0xA805, 0xA905														
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reference Follower Mask/ Reference Weight															

- Please note that the register value is used for either Follower Mask or Reference Weight based on the mode selected in Table A.17 / A.18, bit 14-15
- **Reference Follower Mask** (used to enable current sensor as a reference channel for the selected channel) - Mode = Reference
  - 0: Disabled

- 1: Channel enabled as reference for Channel 0
- 2: Channel enabled as reference for Channel 1 enabled
- 4: Channel enabled as reference for Channel 2 enabled
- 8: Channel enabled as reference for Channel 3 enabled
- 16: Channel enabled as reference for Channel 4 enabled
- 32: Channel enabled as reference for Channel 5 enabled
- 64: Channel enabled as reference for Channel 6 enabled
- 128: Channel enabled as reference for Channel 7 enabled
- 256: Channel enabled as reference for Channel 8 enabled
- 512: Channel enabled as reference for Channel 9 enabled

› **Reference Weight** - Mode = Follower
- 16-bit decimal value/256

Table A.24: Filter Betas

Register: 0xAA00

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Low Power Beta				LTA Normal Power Beta				Counts Low Power Beta				Counts Normal Power Beta			

› Bit 12-15: **LTA Low Power Beta Filter Value**
- 4-bit value

› Bit 8-11: **LTA Normal Power Beta Filter Value**
- 4-bit value

› Bit 4-7: **Counts Low Power Beta Filter Value**
- 4-bit value

› Bit 0-3: **Counts Normal Power Beta Filter Value**
- 4-bit value

Table A.25: Fast Filter Betas

Register: 0xAA01

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

› Bit 4-7: **LTA Low Power Fast Beta Filter Value**
- 4-bit value

› Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
- 4-bit value

Table A.26: Slider Setup and Calibration

Register: 0xB000, 0xB100

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Lower Calibration								Static Filter	Slow/Static Beta			Wheel Enable	Total Channels		

› Bit 8-15: **Lower Calibration**
- 8-bit value

› Bit 7: **Static Filter**
- 0: Static filter disabled
- 1: Static filter enabled

› Bit 4-6: **Slow/Static Beta**
- 3-bit value

› Bit 3: **Wheel Enable**
- 0: Wheel disabled
- 1: Wheel enabled

› Bit 0-2: **Total Channels**
- 0010: 2 Channels
- 0011: 3 Channels
- 0100: 4 Channels
- Else: Disabled

Table A.27: Slider Calibration and Bottom Speed

Register: 0xB001, 0xB101

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bottom FIlter Speed								Upper Calibration							

- Bit 8-15: **Bottom Filter Speed**
  - 8-bit value
- Bit 0-7: **Upper Calibration**
  - 8-bit value

Table A.28: Slider Enable Mask

Register: 0xB004, 0xB104

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Please note that all channels in use must be selected
- Bit 0-9: **Slider Channel Enable Mask**
  - 0: Disabled
  - 1: Channel 0 enabled for slider
  - 2: Channel 1 enabled for slider
  - 4: Channel 2 enabled for slider
  - 8: Channel 3 enabled for slider
  - 16: Channel 4 enabled for slider
  - 32: Channel 5 enabled for slider
  - 64: Channel 6 enabled for slider
  - 128: Channel 7 enabled for slider
  - 256: Channel 8 enabled as output
  - 512: Channel 9 enabled as output

Table A.29: Slider Enable Status Link

Register: 0xB005, 0xB105

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable Status Link															

- Bit 0-15: **Enable Status Link**
  - 0x694 (decimal = 1684): Output linked to channel prox
  - 0x696 (decimal = 1686): Output linked to channel touch

Table A.30: Delta Link

Register: 0xB006, 0xB007, 0xB008, 0xB009, 0xB106, 0xB107, 0xB108, 0xB109

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Delta Link															

- Bit 0-15: **Delta Link** - Select element order per channel
- Delta link number corresponds with slider element order
  - 0x000 (decimal = 0): Disabled
  - 0x438 (decimal = 1080): Channel 0 enabled for element
  - 0x462 (decimal = 1122): Channel 1 enabled for element
  - 0x48C (decimal = 1164): Channel 2 enabled for element
  - 0x4B6 (decimal = 1206): Channel 3 enabled for element
  - 0x4E0 (decimal = 1248): Channel 4 enabled for element
  - 0x50A (decimal = 1290): Channel 5 enabled for element
  - 0x534 (decimal = 1332): Channel 6 enabled for element
  - 0x55E (decimal = 1374): Channel 7 enabled for element
  - 0x588 (decimal = 1416): Channel 8 enabled for element
  - 0x5B2 (decimal = 1458): Channel 9 enabled for element

Table A.31: Output X Control[ii]

Register: 0xC000, 0xC100, 0xC200

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								0	OUTC	OUTB	0	0	OUTA	Output Con-figura-tion	Enable

- Bit 6: **OUTC**
  - 0: OUTC not linked to output
  - 1: OUTC linked to output
- Bit 5: **OUTB**
  - 0: OUTB not linked to output
  - 1: OUTB linked to output
- Bit 2: **OUTA**
  - 0: OUTA not linked to output
  - 1: OUTA linked to output
- Bit 1: **Output Configuration**
  - 0: Push-Pull active high logic
  - 1: Open-Drain active low logic (requires additional pull-up resistance to VDD level, no internal pull-up)
- Bit 0: **Enable**
  - 0: GPIO Output disabled
  - 1: GPIO Output enabled

Table A.32: Output X Enable Mask

Register: 0xC001, 0xC101, 0xC201

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Please note that more than one channel can be selected as an output
- Bit 0-7: **Channel Enable Mask**
  - 0: Disabled
  - 1: Channel 0 enabled as output
  - 2: Channel 1 enabled as output
  - 4: Channel 2 enabled as output
  - 8: Channel 3 enabled as output
  - 16: Channel 4 enabled as output
  - 32: Channel 5 enabled as output
  - 64: Channel 6 enabled as output
  - 128: Channel 7 enabled as output
- Bit 8-9: **Channel Enable Mask**
  - 256: Channel 8 enabled as output
  - 512: Channel 9 enabled as output

Table A.33: Output X Status Link

Register: 0xC002, 0xC102, 0xC202

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enable Status Link															

- Bit 0-15: **Enable Status Link**
  - 0x694 (decimal = 1684): Output linked to channel prox
  - 0x696 (decimal = 1686): Output linked to channel touch
  - 0x6A4 (decimal = 1700): Direct output (Use register 0xDB (See Table A.37) to directly override the GPIO output state for the instance of CH0, CH1 or CH2)

[ii] OUTA and OUTB should not be used at the same time on the WLCSP18 package.

Table A.34: Control Settings

Register: 0xD0

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Interface type		Power mode		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 6-7: **Interface Selection**
  - 00: I²C streaming
  - 01: I²C event mode
  - 10: I²C Stream in touch
- Bit 4-5: **Power Mode Selection**
  - 00: Normal power
  - 01: Low power
  - 10: Ultra-low Power
  - 11: Automatic power mode switching
- Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
- Bit 2: **Execute ATI Command**
  - 0: Do not ATI
  - 1: ATI
- Bit 1: **Soft Reset**
  - 0: Do not reset device
  - 1: Reset device after communication window terminates
- Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

Table A.35: Event Enable

Register: 0xD9

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power event	ATI event	Reserved										Touch event	Prox event

- Bit 13: **Power Event**
  - 0: Power event masked
  - 1: Power event enabled
- Bit 12: **ATI Event**
  - 0: ATI event masked
  - 1: ATI event enabled
- Bit 1: **Touch Event**
  - 0: Touch event masked
  - 1: Touch event enabled
- Bit 0: **Prox Event**
  - 0: Prox event masked
  - 1: Prox event enabled

Table A.36: I²C Communication

Register: 0xDA

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														RW check disabled	Stop bit disabled

- Bit 1: **RW Check Disabled**
  - 0: Write not allowed to read only registers
  - 1: Read and write allowed to read only registers
- Bit 0: **Stop Bit Disabled**
  - 0: I²C communication window terminated by stop bit.
  - 1: I²C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window

Table A.37: GPIO Direct Output Control

Register:		0xDB													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved													CH2	CH1	CH0

- Note: To write to this register, the register's address (0xDB) must be commanded explicitly before writing data i.e. in a separate I^2C write setup command.
- Bit 2: **CH2**
  - 0: Channel 2 direct output state inactive
  - 1: Channel 2 direct output state active
- Bit 1: **CH1**
  - 0: Channel 1 direct output state inactive
  - 1: Channel 1 direct output state active
- Bit 0: **CH0**
  - 0: Channel 0 direct output state inactive
  - 1: Channel 0 direct output state active
- Note: To use direct outputs
  - Output must be enabled as "Direct".
  - The corresponding channel "CHx" in the Channel Enable Mask register (refer to Table A.32) must be enabled. E.g. For output 2, CH2 must be selected.
  - The corresponding GPIO override bit, "CHx" must be enabled. E.g. For output 2, the CH2 bit under "GPIO Direct Output Control" must be enabled.

Table A.38: I^2C Communication Timeout

Register:		0xDC													
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I^2C Communication Timeout															

- Note: To write to this register, the register's address (0xDC) must be commanded explicitly before writing data i.e. in a separate I^2C write setup command.
- Bit 0-15: **I^2C Communication Timeout**
  - 16-bit value [ms]
  - Range: 0 - 65535
  - Default = 500 ms

B Known Issues

B.1 I²C Polling During Start-up

V2.23 and earlier

Polling during start-up may result in device lockup. Suspend polling for at least 25ms after receiving a NACK.

The I²C initialize can fail if one of the I²C lines have been kept low for longer than 50ms.

B.2 ATI Power Mode Issue

- When signal drift is present in a low-power mode, an auto-ATI event is possible to ensure the signal is in an optimal operating range.
- An auto-ATI event will wake the IC from LP or ULP mode, causing it to spend the preset times to step down to low power modes again. In cases where significant signal drift is expected, this effect could affect battery life calculations.
- For optimal battery life it is recommended to use the ATI events to manually put the IC back into the lowest power mode and reinstate auto power modes after that. Please contact Azoteq for sample code to achieve this.

B.3 Force Communication Request may Close a Communication Window

A force communication request (0xFF command) may unintentionally close a communication window instead of opening it. This occurs if the IQS7222C receives the force communication request while the RDY is low. The I²C STOP condition at the end of the 0xFF byte triggers the IQS7222C to close its communication window, causing the RDY to go back high immediately. This may also happen if the communication window automatically opens during the transmission of the 0xFF byte, as shown in Figure B.1.

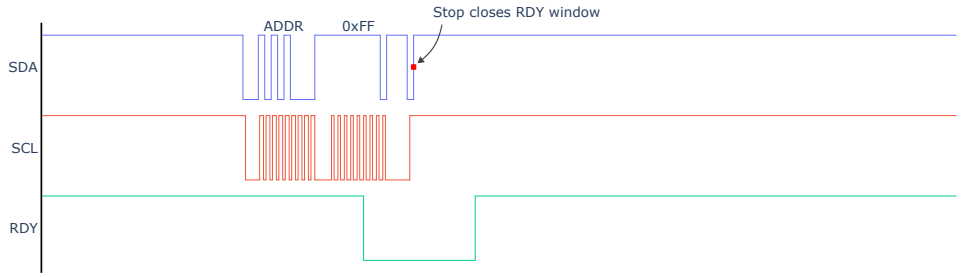


Figure B.1: Force Communication Closing a Communication Window

As a result, the MCU may observe the RDY pin change, and then attempt to communicate with the IC as soon as the force communication transaction is complete. This will cause the IQS7222C to respond with the error code 0xEE.

The following protocol can be used to minimise the likelihood of this error condition.

Step 1: Before sending the 0xFF command, read the state of the RDY pin and verify that it is high (the communication window is closed). If the RDY pin is already low, the communications window is open and can be handled as normal.

Step 2: If the RDY pin is high, issue the force communication I²C command.

Step 3: As soon as the I²C transmission of the force communication command has started, wait for the RDY window.

Step 4: Once the RDY is received, the MCU should wait at least 300 µs, then re-check the state of the RDY pin.

(a) If the RDY pin is high, then the window was closed due to the STOP condition. Re-issue the 0xFF command, repeating the above procedure.

(b) If the RDY pin is low, the communication window is still open, and normal I²C operations may resume.

Figure B.2 shows an example of this process. The first force communication request occurred simultaneously with a RDY window, and the RDY window was closed due to the STOP condition. The MCU detected the RDY window, waited 300 µs, then checked the RDY pin state. The pin was HIGH, and the force communication request was repeated.

The second request opened the RDY window after some time, and the MCU waited 300 µs again before checking the RDY pin state. The RDY was low, and normal communication could continue.

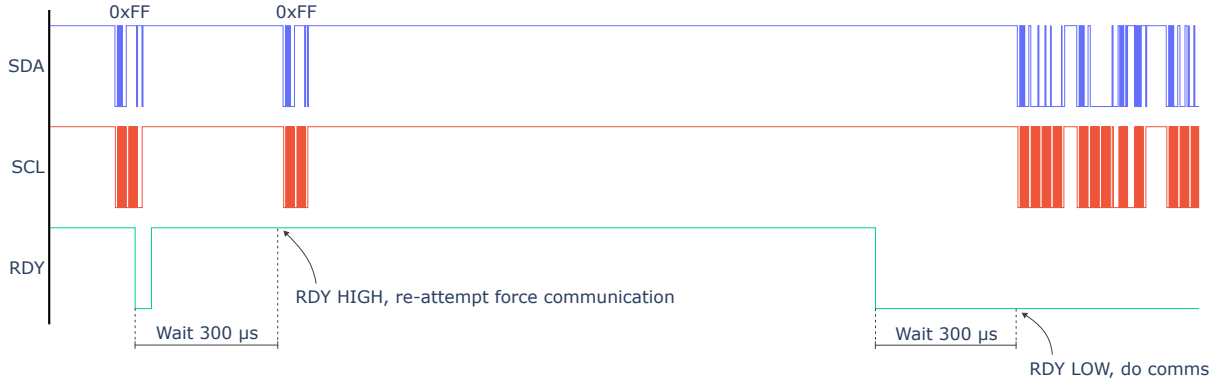


Figure B.2: Force Communication With RDY Check

B.4 Force Communication Request May Be Missed

There is a possibility of a force communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period (described in Section 10.8.2). However, it is essential to retry at different timings that are not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional recovery mechanism, the IC can be reset using the MCLR pin and reinitialised if there is no response after a specified number of retries.

C Revision History

Release	Date	Changes
v1.0	July 2021	› Initial release
v1.1	July 2021	› Filter beta bit definition corrected
v1.2	August 2021	› Reference schematics updated to include 3 GPIO's › Extra GPIO registers and descriptions add › Order code 101 and 102 added › Tape and Reel information added › Slider and wheel combinations added › Firmware version changed to v2.6 › Bit definition for Read-write check corrected
v1.3	November 2021	› Changed Communication protocol description › Read-write permissions added in memory map › Stop-bit disable bit definition corrected › Revision history added › Force communication section added › Register 0xDC added › VREG minimum and maximum values added › Firmware version changed to v2.23 › Changes implemented for IQS7222C 101 and 102 IC options according to "PCN-PR560-IQS7222C Product Change note v0.1"
v1.4	December 2021	› Firmware version changed to v2.27. › Appendix C, known issues added › Changes implemented for IQS7222C 101 and 102 IC options according to "PCN-PR560-IQS7222C Product Change note v1.0"
v1.5	January 2022	› Information regarding h files added › Added program flow diagram
v1.6	June 2022	› Added watchdog timer › Minor format and spelling errors addressed › Frontpage package dimension update › Description of Direct Output GPIO function added › Package description and dimension updated › Schematics updated to match VREG capacitor recommendations
v1.7	June 2022	› Update QFN20 pin diagram to show TAB pad.
v1.8	August 2022	› Minor formatting and grammar changes
v1.9	November 2022	› QF package type added to ordering code › Update to package outline description of QFN20 (QFR & QNR) › Update to package outline description of WLCSP18

v1.10	May 2023	› Firmware version updated to v2.32/v2.33 › Added order codes 201 & 202 › Changes implemented for IQS7222C 201/202 IC options according to "PIN-230172" › Updated current consumption tables › Updated channel options section › Updated addressing information for order code 202 › Updated power mode and mode timeout section › Update Memory Map version information table › Memory Map reserved bits corrected › Updated force communication “t_{wait}” description › Updated Output pin naming
v1.11	July 2023	› Updated force communication description › Memory Map reserved bits corrected › Added a warning for the use of GPIO0 and GPIO3 at the same time as an output on the WLCSP18 package
v1.12	May 2024	› Updated QNR package outline drawing. › Added recommended footprints for all IC packages.
v1.13	May 2024	› Added footnote in electrical characteristics table regarding VREG capacitor derating
v1.14	August 2024	› Added power-on timing characteristics
v1.15	June 2026	› Overhauled ProxFusion Module section, expanding descriptions and including a list of all relevant settings › Re-ordered I^2C Interface section › Added recommended Conversion Frequency settings to Memory Map Descriptions › Updated Tape and Reel dimensions to include additional dimensions › Removed GPIOx designators in pinout › Added default values to memory map registers › Added known issue regarding power mode changes after ATI › Added known issues regarding I^2C force communication › Removed “ATI Active” from Program Flow Diagram › Added GPIO Output section

Contact Information

	South Africa (Headquarters)	China
Physical Address	1 Bergsig Avenue Paarl 7646 South Africa	Room 501A, Block A T-Share International Centre Taoyuan Road, Nanshan District Shenzhen, Guangdong, PRC
Tel	+27 21 863 0033	+86 755 8303 5294 ext 808
Email	info@azoteq.com	info@azoteq.com

	USA	Taiwan
Physical Address	7000 North Mopac Expressway Suite 200 Austin TX 78731 USA	Xintai 5th Road, Sec. 1 No. 99, 9F-12C Xizhi District 221416 New Taipei City Taiwan
Tel	+1 512 538 1995	+886 932 219 444
Email	info@azoteq.com	info@azoteq.com

Visit www.azoteq.com
for a list of distributors and worldwide representation.

Patents as listed on www.azoteq.com/patents-trademarks/ may relate to the device or usage of the device.