IQS7222B DATASHEET

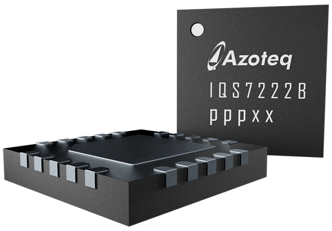
20 Channel Mutual / 8 Channel Self- Capacitive Touch and Proximity Controller with I^{2}C communications interface and low power options

1 Device Overview

The IQS7222B ProxFusion® IC is a sensor fusion device for various multi-button applications. The sensor is fully I^{2}C compatible and on-chip calculations enable the IC to respond effectively even in lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) / 8 (WLCSP)external sensor pad connections
- Configure up to 20 Mutual capacitive buttons, 18 mutual capacitance buttons with proximity wake-up function or up to 8 self-capacitance buttons[i]
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Debounce & hysteresis
  - Dual direction trigger indication
- Design simplicity
  - PC Software for debugging and obtaining optimal settings and performance
  - One-time programmable settings for custom power-on IC configuration
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I^{2}C communication interface with IRQ/RDY(up to fast plus -1 MHz)
- Event and streaming modes
- Customizable user interface due to programmable memory
- Small packages
  - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4 mm x 0.6 mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4 mm pitch



QFN20 Package

WLCSP18 Package

1.2 Applications

- Multi-button keypads or user interfaces.
- Low power wake-up on proximity or touch.

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[i] WLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured is 18 buttons or 16 buttons with a wake-up function.

1.3 Block Diagram

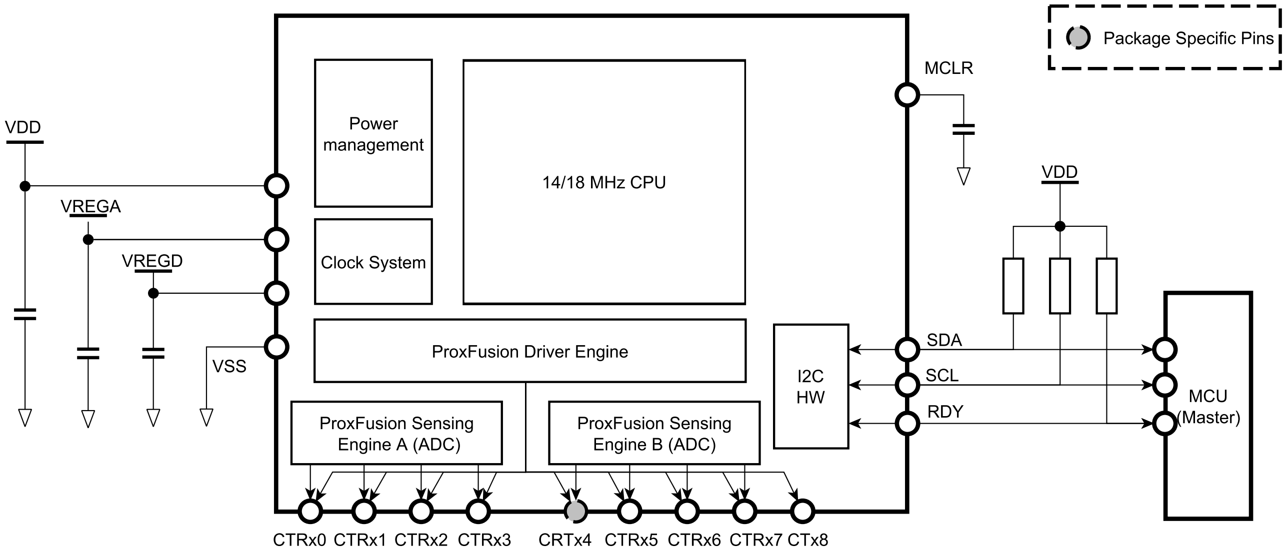

Figure 1.3: Functional Block Diagramgit

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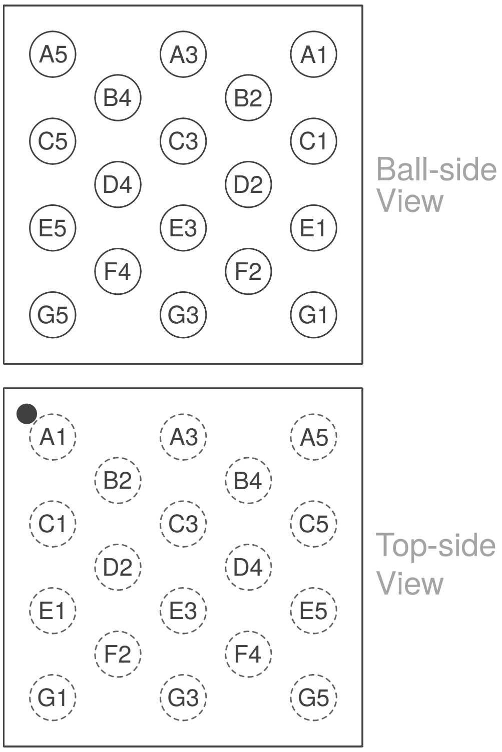
2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

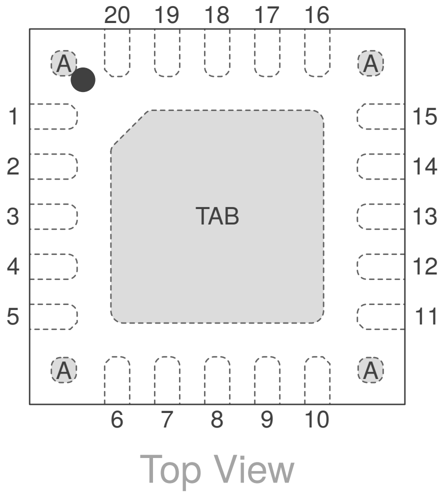
Table 2.1: 18-pin WLCSP18 Package



Pin no.	Signal
A1	NC
A3	SCL
A5	MCLR
B2	NC
B4	SDA
C1	CTx8
C3	RDY
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CRx6/CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CRx5/CTx5
F4	CRx0/CTx0
G1	CRx7/CTx7
G3	CRx3/CTx3
G5	VREGA

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8
4	VREGA	14	NC
5	CRx0/CTx0	15	NC
6	CRx1/CTx1	16	NC
7	CRx2/CTx2	17	RDY
8	CRx3/CTx3	18	SCL
9	CRx4/CTx4	19	SDA
10	CRx5/CTx5	20	MCLR

Area name	Signal name
TAB[i]	Thermal pad (floating)
A[ii]	Thermal pad (floating)

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[i] It is recommended to connect the thermal pad (TAB) to VSS.

[ii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
-	14	NC	-		-
B4	19	SDA	Digital		VDD
A3	18	SCL	Digital		VDD
A1	15	NC	-		-
B2	16	NC	-		-
C3	17	RDY	Digital		VDD
A5	20	MCLR	Digital		VDD

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iii]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CRx4/CTx4	-	9	IO	
	CRx5/CTx5	F2	10	IO	
	CRx6/CTx6	E1	11	IO	
	CRx7/CTx7	G1	12	IO	
	CTx8	C1	13	O	CTx8 pad
GPIO	NC	-	14	-	Not Connected
	NC	A1	15	-	Not Connected
	NC	B2	16	-	Not Connected
	RDY	C3	17	O	RDY pad
	MCLR	A5	20	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^{2}C	SDA	B4	19	IO	I^{2}C data
	SCL	A3	18	IO	I^{2}C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

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[iii] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.5 Reference Schematic

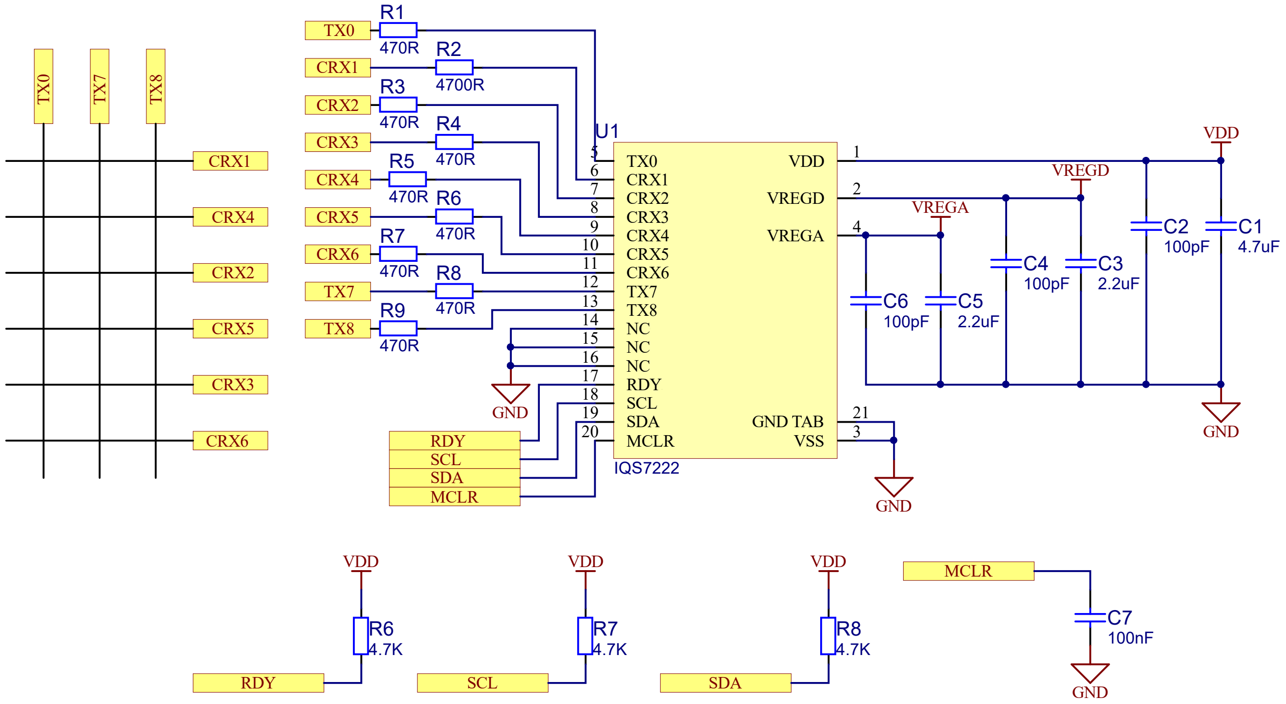

Figure 2.1: 18 Button Mutual Capacitance Reference Schematic

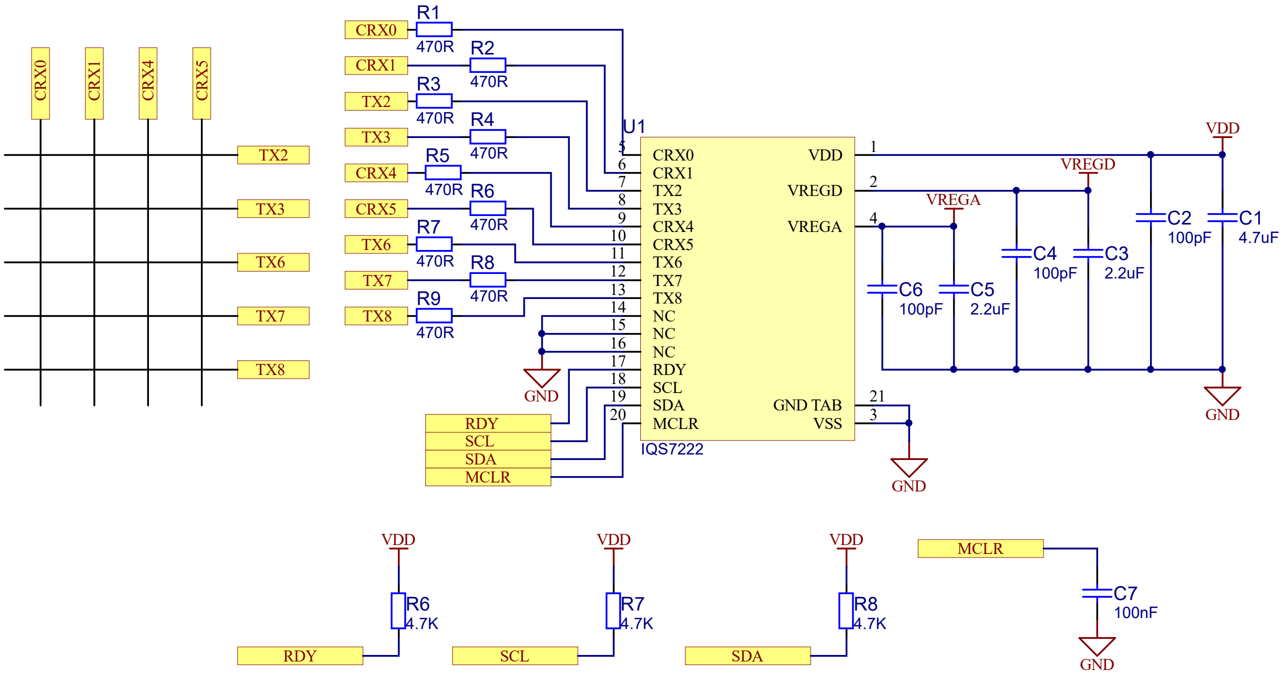

Figure 2.2: 20 Button Mutual Capacitance Reference Schematic

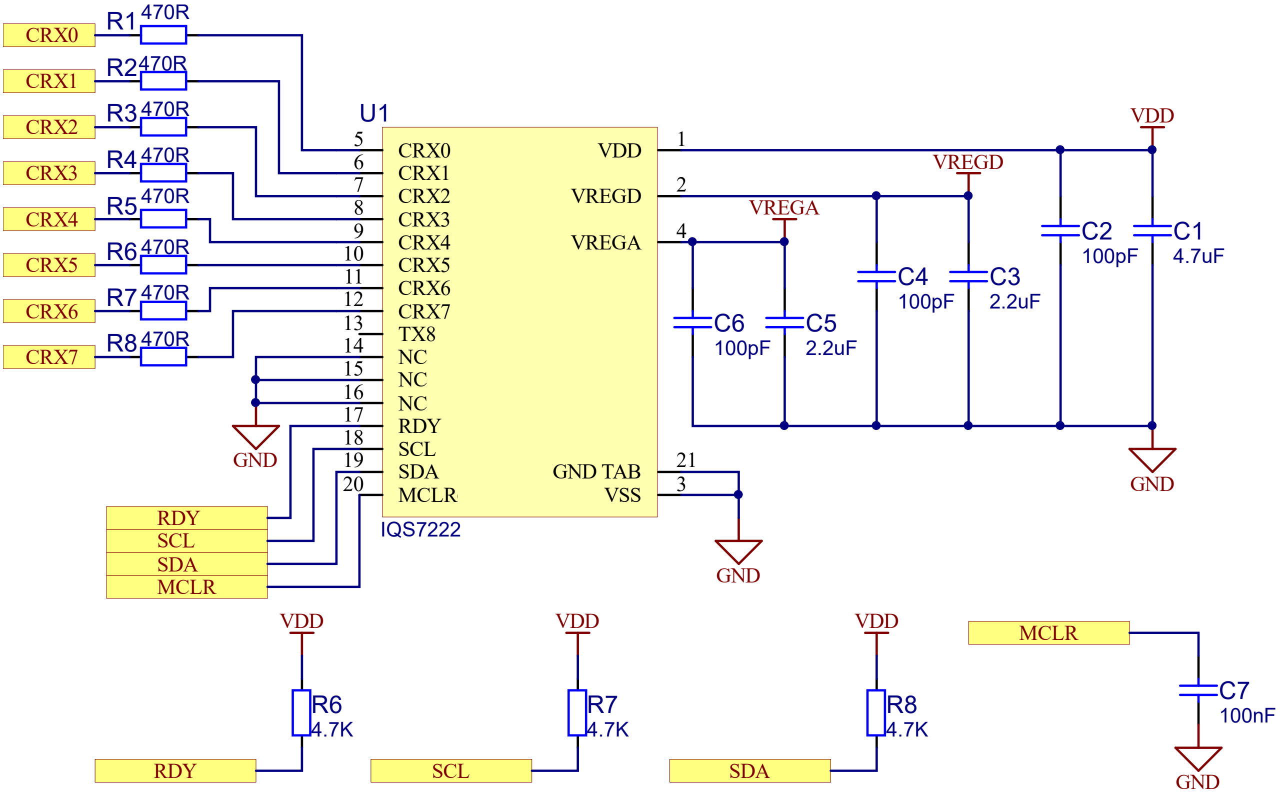

Figure 2.3: 8 Button Self Capacitance Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	−0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	−0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	−40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: f_{OSC} = 14 MHz f_{OSC} = 18 MHz	 1.71 2.2		 3.6 3.6	V
VREGA	Internal regulated supply output for analog domain: f_{OSC} = 14 MHz f_{OSC} = 18 MHz	 1.49 1.49	 1.53 1.53	 1.57 1.57	V
VREGD	Internal regulated supply output for digital domain: f_{OSC} = 14 MHz f_{OSC} = 18 MHz	 1.56 1.75	 1.59 1.8	 1.64 1.85	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	−40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREGA}$	$3\times C_{VREGA}$		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF-VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{CTx-CRx}$	Capacitance between receiving and transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{CRx-VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode at f_{xfer} = 1 MHz)			100[ii]	pF
$\frac{Cp_{CRx-VSS}}{Cm_{CTx-CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

3.4 Current Consumption

Mutual Capacitive Mode Setup:	Target: CH0 & CH10 = 800, all other channels = 512 @ VDD = 3.3 V
Self-capacitive Mode Setup:	Target = 512, f_{xfer} = 500 kHz @ VDD = 3.3 V
Interface Selection:	Event mode

Table 3.4: Typical Current Consumption for IQS7222B101

Power mode	Active channels	Report rate (Sampling rate) [ms]	Current [µA] Order Code 101
NP	Mutual Capacitance (20 channels)	10	720
	Self-capacitive (8 channels)	10	505
LP	Mutual Capacitance (20 channels)	50	147
	Self-capacitive (8 channels)	50	101
ULP	Wake-up proximity - Distributed mutual channel	100	14.3
	Wake-up proximity - Distributed self channel	100	8.7
	Wake-up proximity - Distributed mutual channel	160	9.8
	Wake-up proximity - Distributed self channel	160	7

Table 3.5: Typical Current Consumption for IQS7222B201/202

Power mode	Active channels	Report rate (Sampling rate) [ms]	Current [µA] Order Code	
			201	202
NP	Mutual Capacitance (20 channels)	16	694	631
	Self-capacitive (8 channels)	16	457	384
LP	Mutual Capacitance (20 channels)	60	180	164
	Self-capacitive (8 channels)	60	117	100
ULP	Wake-up proximity - Distributed mutual channel	100	16.9	15.3
	Wake-up proximity - Distributed self channel	100	17.2	14.4
	Wake-up proximity - Distributed mutual channel	160	12.2	11.0
	Wake-up proximity - Distributed self channel	160	12.4	10.4

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[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.

[ii] RCx = 0 Ω.

[iii] Please note that the maximum values for Cp and Cm are subject to this ratio.

[iv] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

[v] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. $R_{\text{max}} \times C_{\text{max}} = \frac{1}{(6 \times f_{xfer})}$ where C is the pin capacitance to VSS.

[vi] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < −100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS − 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

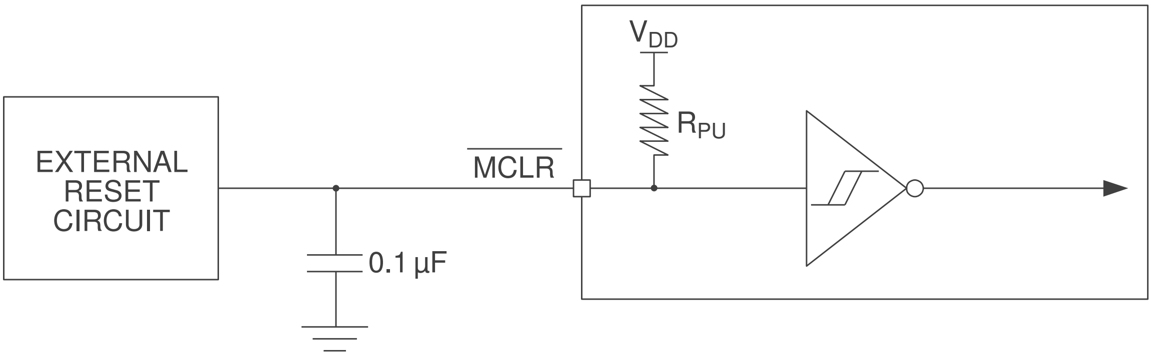


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
f_{OSC}	Master CLK frequency tolerance 18 MHz	17.1	18	19.54	MHz
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	70	500 – 1500	9000	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions[i]	Min	Max	Unit
V_{OL}	Output low voltage of SDA and SCL pins	I_{OL} = 20 mA $V_{DD} > 2$ V		0.4	V
		I_{OL} = 20 mA $V_{DD} \leq 2$ V		0.2 V_{DD}	
	Output low voltage of SDA and SCL pins in GPIO output mode	I_{OL} = 10 mA		0.1 V_{DD}	
	Output low voltage of MCLR	I_{OL} = 5 mA			
	Output low voltage of any other GPIO pin	I_{OL} = 10 mA			
V_{OH}	Output high voltage	I_{OH} = −5 mA	0.9 V_{DD}		V
V_{IL}	Input low voltage		V_{SS} − 0.3	0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}	V_{DD} + 0.3	V
C_b	SDA and SCL bus capacitance			550	pF

[i] Standard operating conditions:
V_{DD}: 1.8 V to 3.6 V, unless otherwise stated.
Operating temperature: −20 °C to 80 °C.

4.5 I^{2}C Characteristics

Table 4.5: I^{2}C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

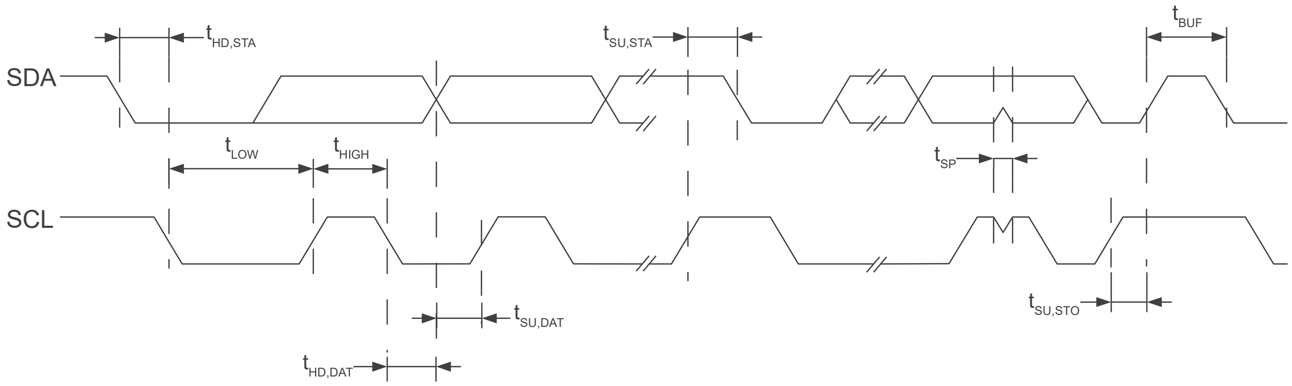


Figure 4.2: I^{2}C Mode Timing Diagram

5 ProxFusion® Module

The IQS7222B contains dual ProxFusion® modules which use patented technology to measure and process relative changes in capacitive and inductive sensors. It supports up to 20 sensing channels. The two modules allow for simultaneous sensing of two channels at a time, ensuring a rapid response from multi-channel implementations. Each channel can detect proximity and touch events.

5.1 Overview

Self-capacitance, mutual capacitance and inductive designs are possible with the IQS7222B.

Please refer to the following application notes for more information:

- AZD004: Azoteq Sensing Technology
- AZD125: Capacitive Sensing Design Guide
- AZD036: Mutual Capacitance Button Layout Guide
- AZD115: Inductive Sensing Design Guide
- AZD137: User Interfaces Application Note

5.2 Counts

Each ProxFusion module reports a sensing measurement as a relative, unit-less value referred to as “Counts”, which are stored as *16-bit values*. These counts report the number of charge transfer cycles necessary to charge an internal sampling capacitor, and are typically inversely proportional to the signal measured on the external sensor. Count values are thus inversely proportional to capacitance/inductance. All further outputs are derived from these counts values.

User interaction is detected by comparing the measured count values to some reference value. The reference value, known as the *Long-Term Average* (LTA), is slowly updated using a low-pass filter to track changes in the environment. Detected proximity and touch events are then reported for each channel in the *Proximity* and *Touch* Event registers.

5.3 Cycle and Channel Relationship

The IQS7222B has 2 Prox engines, A and B, that perform sensing simultaneously. Sensing is performed across 10 time slots, labelled cycle 0 to cycle 9, where each cycle is associated with two channels, one for each Prox engine. The relationship between the cycles and channels is shown in Table 5.1 below.

Table 5.1: Cycle and Channel Relationship

Cycle	Channel on Prox Engine A	Channel on Prox Engine B
Cycle 0	Channel 0	Channel 10
Cycle 1	Channel 1	Channel 11
Cycle 2	Channel 2	Channel 12
Cycle 3	Channel 3	Channel 13
Cycle 4	Channel 4	Channel 14
Cycle 5	Channel 5	Channel 15
Cycle 6	Channel 6	Channel 16
Cycle 7	Channel 7	Channel 17
Cycle 8	Channel 8	Channel 18
Cycle 9	Channel 9	Channel 19

ProxFusion sensing settings can be either channel-specific or cycle-specific (i.e. applies to both channels in the same cycle). It is important to note that both channels of a particular cycle must use the same sensing mode (self-capacitance, inductive, etc). Refer to Section 5.7.1 for a list of cycle-specific settings, and Section 5.7.2 for a list of channel-specific settings.

5.4 ProxFusion Hardware Settings

5.4.1 Sensing Mode

Each channel can be independently enabled via the *Channel Enable* bit of the respective channel's *General Channel Setup* register. Additionally, the sensing mode (or *PXS Mode*) of the channel must be specified for the associated cycle in the *Cycle Setup 1* register. Cycle and channel associations are given in Table 5.1.

5.4.2 Rx and Tx Selection

Each sensor must have an associated Rx and Tx selected. Tx pins are assigned per cycle in the *Cycle Setup 1* register, while Rx pins are assigned per channel in the *CRX Select* register.

While any pin may be used as Tx for either prox engine, only certian pins may be used as Rx for each prox engine, as shown in Table 5.2

Table 5.2: Rx Prox Engine Relationship

CRx	Prox Engine A	Prox Engine B
CRx0	✓	-
CRx1	✓	-
CRx2	✓	-
CRx3	✓	-
CRx4	-	✓
CRx5	-	✓
CRx6	-	✓
CRx7	-	✓

Additional notes:

- For self-capacitive sensors, both Rx and Tx must be assigned to the same pin.

5.4.3 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}), also known as the conversion frequency, is set using the *Conversion Frequency Fraction* and *Conversion Frequency Period* fields in the *Cycle Setup 0* register. This frequency is derived from the system clock, f_{OSC}.

For capacitive sensing, a lower frequency allows the capacitive electrode to charge and discharge completely. For inductive sensing, this frequency should be selected based on the resonant frequency of the LC circuit, unless *FOSC Tx Frequency* is used. Lower frequencies may provide more stable measurements, but increase sensing duration and current consumption.

It is recommended to always set the *Conversion Frequency Fraction* to '127' and to select the conversion frequency with the *Conversion Frequency Period*. Please refer to Tables A.9 and A.10 to select suitable *Conversion Frequency Period* values for the desired conversion frequency.

The *Dead Time Enable* option in the *Cycle Setup 1* register must be considered when setting the conversion frequency. Dead time should always be enabled for capacitance measurements, and disabled for inductive measurements.

5.4.4 FOSC Tx Frequency

The *FOSC Tx Frequency* setting in the *Cycle Setup 1* register enables f_{OSC} (14 MHz or 18 MHz) as output on the associated Tx pins during sensing. This can be used to excite resonated inductive sensors at a frequency higher than can be achieved using the charge transfer frequency. This is beneficial for certain inductive sensing applications, but is not supported for capacitive sensing.

5.4.5 Maximum Counts

The *Maximum Counts* setting in the *Global Cycle Setup* register sets the maximum counts value that the Proxfusion engine will allow a particular measurement or channel to reach. This acts as a timeout, stopping the measurement early if the sensing takes too long to complete. The resulting counts stored for that measurement will be set to the maximum counts value. Available values are:

- 1023 counts
- 2047 counts
- 4095 counts
- 16383 counts

The maximum counts should be increased if a high target value is used on a particular channel. (For example, 2047 or 4095 should be used for a channel with a target of 1000). However, this may (situationally) increase current consumption and increase ATI duration.

5.4.6 Cs Size

The *Cs Size* setting in the *CRX Select and General Channel Setup* register sets the size of the internal sampling capacitor to either 40 pF or 80 pF. It is recommended to use the 80 pF capacitor wherever possible. However, the 40 pF capacitor requires only half the amount of charge to reach its threshold voltage, and may therefore be used in designs where the load/signal is very small.

The effective size of the internal sampling capacitor may be further reduced by enabling *Vref 0.5 V Enable* in the *CRX Select and General Channel Setup* register. This setting lowers the threshold voltage on the sampling capacitor. It is recommended to keep this disabled.

5.5 ProxFusion UI Settings

5.5.1 Filtering

Raw counts obtained from the ProxFusion engines are filtered using a low-pass IIR filter to reduce the high-frequency noise in the measurement. The response of the filter can be adjusted with the *Filter Beta* values. Higher beta values result in a slower filter response, with less noise on the measurement. Note that the selected filter beta values apply to all channels.

Separate beta values are used for normal power and lower power modes. It may be beneficial to use a lower beta value for low power modes, which have lower sampling rates, in order to maintain responsiveness to user inputs.

Each beta setting is a 4-bit value, with a range of ‘0’ – ‘15’, where ‘0’ is no filtering, and ‘15’ is maximum filtering. Counts filtering typically uses low values, under ‘3’, to ensure responsiveness.

5.5.2 Long Term Average

The *Long Term Average* (LTA) is derived from the *filtered counts*, and acts as a stable reference value. While the channel is not in activation, the LTA is slowly updated to track changes in the environment using a low-pass filter. During activation, the LTA is kept fixed (halted). The LTA filter response is controlled by the *LTA Beta* values. LTA beta values should typically be ‘8’ or higher.

The difference between the filtered counts and the LTA is stored as the Delta value. The IQS7222B uses this delta value to detect proximity and touch activations.

$$\text{Delta} = \text{LTA} - \text{Counts} \tag{1}$$

5.5.3 Reseed

The *Reseed* function of the device will replace the filtered counts and the LTA value of the channel with the latest sampled raw counts value to reset the environmental reference of the channel. This may be necessary in certain instances when a channel gets incorrectly stuck in an activation.

The *Reseed* command can be given manually by setting the corresponding bit in the *Control Settings* register.

5.5.4 Proximity Event

A proximity event occurs on a channel when the *Delta* exceeds the *Proximity Threshold*, which is set in the *Channel Setup 0* register.

To reduce jitter and false events, debouncing is applied to the channel when the delta initially crosses the proximity threshold. Debouncing forces the IQS7222B to perform a number of quick measurements, checking that all measurements exceed the threshold. The number of high-frequency measurements that are executed during debouncing is controlled by the *Channel Setup 0* register, and can be configured independently for entering or exiting proximity events. Setting the debounce values to ‘0’ or ‘1’ will disable debouncing.

The proximity threshold and debouncing settings can be configured separately for each channel. An active proximity activation is indicated in the *Proximity Event States* register.

5.5.5 Touch Event

A touch event occurs on a channel when the delta exceeds the touch threshold. The touch threshold is calculated on-chip as a function of the LTA and an 8-bit *Touch Threshold* value stored in the *Channel Setup 1* register.

$$T_{\text{counts}} = \frac{T_{\text{reg}} \times \text{LTA}}{256} \tag{2}$$

where

- T_{reg} is the 8-bit value stored in the *Touch Threshold* setting, and
- T_{counts} is the resulting threshold value in counts (rounded down).

Touch enter and exit events are not debounced. However, hysteresis is applied on touch release in order to reduce jitter. The size of the hysteresis is controlled by the *Hysteresis* setting in the *Channel Setup 1* register, and its value in counts ($\mathrm{H_{counts}}$) is calculated as

$$\mathrm{H_{counts}} = \frac{\mathrm{H_{reg}} \times \mathrm{T_{counts}}}{256} \tag{3}$$

where $\mathrm{T_{counts}}$ is obtained from Equation (2), and $\mathrm{H_{reg}}$ is the 8-bit *Hysteresis* setting value.

Therefore, taking on-chip integer division into account, the touch "exit" threshold can be calculated as

$$\text{Exit Threshold (counts)} = \mathrm{floor}\left(\frac{\text{LTA} \times \left(\mathrm{T_{reg}} - \mathrm{floor}\left(\frac{\mathrm{T_{reg}} \times \mathrm{H_{reg}}}{256}\right)\right)}{256}\right). \tag{4}$$

For example, assume an LTA value of 500, threshold setting of '20', and a hysteresis setting of '50'. The touch enter threshold in counts is calculated as

$$\mathrm{T_{enter(counts)}} = \mathrm{floor}\left(\frac{20 \times 500}{256}\right) = 39\,\text{counts},$$

and the exit threshold is calculated as

$$\mathrm{T_{exit(counts)}} = \mathrm{floor}\left(\frac{500 \times \left(20 - \mathrm{floor}\left(\frac{20 \times 50}{256}\right)\right)}{256}\right) = 33\,\text{counts}.$$

5.5.6 Event Direction

Negative delta values are typically ignored, as they typically indicate an unexpected decrease in signal. This can occur due to sudden environmental changes, or due to the user releasing the sensor after the sensor was calibrated while in a touch state. Proximity and touch events are therefore only registered if the delta is positive, or

$$\text{Counts} < \text{LTA} - \text{Threshold}. \tag{5}$$

When a large negative delta is detected, the IQS7222B switches the LTA filter beta to the Fast LTA beta, which can be configured to track the counts more quickly to exit the negative delta state.

This behavior can be modified with the following settings from the *CRX Select and General Channel Setup* register:

- The *Invert* bit changes the sign of the delta, so events are set when

  $$\text{Counts} > \text{LTA} + \text{Threshold}. \tag{6}$$

  This is required for mutual capacitive sensing and inductive sensing.
- Bi-directional sensing ignores the sign of the delta, so that events are detected for either positive or negative deltas. The Fast LTA beta is never used.

5.5.7 Event Timeouts

In order to prevent stuck states where a channel is incorrectly stuck in a proximity or touch event (when the LTA filter is halted), the IQS7222B provides timeouts for proximity and touch events. The duration of these timeouts are controlled by the *Proximity Event Timeout* and *Touch Event Timeout* values in the *Event Timeouts* register, and can be set in 500 ms increments. Once the timeout duration expires, the channel is automatically reseeded.

Event timeouts can be configured per-channel. A timeout may be disabled by setting the register value to ‘0’. Disabling the timeout is required for ULP entry channels retaining an active state in ULP.

5.5.8 Global Halt

The global halt feature provides functionality to halt the LTA filters of certain channels if any of them are in activation.

Global halt can be enabled for any channel by setting the *Global Halt* bit in the channel’s *General Channel Setup* register.

If any global-halt-enabled channels are in activation, the *Global Halt* flag in the *System Status* register is set. Once *Global Halt* is set, all channels that have global halt enabled will keep their LTA values static until all the relevant channels exit activation.

5.6 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in ProxFusion devices to allow optimal performance of the devices for a wide range of sensing electrode designs, without modification to external components. The ATI functionality ensures that sensor sensitivity is not affected by external influences such as temperature, parasitic capacitance, and ground reference changes.

In order for the ProxFusion engine to handle a wide range of capacitive loads and input signals, the IQS7222B provides two mechanisms to condition the input signal for a desired working counts range: gain and DC subtraction. Gain scales the sensor input to a desired range. The amount of gain is controlled by the *Multipliers and Dividers* register. After the gain stage, DC subtraction is performed to compensate for DC offsets and increase sensitivity to changes in the input signal. DC subtraction is controlled by the *Compensation* register. Multipliers, dividers, and compensation are adjusted on a per-channel basis.

The working range of each channel of the IQS7222B can be calibrated automatically using the on-chip ATI feature, which adjust the *Multiplier and Divider* and *Compensation* registers until the reported counts from the sensor reaches a set of target counts values. These targets are known as the *ATI Base* and *ATI Target*.

The *ATI Base* value sets the desired nominal counts of a channel after the gain stage, and thus controls the amount of gain applied to the input signal. The *ATI Target* value sets the desired raw counts after both the gain and DC subtraction stages. The ATI algorithm first calibrates the multipliers to reach the Base counts, then calibrates the compensation to reach the target counts. Since counts are inversely proportional to signal strength, using DC subtraction will cause an increase in counts. Therefore the Target should always be higher than the Base value if compensation is required. Typical values for the Base value lie between 100 and 500 counts, while the Target is typically set to between 500 and 1000 counts.

Note that the Base value in counts is calculated from the 5-bit register value as Base counts $= 16 \times$ *Base Register Value*. The target value in counts is calculated from its 8-bit register value as

Target counts $= 8 \times$ *Target Register Value*. Base and target selection also allows for fine adjustment of the sensitivity of the sensor to user interaction, following the relationship

$$\text{Sensitivity} \propto \frac{\text{Target}}{\text{Base}}.$$

Sensitivity can thus be increased by either increasing the Target value or decreasing the Base value. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility.

Compensation is typically not recommended for inductive sensing. Compensation may be disabled by setting Base $\geq$ Target.

ATI can be triggered manually by setting the *ATI* bit in the *Control Settings* register. ATI may also be triggered automatically under certain conditions, described in Section 5.6.3.

5.6.1 ATI Modes

The ATI functionality can be set to one of the following modes:

- Full ATI
- ATI From Coarse Fractional Divider
- ATI From Fine Fractional Divider
- ATI From Compensation Divider
- ATI From Compensation Only
- ATI Disabled

"Full ATI" will calibrate all the *Multipliers and Dividers* and the *Compensation*. "ATI From Compensation Divider" will only calibrate the Compensation register. This allows an application to use a fixed set of Multipliers for all devices across production. "ATI Disabled" will never allow the channel to perform an ATI calibration, even if an ATI command is given.

5.6.2 ATI Error

After the ATI algorithm has completed, a check is performed to verify that no errors occurred during the ATI execution. An *ATI Error* is reported in the *System Status* register if one of the following conditions occur for any channel:

- ATI Compensation = 0 (mininum value)
- ATI Compensation = 1023 (maximum value)
- Reported counts value is outside the Re-ATI range upon completion of the ATI algorithm

The *ATI Error* status is only updated the next time ATI executes.

5.6.3 Automatic Re-ATI

The Automatic Re-ATI feature allows for easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor, and can also automatically recalibrate the sensor if environmental drift is detected. It is always recommended to have the automatic Re-ATI functionality enabled. When a Re-ATI is performed on the IQS7222B, a status bit will be momentarily set to indicate that this has occurred.

A Re-ATI is automatically triggered under the following conditions:

- If an ATI Error occurs.
- When the reference of a channel drifts outside of the acceptable range around the ATI Target.

The threshold to trigger an ATI due to reference drift is controlled by the *ATI Band* setting, which is specified as a fraction of the ATI target. The band can be set to one of the following values in the *CRX Select and General Channel Setup* register:

- 1/2
- 1/4
- 1/8
- 1/16

The boundaries around the ATI Target where re-ATI occurs is calculated as $\pm(\text{ATI Target} \times \text{ATI Band})$.

For example, for an ATI Target of 800 counts and an ATI band of 1/8, the boundary value is $800 \times \frac{1}{8} = 100$ counts. If Re-ATI is enabled, the ATI algorithm will be triggered under the following conditions:

$$\text{Reference} < 700 \quad \text{or} \quad \text{Reference} > 900$$

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI Error Timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. The ATI Error Timeout is specified in increments of 0.5 seconds. An ATI error should, however, not occur under normal circumstances.

5.7 Summary of ProxFusion® Settings

5.7.1 Summary of Cycle Settings

Cycle settings apply to both channels associated with that cycle. A list of settings related to cycle setup is given in Table 5.3 below.

Table 5.3: Cycle Settings

Setting	Description
PXS Mode	Sets the sensing mode for the cycle. See Table A.11.
Conversion Frequency Fraction	Sets the conversion frequency. See Section 5.4.3.
Conversion Frequency Period	
Dead Time Enable	Enable for capacitive sensing, disable for inductive sensing. See Section 5.4.3.
F_{OSC} Tx Frequency	Recommended for inductive sensing only. See Section 5.4.4.
Tx Selection	CTx0 to CTx8. See Section 5.4.2.
Maximum Counts	See Section 5.4.5.
Ground Inactive Rx's	Ground or float unused Rx pins. It is always recommended to ground inactive Rxs.
V_{bias} Enable	Enable V_{bias} (constant voltage drive onto CTx8) for resonant inductive sensing. Recommend keeping disabled.

5.7.2 Summary of Channel Settings

Settings related to channel setup are shown in Table 5.4 below.

Table 5.4: Channel Settings

Setting	Description
Channel Enable	Enables sensing on the channel.
Rx Selection	CRx0 to CRx7. See Section 5.4.2.
Cs Size	80 pF recommended. See Section 5.4.6.
Vref 0.5 V Enable	Recommend keeping this disabled. See Section 5.4.6.
Projected Bias Select	Selection of bias current for mutual capacitive mode. Set to 10 µA. See Table A.17.
Proximity Threshold	See Section 5.5.4.
Touch Threshold	See Section 5.5.5.
Proximity Enter Debounce	Section 5.5.4.
Proximity Exit Debounce	Section 5.5.4.
Touch Hysteresis	See Section 5.5.5.
Proximity Event Timeout	Section 5.5.7.
Touch Event Timeout	Section 5.5.7.
ATI Mode	Auto Tuning Implementation mode. See Section 5.6.1.
ATI Base	See Section 5.6.
ATI Target	See Section 5.6.
ATI Band	See Section 5.6.3.
Invert Direction	See Section 5.5.6.
Bi-directional Sensing	See Section 5.5.6.
Global Halt	See Section 5.5.8.

5.7.3 Summary of Global Settings

Global UI settings are listed in Table 5.5 below.

Table 5.5: Global Settings

Setting	Description
Counts Filter Beta	See Section 5.5.1.
Counts Low Power Filter Beta	
LTA Filter Beta	See Section 5.5.2.
LTA Low Power Filter Beta	
LTA Fast Filter Beta	See Section 5.5.6.
LTA Low Power Fast Filter Beta	

5.7.4 Summary of ProxFusion Outputs

ProxFusion sensor output registers are listed in Table 5.6 below.

Table 5.6: ProxFusion Sensor Outputs

Setting	Description
Proximity Event States	Shows proximity state of each channel.
Touch Event States	Shows touch state of each channel.
Channel X Counts	Filtered counts value of each channel.
Channel X LTA	Reference value of each channel.

6 Power Modes

6.1 Power Mode and Mode Timeout

The IQS7222B offers 3 power modes:

- Normal power mode (NP)
  - Flexible key scan rate
- Lower power mode (LP)
  - Flexible key scan rate
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimised firmware setup.
  - Intended for rapid wake-up on a single channel (e.g., distributed proximity event), enabling immediate button response for an approaching user.
  - The wake-up channels are sampled at the ULP report rate. These channels are updated at the rate calculated by ULP-RR × AUTO Mode Register Value.
  - The other sensors are sampled at the rate specified in the normal power update rate in the ultra-low power register.

To optimise power consumption and performance, power modes are "stepped" by default to move to power-efficient modes when no interaction has been detected for a certain (configurable) time known as the "mode timeout". The value for the power mode to never timeout (i.e, the current power mode will never progress to a lower power mode) is 0x00.

6.1.1 Ultra-Low Power Mode

In ULP mode, only Cycle 0 (Channels 0 and 10) are sampled. These channels should be used as wake-up channels, allowing the IQS7222B to wake up and switch to a higher power mode when detecting any user interaction.

CH0 and CH10 are sampled at the *ULP report rate*. LTA and filter values for CH0 and CH10 are not processed every cycle, but are processed once every N cycles, based on the *Auto Mode* setting in *Global Cycle Setup*.

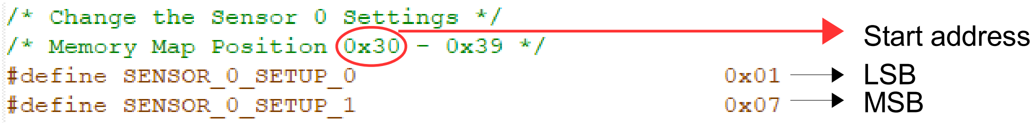
The IQS7222B will also wake up periodically to perform a full “Normal Power” cycle. Here, all channels are sampled, and their respective LTAs updated, in order to maintain consistent environmental tracking. The rate at which the IQS7222B performs these “Normal Power” cycles is controlled by the *Normal Power Update Rate in ULP* parameter, also known as the *ULP Timeout*. After this cycle, the IQS7222B returns to ULP mode.

7 Additional Features

7.1 Debug and Display Software (GUI)

The Azoteq IQS7222B GUI can be utilised to configure the optimal settings required for a specific hardware setup or application. The device performance can be easily monitored and evaluated in the graphical environment until the optimal device configuration is obtained.

Once the IQS7222B is configured in the GUI as desired, a C header file (.h file) can be exported that stores the values of all the read-write registers of the IQS7222B. The .h file displays the start address of each block of data, with each address containing two bytes in little endian order. An example of the .h file exported by the GUI is shown below.



```
/* Change the Sensor 0 Settings */
/* Memory Map Position 0x30 - 0x39 */
#define SENSOR_0_SETUP_0                        0x01
#define SENSOR_0_SETUP_1                        0x07
```

Figure 7.1: Example of an H file Exported by the GUI

7.2 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (Low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.
- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.

7.3 RF Immunity

The IQS7222B has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DDHI}.

Place a 100 pF in parallel with the 2.2 µF ceramic on V_{REG}. Place a 4.7 µF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470 Ω – 1 kΩ. PCB ground planes also improve noise immunity.

7.4 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*, if it becomes set again, the master will know a reset has occurred, and can react appropriately.

While *Reset* bit remains set:

- The device will not be able to enter into I²C Event mode operation (i.e. streaming communication behavior will be maintained until the Reset bit is cleared).
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in much longer time to finish the ATI routine.

7.5 Software Reset

The IQS7222B can be reset by means of an I²C command (*Soft Reset*).

8 I^{2}C Interface

8.1 I^{2}C Module Specification

The device features a standard two-wire I^{2}C interface, complemented by a RDY (ready interrupt) line, supporting a maximum bit rate of up to 1 Mbit/s. The IQS7222B implements a combination of 8-bit addressing and 16-bit addressing, with 2 data bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes, stored at each address in little-endian order, will be referred to as “byte 0” (least significant byte) and “byte 1” (most significant byte).

Features:

- Standard two-wire interface with RDY interrupt line
- *Fast-Mode Plus* I^{2}C with up to 1 Mbit/s bit rate
- 7-bit device address
- Combination of 8-bit and 16-bit register addressing
- Two data bytes stored per register address, in little-endian order
- Streaming and Event modes

8.2 I^{2}C Address

The 7-bit device address for order code 001 is 0x56 (0b01010110), The full address byte for address 0x56 will thus be 0xAD (read) or 0xAC (write).

Other address options exist on special request. Please contact Azoteq.

8.3 I^{3}C Compatibility

This device is not compatible with an I^{3}C bus due to clock stretching allowed for data retrieval.

8.4 Memory Map Addressing

8.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement a 16-bit addressing scheme.

8.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to address each block as an 8-bit address and then continue to clock into the next address locations. Figure 8.1 depicts a hypothetical procedure to read data from address 0xE000 to 0xE003 by sending 0xE0 as the register address.

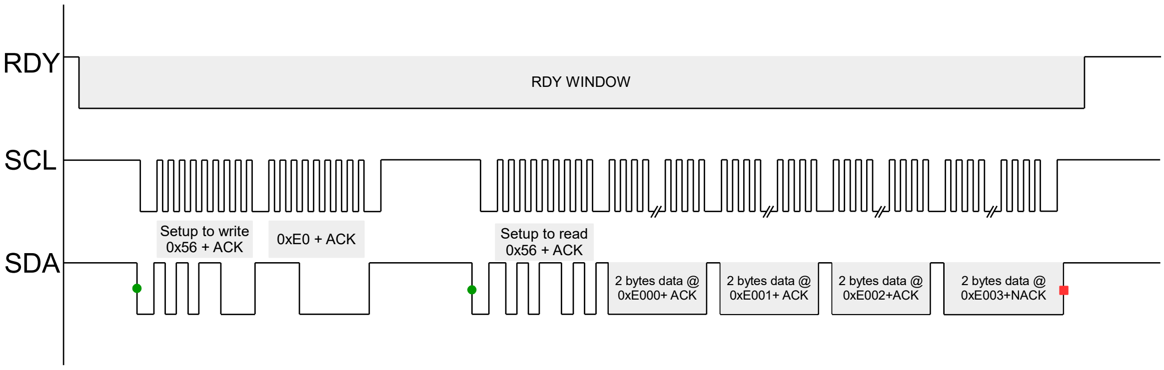


Figure 8.1: Extended 16-bit Addressing for Continuous Block

However, in order to address specific bytes in the extended memory map space, the full 16-bit address must be sent in big endian order (most significant byte first). Below is an example of reading data bytes from register 0xE003.

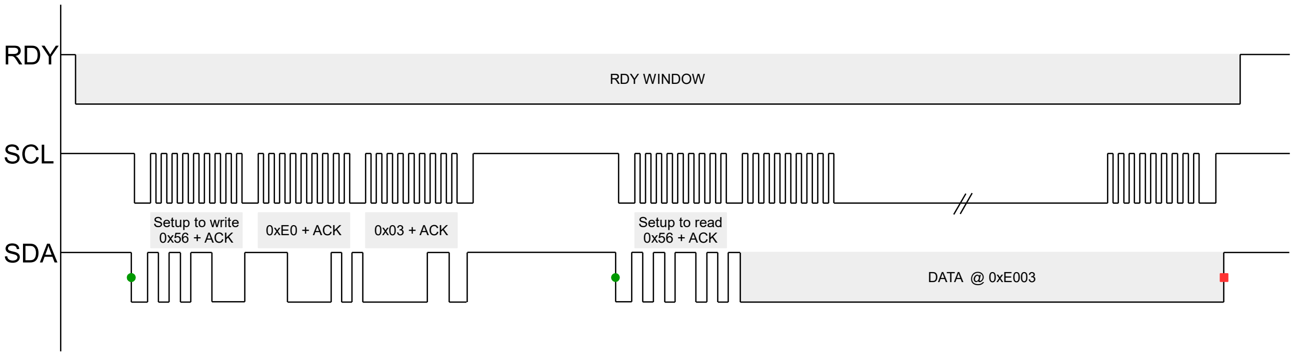


Figure 8.2: Extended 16-bit Addressing for a Specific Register

Note that extended 16-bit addresses are sent in big endian order, but data from those addresses is stored in little endian format.

8.5 Memory Map Data

Data is stored in 16-bit words, meaning that each address contains two bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11. The 16-bit data is sent in little endian byte order (least significant byte first).

8.6 RDY/IRQ

The IQS7222B has an open-drain active low RDY signal to inform the master that updated data is available. The IQS7222B will pull the RDY line low to indicate that it has opened a communications window, or "RDY window", for the master to read the new updated data. While the master can communicate with the device at any time according to the *Force Communication Method*, it is recommended to use the RDY signal for optimal power consumption. Integrating the RDY signal as an interrupt input allows the master MCU to read and write data efficiently.

The IQS7222B will open a communication window when new data is available, and will typically close the window after an I^{2}C stop event is detected.

8.7 I²C Interface Modes

The IQS7222B has three *I²C interface options*:

- **Streaming Mode**: The IQS7222B opens a communication window (by pulling the RDY pin low) after every sensing cycle to report new data. This mode is useful for evaluation and debugging.
- **Event Mode**: A communication window is opened only if an enabled event occurs, and activity is detected. This reduces the amount of unnecessary I²C traffic and RDY interrupts, and is the recommended mode for normal operation.
- **Stream in Touch Mode**: Stream in Touch is a hybrid between Streaming Mode and Event Mode. The device follows the Event Mode I²C protocol. When a touch is registered on any channel, the device enters Streaming Mode until the touch is released. This mode is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

8.8 Event Mode Communication

Event Mode bypasses the communication window when no activity is sensed. This is usually enabled since the master does not need to be interrupted unnecessarily during every cycle if no activity occurs. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

Event Mode can only be entered if the following requirements are met:

- Events must be serviced by reading from the *Events* register to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every cycle, similar to streaming mode.
- The *Device Reset* bit in the *System Status* register has been cleared by setting the *Acknowledge Reset* bit in *Control Settings*.

8.8.1 Events

Numerous events can be individually enabled to trigger communication in Event Mode. Bit definitions can be found in Tables A.2 and A.3:

- Power mode change
- Prox or touch event
- ATI event

8.8.2 Force Communication

In Streaming Mode, the IQS7222B I²C will provide communication windows at regular intervals specified by the relevant power mode report rate. This will provide the master with regular opportunities to perform I²C communication as necessary.

If the device is placed in Event Mode, the IQS7222B will not open RDY windows unless certain conditions are met. A new RDY window can be requested by writing 0xFF over I²C, followed by a stop condition. After a short delay, the IQS7222B will pull the RDY line low and open a new communication window. This is shown in Figure 8.3.

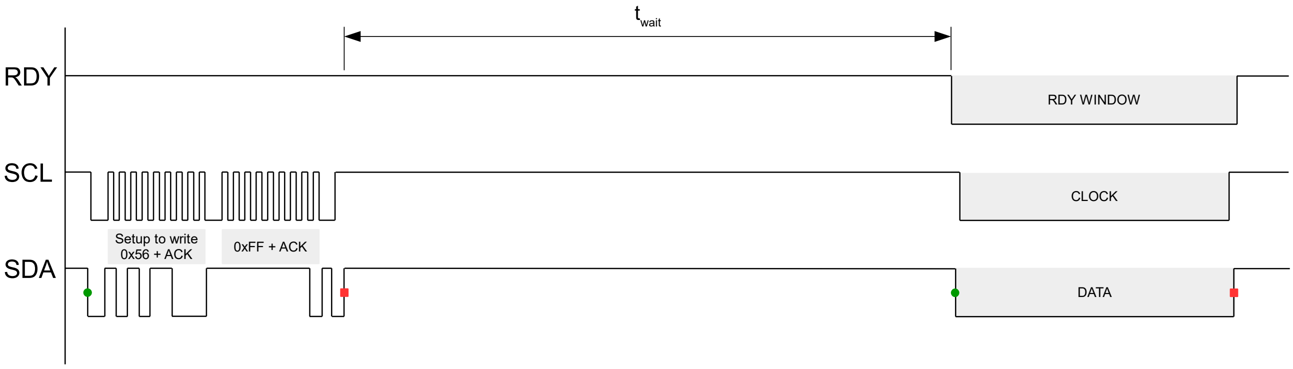


Figure 8.3: Force Communication Sequence

The time between the communication request and the opening of a RDY window (t_{wait}) is dependent on the specific application. Once the communication request is received, the IQS7222B wakes up from sleep mode, performs sampling and processing on all channels, and then opens a communication window. As a result, t_{wait} is dependent on channel and cycle settings, and may be on the order of 20 ms for a full 20-channel device.

Note: The IQS7222B may clock stretch (hold the SCL line low) for up to 400 µs after the 0xFF byte if the force communication command is received while the IQS7222B is in an internal sleep mode.

A force communication request should be avoided while RDY is held low, as the STOP condition after the 0xFF byte will cause an existing communication window to close immediately.

8.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside a communication window (while RDY is high).

8.10 I^{2}C Timeout

If the communication window is not serviced within the *Communication Timeout* period (in milliseconds), the session is ended (RDY goes high), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be lost, so this should be avoided. The default I^{2}C timeout period is set to 500 ms.

8.11 Terminate Communication

By default, a standard I^{2}C STOP will end the current communication window. If multiple I^{2}C transactions need to be performed within a single communication window, they should be strung together using repeated START conditions, with only the last transaction ending with a STOP. Allowing an I^{2}C STOP to terminate the communication window is recommended.

However, for I^{2}C controllers that cannot support repeated START conditions, the IQS7222B provides an option to ignore the STOP condition and keep the window open. This behaviour can be enabled by setting the *Stop Bit Disabled* bit in the *I^{2}C Communication* register.

In this case, the communication window can be terminated as desired using one of the following methods:

- Writing a single 0xFF byte will close the communication window, as illustrated in Figure 8.4.

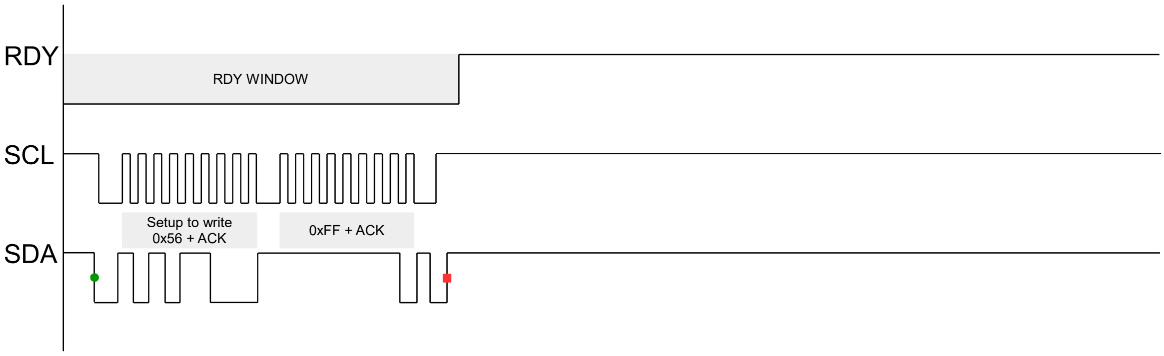


Figure 8.4: Force Stop Communication Sequence

- Alternatively, in each communication window, the stop bit check may be disabled in the first transaction, followed by normal I^{2}C transactions. The window can be closed by re-enabling the check as the final transaction, followed by a STOP.

8.12 Summary of I^{2}C Settings

Table 8.1: I^{2}C Module Settings

Setting	Description
Interface selection	Enable Streaming or Event Mode. See Section 8.7.
Event Mask	Sets which system events should open a communication window if in Event mode. See Section 8.8.1.
Stop Bit Disabled	See Section 8.11.
RW Check Disabled	See Table A.27.
I^{2}C Communication Timeout	See Section 8.10.

9 Program Flow Diagram

The program flow for event mode communication is shown in Figure 9.1.

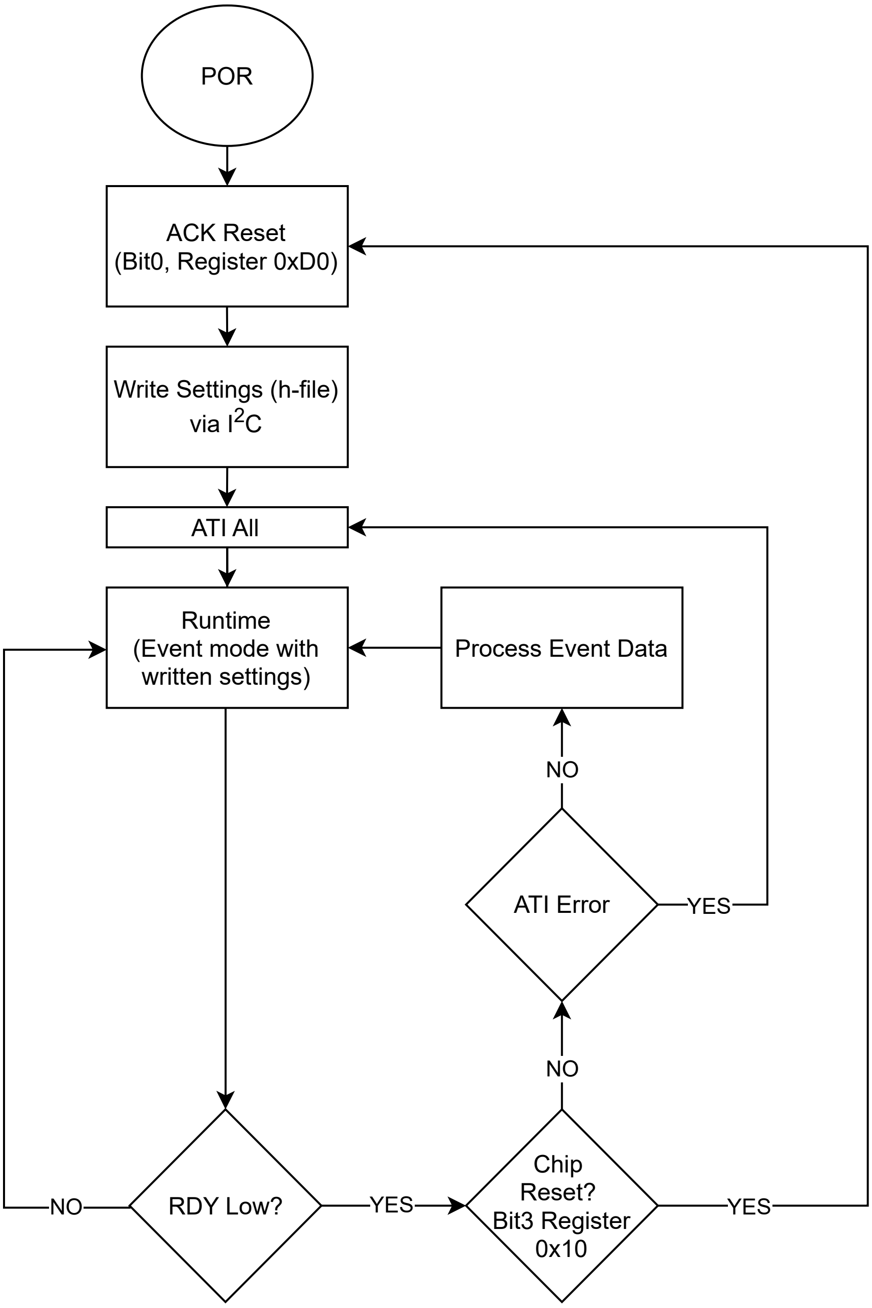


Figure 9.1: Progam Flow Diagram

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions.

Address	Data (16bit)	Default	Notes
0x00 - 0x09	Version details		See Table A.1
Read Only			
0x10	System Status		See Table A.2
0x11	Events		See Table A.3
0x12	Prox event States		See Table A.4
0x13			See Table A.5
0x14	Touch event States		See Table A.6
0x15			See Table A.7
Read Only	**Channel Counts**		
0x20	Channel 0 Counts		16-bit value
0x21	Channel 1 Counts		
0x22	Channel 2 Counts		
0x23	Channel 3 Counts		
0x24	Channel 4 Counts		
0x25	Channel 5 Counts		
0x26	Channel 6 Counts		
0x27	Channel 7 Counts		
0x28	Channel 8 Counts		
0x29	Channel 9 Counts		
0x2A	Channel 10 Counts		
0x2B	Channel 11 Counts		
0x2C	Channel 12 Counts		
0x2D	Channel 13 Counts		
0x2E	Channel 14 Counts		
0x2F	Channel 15 Counts		
0x30	Channel 16 Counts		
0x31	Channel 17 Counts		
0x32	Channel 18 Counts		
0x33	Channel 19 Counts		
Read Only	**Channel LTA**		
0x40	Channel 0 LTA		16-bit value
0x41	Channel 1 LTA		
0x42	Channel 2 LTA		
0x43	Channel 3 LTA		
0x44	Channel 4 LTA		
0x45	Channel 5 LTA		
0x46	Channel 6 LTA		
0x47	Channel 7 LTA		
0x48	Channel 8 LTA		
0x49	Channel 9 LTA		
0x4A	Channel 10 LTA		
0x4B	Channel 11 LTA		
0x4C	Channel 12 LTA		
0x4D	Channel 13 LTA		
0x4E	Channel 14 LTA		
0x4F	Channel 15 LTA		
0x50	Channel 16 LTA		
0x51	Channel 17 LTA		

0x52	Channel 18 LTA		
0x53	Channel 19 LTA		
Read-Write	**Cycle Setup**		
0x8000	Cycle 0 Setup	0x027F	See Table A.8
0x8001		0xC462	See Table A.11
0x8100	Cycle 1 Setup	0x057F	See Table A.8
0x8101		0x8062	See Table A.11
0x8200	Cycle 2 Setup	0x057F	See Table A.8
0x8201		0x4062	See Table A.11
0x8300	Cycle 3 Setup	0x057F	See Table A.8
0x8301		0x0462	See Table A.11
0x8400	Cycle 4 Setup	0x057F	See Table A.8
0x8401		0x8062	See Table A.11
0x8500	Cycle 5 Setup	0x057F	See Table A.8
0x8501		0x4062	See Table A.11
0x8600	Cycle 6 Setup	0x057F	See Table A.8
0x8601		0x0462	See Table A.11
0x8700	Cycle 7 Setup	0x057F	See Table A.8
0x8701		0x8062	See Table A.11
0x8800	Cycle 8 Setup	0x057F	See Table A.8
0x8801		0x4062	See Table A.11
0x8900	Cycle 9 Setup	0x057F	See Table A.8
0x8901		0x0462	See Table A.11
0x8A00	Global Cycle Setup	0x2B8B	See Table A.12
0x8A01	Coarse and Fine Divider Preloads	0x3010	See Table A.13
0x8A02	Compensation Preload	0x0200	See Table A.14
Read-Write	**Channel Setup**		
0x9000	Channel 0 Setup	0x120A	See Table A.15
0x9001		0x0019	See Table A.16
0x9100	Channel 1 Setup	0x120A	See Table A.15
0x9101		0x0019	See Table A.16
0x9200	Channel 2 Setup	0x120A	See Table A.15
0x9201		0x0019	See Table A.16
0x9300	Channel 3 Setup	0x120A	See Table A.15
0x9301		0x0019	See Table A.16
0x9400	Channel 4 Setup	0x120A	See Table A.15
0x9401		0x0019	See Table A.16
0x9500	Channel 5 Setup	0x120A	See Table A.15
0x9501		0x0019	See Table A.16
0x9600	Channel 6 Setup	0x120A	See Table A.15
0x9601		0x0019	See Table A.16
0x9700	Channel 7 Setup	0x120A	See Table A.15
0x9701		0x0019	See Table A.16
0x9800	Channel 8 Setup	0x120A	See Table A.15
0x9801		0x0019	See Table A.16
0x9900	Channel 9 Setup	0x120A	See Table A.15
0x9901		0x0019	See Table A.16
0x9A00	Channel 10 Setup	0x120A	See Table A.15
0x9A01		0x0019	See Table A.16
0x9B00	Channel 11 Setup	0x120A	See Table A.15
0x9B01		0x0019	See Table A.16

0x9C00	Channel 12 Setup	0x120A	See Table A.15
0x9C01		0x0019	See Table A.16
0x9D00	Channel 13 Setup	0x120A	See Table A.15
0x9D01		0x0019	See Table A.16
0x9E00	Channel 14 Setup	0x120A	See Table A.15
0x9E01		0x0019	See Table A.16
0x9F00	Channel 15 Setup	0x120A	See Table A.15
0x9F01		0x0019	See Table A.16
0xA000	Channel 16 Setup	0x120A	See Table A.15
0xA001		0x0019	See Table A.16
0xA100	Channel 17 Setup	0x120A	See Table A.15
0xA101		0x0019	See Table A.16
0xA200	Channel 18 Setup	0x120A	See Table A.15
0xA201		0x0019	See Table A.16
0xA300	Channel 19 Setup	0x120A	See Table A.15
0xA301		0x0019	See Table A.16
Read-Write	**Channel Setup**		
	Channel 0		
0xB000	CRX Select and General Channel Setup	0x1573	See Table A.17
0xB001	ATI Base and Target	0x643D	See Table A.19
0xB002	Fine and Coarse Multipliers		See Table A.20
0xB003	ATI Compensation		See Table A.21
	Channel 1		
0xB100	CRX Select and General Channel Setup	0x1513	See Table A.17
0xB101	ATI Base and Target	0x3E3D	See Table A.19
0xB102	Fine and Coarse Multipliers		See Table A.20
0xB103	ATI Compensation		See Table A.21
	Channel 2		
0xB200	CRX Select and General Channel Setup	0x1513	See Table A.17
0xB201	ATI Base and Target	0x3E3D	See Table A.19
0xB202	Fine and Coarse Multipliers		See Table A.20
0xB203	ATI Compensation		See Table A.21
	Channel 3		
0xB300	CRX Select and General Channel Setup	0x1513	See Table A.17
0xB301	ATI Base and Target	0x3E3D	See Table A.19
0xB302	Fine and Coarse Multipliers		See Table A.20
0xB303	ATI Compensation		See Table A.21
	Channel 4		
0xB400	CRX Select and General Channel Setup	0x1523	See Table A.17
0xB401	ATI Base and Target	0x3E3D	See Table A.19
0xB402	Fine and Coarse Multipliers		See Table A.20
0xB403	ATI Compensation		See Table A.21
	Channel 5		
0xB500	CRX Select and General Channel Setup	0x1523	See Table A.17
0xB501	ATI Base and Target	0x3E3D	See Table A.19
0xB502	Fine and Coarse Multipliers		See Table A.20
0xB503	ATI Compensation		See Table A.21
	Channel 6		
0xB600	CRX Select and General Channel Setup	0x1523	See Table A.17
0xB601	ATI Base and Target	0x3E3D	See Table A.19
0xB602	Fine and Coarse Multipliers		See Table A.20

0xB603	ATI Compensation		See Table A.21
	Channel 7		
0xB700	CRX Select and General Channel Setup	0x1543	See Table A.17
0xB701	ATI Base and Target	0x3E3D	See Table A.19
0xB702	Fine and Coarse Multipliers		See Table A.20
0xB703	ATI Compensation		See Table A.21
	Channel 8		
0xB800	CRX Select and General Channel Setup	0x1543	See Table A.17
0xB801	ATI Base and Target	0x3E3D	See Table A.19
0xB802	Fine and Coarse Multipliers		See Table A.20
0xB803	ATI Compensation		See Table A.21
	Channel 9		
0xB900	CRX Select and General Channel Setup	0x1543	See Table A.17
0xB901	ATI Base and Target	0x3E3D	See Table A.19
0xB902	Fine and Coarse Multipliers		See Table A.20
0xB903	ATI Compensation		See Table A.21
	Channel 10		
0xBA00	CRX Select and General Channel Setup	0x1573	See Table A.18
0xBA01	ATI Base and Target	0x643D	See Table A.19
0xBA02	Fine and Coarse Multipliers		See Table A.20
0xBA03	ATI Compensation		See Table A.21
	Channel 11		
0xBB00	CRX Select and General Channel Setup	0x1513	See Table A.18
0xBB01	ATI Base and Target	0x3E3D	See Table A.19
0xBB02	Fine and Coarse Multipliers		See Table A.20
0xBB03	ATI Compensation		See Table A.21
	Channel 12		
0xBC00	CRX Select and General Channel Setup	0x1513	See Table A.18
0xBC01	ATI Base and Target	0x3E3D	See Table A.19
0xBC02	Fine and Coarse Multipliers		See Table A.20
0xBC03	ATI Compensation		See Table A.21
	Channel 13		
0xBD00	CRX Select and General Channel Setup	0x1513	See Table A.18
0xBD01	ATI Base and Target	0x3E3D	See Table A.19
0xBD02	Fine and Coarse Multipliers		See Table A.20
0xBD03	ATI Compensation		See Table A.21
	Channel 14		
0xBE00	CRX Select and General Channel Setup	0x1523	See Table A.18
0xBE01	ATI Base and Target	0x3E3D	See Table A.19
0xBE02	Fine and Coarse Multipliers		See Table A.20
0xBE03	ATI Compensation		See Table A.21
	Channel 15		
0xBF00	CRX Select and General Channel Setup	0x1523	See Table A.18
0xBF01	ATI Base and Target	0x3E3D	See Table A.19
0xBF02	Fine and Coarse Multipliers		See Table A.20
0xBF03	ATI Compensation		See Table A.21
	Channel 16		
0xC000	CRX Select and General Channel Setup	0x1523	See Table A.18
0xC001	ATI Base and Target	0x3E3D	See Table A.19
0xC002	Fine and Coarse Multipliers		See Table A.20
0xC003	ATI Compensation		See Table A.21

	Channel 17		
0xC100	CRX Select and General Channel Setup	0x1543	See Table A.18
0xC101	ATI Base and Target	0x3E3D	See Table A.19
0xC102	Fine and Coarse Multipliers		See Table A.20
0xC103	ATI Compensation		See Table A.21
	Channel 18		
0xC200	CRX Select and General Channel Setup	0x1543	See Table A.18
0xC201	ATI Base and Target	0x3E3D	See Table A.19
0xC202	Fine and Coarse Multipliers		See Table A.20
0xC203	ATI Compensation		See Table A.21
	Channel 19		
0xC300	CRX Select and General Channel Setup	0x1543	See Table A.18
0xC301	ATI Base and Target	0x3E3D	See Table A.19
0xC302	Fine and Coarse Multipliers		See Table A.20
0xC303	ATI Compensation		See Table A.21
Read-Write	**Filter Betas**		
0xC400	Filter Beta	0x7812	See Table A.22
0xC401	Fast Filter Beta	0x0034	See Table A.23
Read-Write	**PMU and System Settings**		
0xD0	Control settings	0x0030	See Table A.24
0xD1	ATI Error Timeout	0x0002	16-bit value * 0.5 (s)
0xD2	ATI Report Rate	0x0000	16-bit value (ms)
0xD3	Normal Power Mode Timeout	0x1388	16-bit value (ms)
0xD4	Normal Power Mode Report Rate	0x0010	16-bit value (ms) Range: 0 - 3000
0xD5	Low Power Mode Timeout	0x1388	16-bit value (ms)
0xD6	Low Power Mode Report Rate	0x003C	16-bit value (ms) Range: 0 - 3000
0xD7	Normal Power Update rate in Ultra-low Power Mode	0x2710	16-bit value (ms)
0xD8	Ultra-low Power Mode Report Rate	0x0096	16-bit value (ms) Range: 0 - 3000
0xD9	Event Timeouts	0x2808	See Table A.25
0xDA	Event Enable	0xFFFF	See Table A.26
0xDB	I^2C Communication	0x000C	See Table A.27
0xDC	Communication Timeout	0x01F4	See Table A.28

11 Implementation and Layout

11.1 Layout Fundamentals

Note: Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

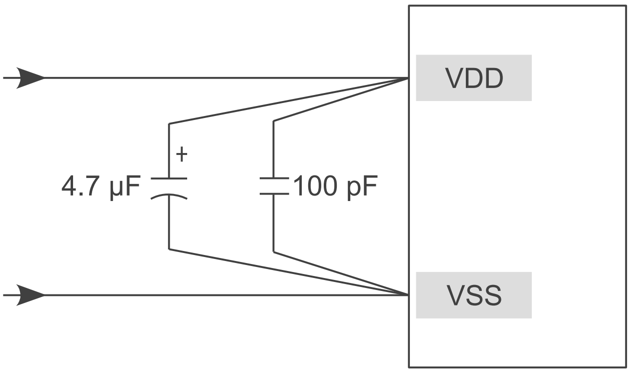


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. Figure 11.2 below shows an example placement of the VREG capacitors.

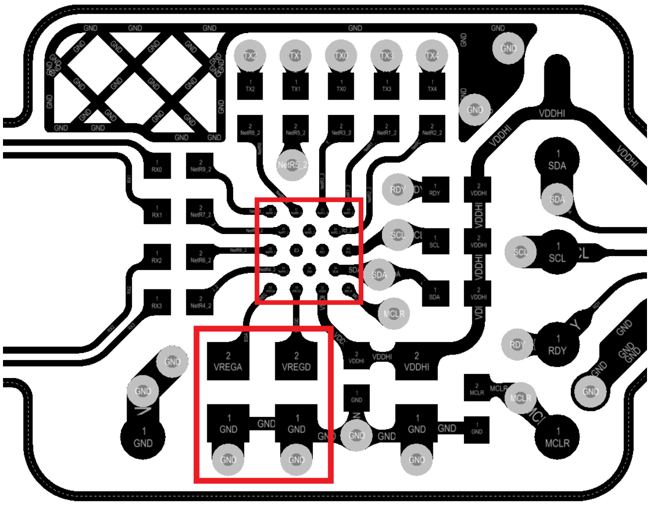


Figure 11.2: VREG Capacitor Placement Close to IC

11.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

12 Ordering Information

12.1 Ordering Code

IQS7222B zzz ppb

Table 12.1: Order Code Description

IC NAME				IQS7222B
POWER-ON CONFIGURATION	zzz	=	001	Reserved
			101	F_{OSC} = 18 MHz (NRFND)
			102	F_{OSC} = 14 MHz (NRFND)
			201	F_{OSC} = 18 MHz[i]
			202	F_{OSC} = 14 MHz[i]
PACKAGE TYPE	pp	=	CS	WLCSP-18 package
		=	QN	QFN-20 package
		=	QF	QFN-20 package
BULK PACKAGING	b	=	R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

12.2 Top Marking

12.2.1 WLCSP18 Package Marking

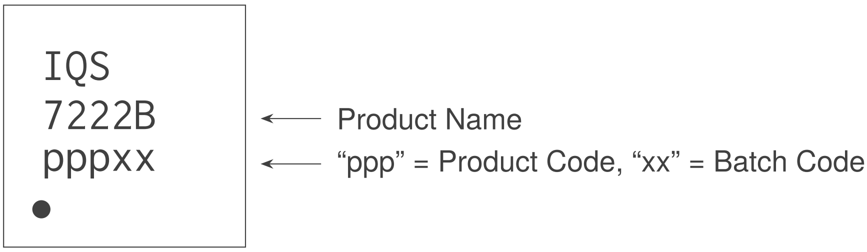


Figure 12.1: IQS7222B-WLCSP18 Package Top Marking

12.2.2 QFN20 Package Marking Option (IQS7222BzzzQNR)

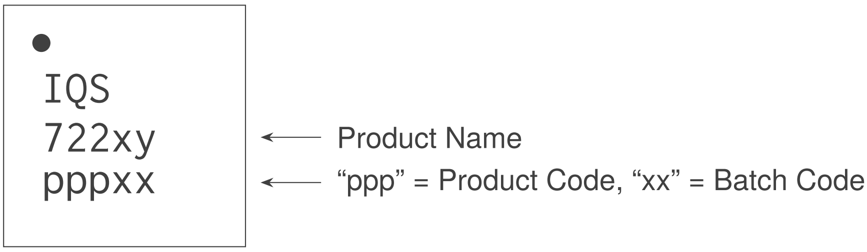


Figure 12.2: IQS722xy-QFN20 Package Top Marking

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[i] Please refer to product information notice PIN-230172 for more details

12.2.3 QFN20 Package Marking Option (IQS7222BzzzQFR)

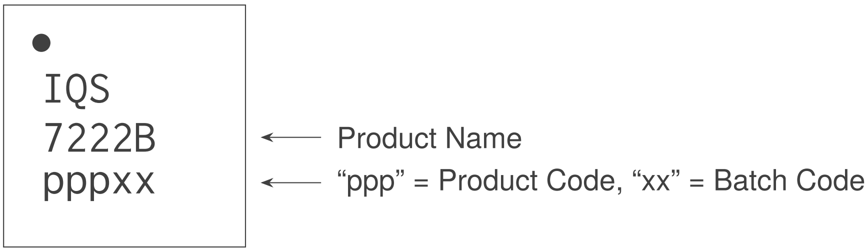
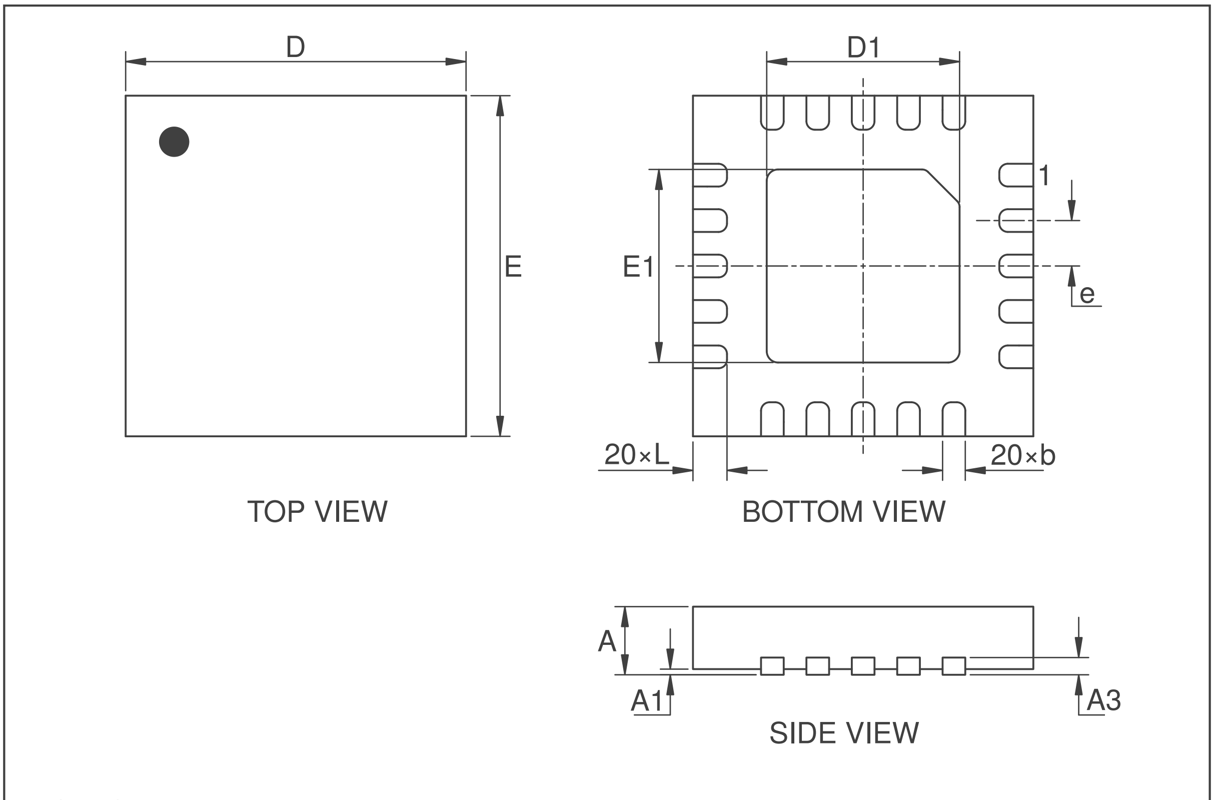


Figure 12.3: IQS7222B-QFN20 Package Top Marking

13 Package Specification

13.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.



NOTES:

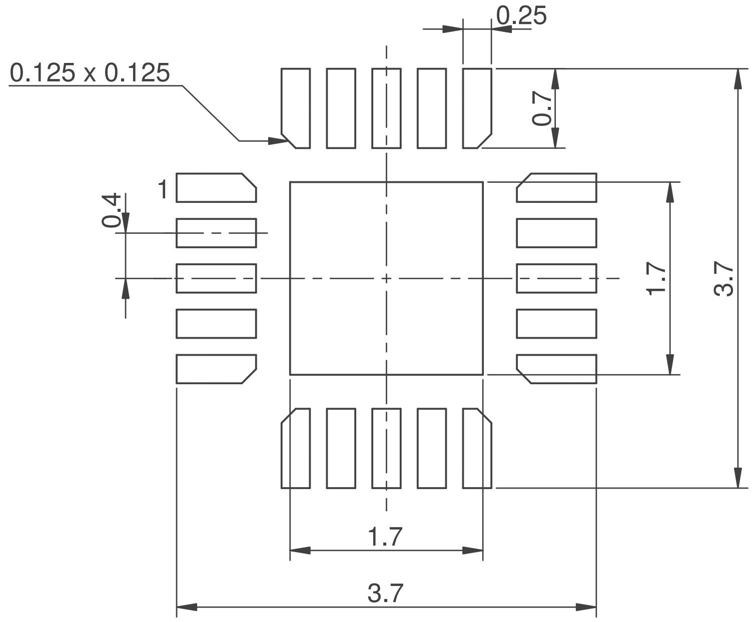
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 13.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

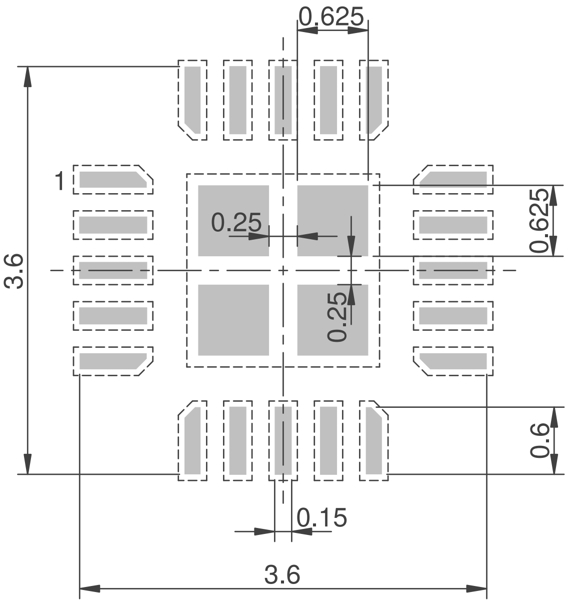
Table 13.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

13.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

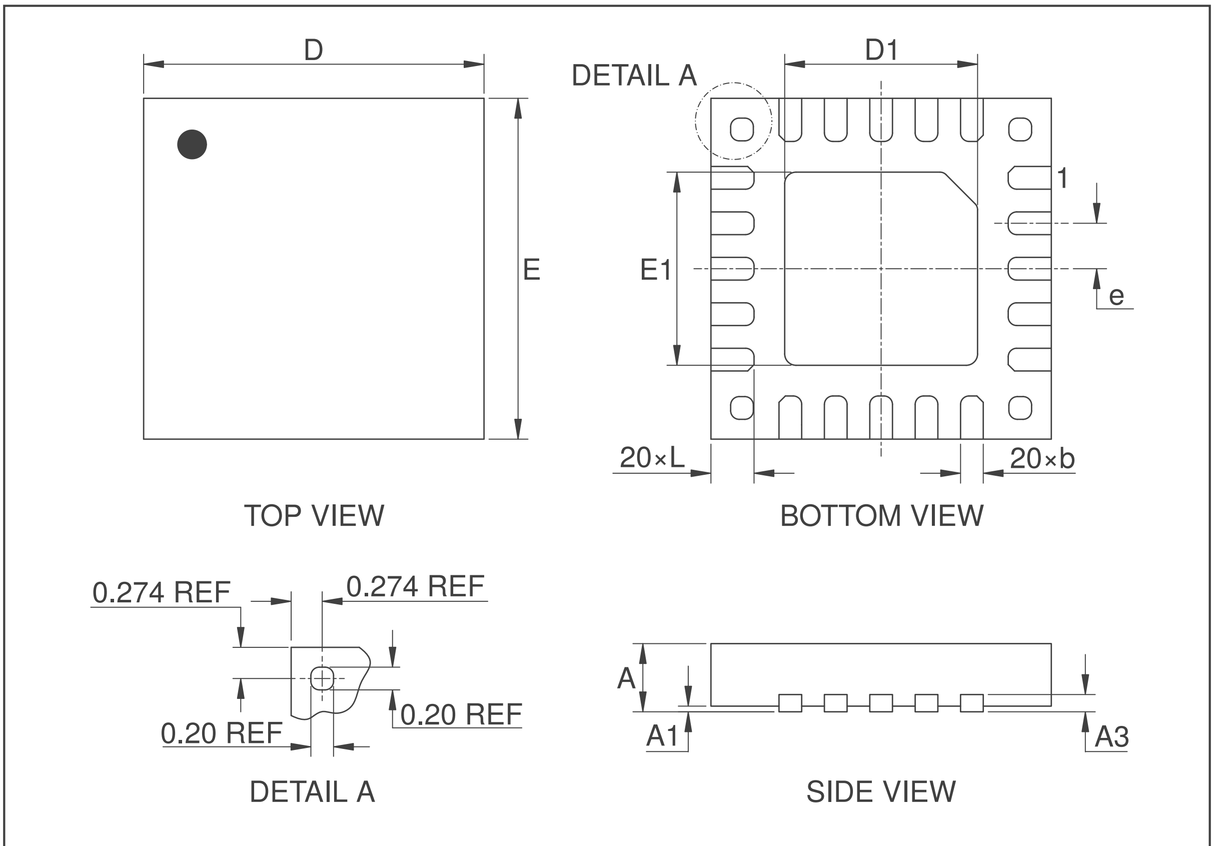
NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.2: QFN (3x3)-20 (QFR) Recommended Footprint

13.3 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.



NOTES:

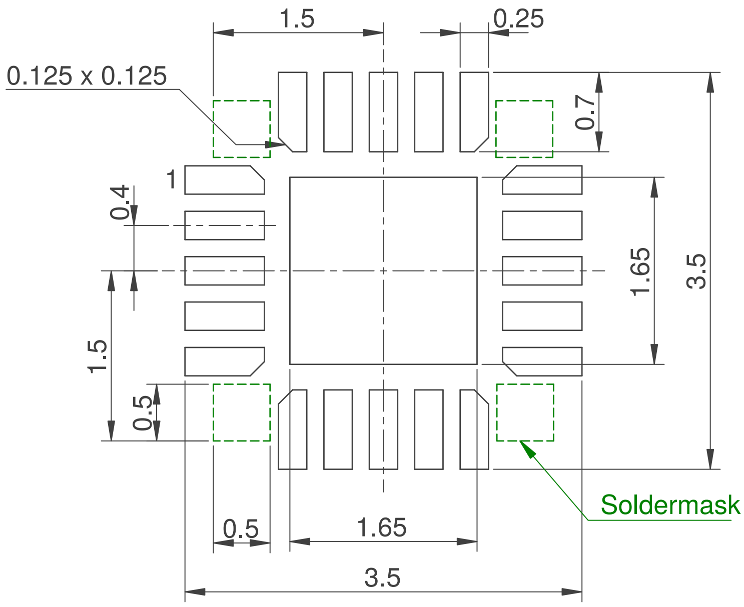
1. Drawing is not to scale.
2. Drawing is subject to change without notice.
3. Dimensions are in millimeters.

Figure 13.3: QFN (3x3)-20 (QNR) Package Outline Visual Description

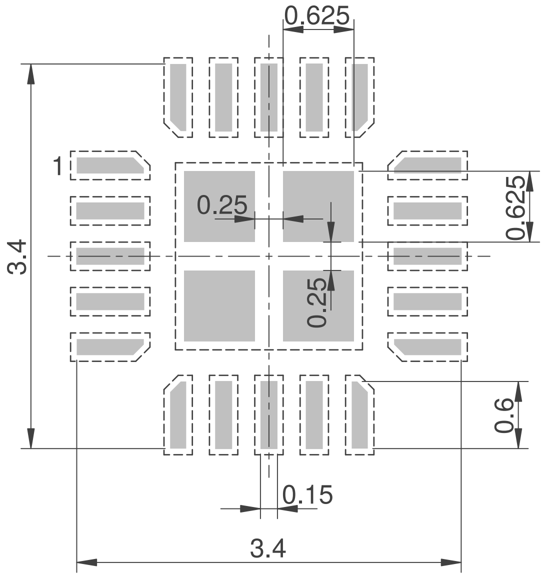
Table 13.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

13.4 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



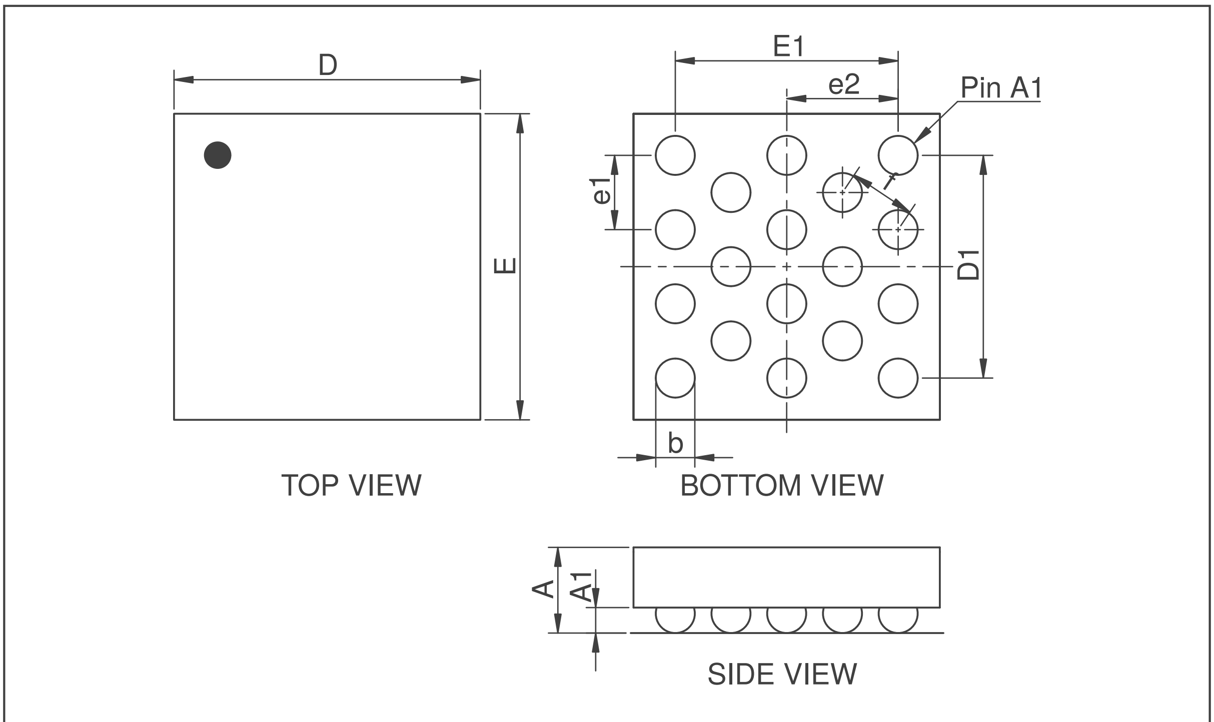
RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 13.4: QFN (3x3)-20 (QNR) Recommended Footprint

13.5 Package Outline Description – WLCSP18



NOTES:

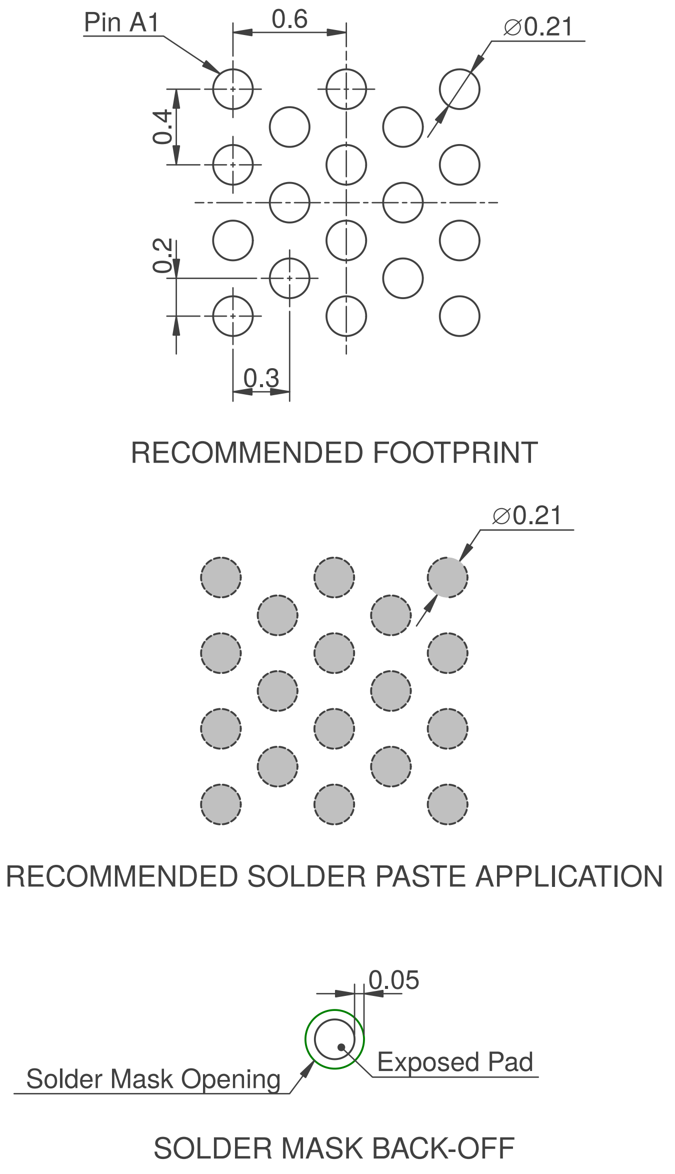
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 13.5: WLCSP (1.62x1.62)-18 Package Outline Visual Description

Table 13.3: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1		1.200 BSC	
E1		1.200 BSC	
e1		0.400 BSC	
e2		0.600 BSC	
f		0.360 REF	

13.6 Recommended PCB Footprint – WLCSP18

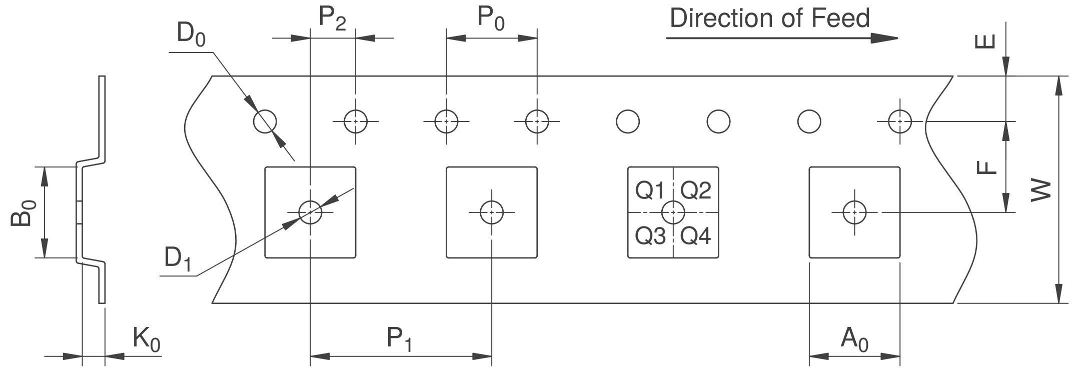


NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 13.6: WLCSP18 Recommended Footprint

13.7 Tape and Reel Specifications

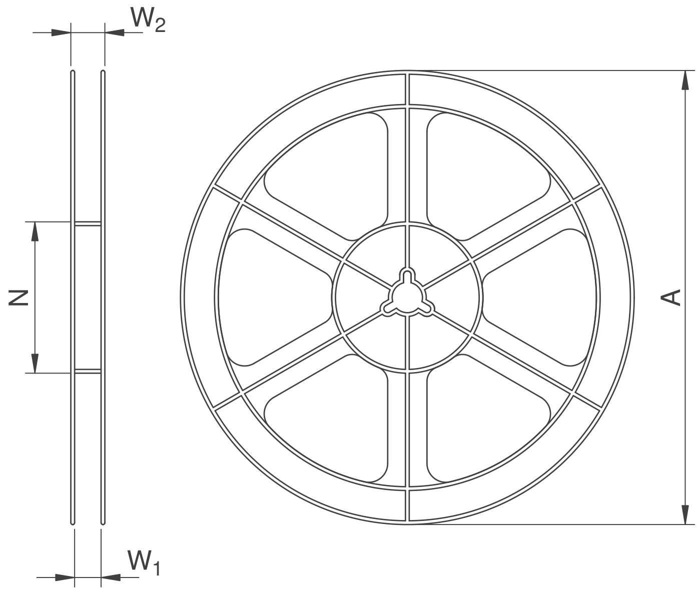


NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 13.7: Carrier Tape Specification

Table 13.4: Carrier Tape Dimensions [mm]

Dimension	Package		
	WLCSP18	QFN20 (QFR)	QFN20 (QNR)
A_0	1.78	3.30	3.30
B_0	1.78	3.30	3.30
K_0	0.69	0.75	0.80
D_0	1.50	1.50	1.55
D_1	0.50	1.55	1.50
E	1.75	1.75	1.75
F	3.50	5.50	5.50
P_0	4.00	4.00	4.00
P_1	4.00	8.00	8.00
P_2	2.00	2.00	2.00
W	8.00	12.00	12.00
Pin 1 Quadrant	Q1	Q2	Q2



NOTES:

1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 13.8: Reel Specification

Table 13.5: Reel Dimensions [mm]

Dimension	Package		
	WLCSP18	QFN20 (QFR)	QFN20 (QNR)
A	179	178	180
N	55	60	60
W_1	8.4	12.4	12.4
W_2 (Max)	14.4	18.4	18.4

13.8 Moisture Sensitivity Levels

Table 13.6: Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

13.9 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Please note: The value of all Read-write bits marked as Reserved, unless otherwise specified, can be set to 0 or 1 depending on customer's preference.

Table A.1: Version Information

Register: 0x00 - 0x09

Address	Catergory	Name	Value	Order Code	
0x00	Application Version Info	Product Number	698		16-bit value
0x01		Major Version	1		
0x02		Minor Version	27	001[i]	
			45	101/102[i]	
			46	201[ii]	
			47	202[ii]	
0x03		Patch Number (commit hash)	Reserved		
0x04					
0x05	ROM Library Version Info	Library Number	Reserved		
0x06		Major Version	Reserved		
0x07		Minor Version	Reserved		
0x08		Patch Number (commit hash)	Reserved		
0x09					

Table A.2: System Status

Register: 0x10

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	NP up-date	Current Power mode		Reset	Res	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global Halt not active
  - 1: Global Halt active
- Bit 6: **Normal Power Update**
  - 0: No Normal Power Update occured
  - 1: Normal Power update occured
- Bit 4-5: **Current Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Device Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.3: Events

Register: 0x11

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power Event	ATI Event	Reserved										Touch Event	Prox Event

- Bit 13: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred

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[i] Please refer to PCN-PR531-IQS7222B Product Change Note v1.0

[ii] Please refer to product information notice PIN-230172 for more details

- Bit 12: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 1: **Touch Event**
  - 0: No Touch Event occurred
  - 1: Touch Event occurred
- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

Table A.4: Proximity Event States 0

Register: 0x12

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-15: **Channel Prox Event**
  - 0: No prox event occurred on channel
  - 1: Prox event occurred on channel

Table A.5: Proximity Event States 1

Register: 0x13

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												CH19	CH18	CH17	CH16

- Bit 0-3: **Channel Prox Event**
  - 0: No prox event occurred on channel
  - 1: Prox event occurred on channel

Table A.6: Touch Event States 0

Register: 0x14

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-15: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.7: Touch Event States 1

Register: 0x15

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved												CH19	CH18	CH17	CH16

- Bit 0-3: **Channel Touch Event**
  - 0: No touch event occurred on channel
  - 1: Touch event occurred on channel

Table A.8: Cycle Setup 0

Register: 0x8000, 0x8100, 0x8200, 0x8300, 0x8400, 0x8500, 0x8600, 0x8700, 0x8800, 0x8900

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 15-8: **Conversion Frequency Period**
  - Range: 0 - 127
- Bit 7-0: **Conversion Frequency Fraction**
  - Fix to 127

It is recommended to fix the *Fraction* value to 127. For capacitive sensing, please refer to the following table to determine the *Period* value for the desired conversion frequency. The *Dead Time* setting must be enabled.

Table A.9: Supported Conversion Frequency Parameters for Capacitive Sensing

FRACTION	PERIOD	Conversion Frequency f_{xfer} 14 MHz f_{OSC}	18 MHz f_{OSC}
127	2	1.75 MHz	2.25 MHz
	3	1.40 MHz	1.80 MHz
	5	1.00 MHz	1.29 MHz
	7	778 kHz	1.00 MHz
	12	500 kHz	643 kHz
	16	389 kHz	500 kHz
	23	280 kHz	360 kHz

* The maximum recommended conversion frequency for self-capacitive sensing is 1 MHz. The maximum recommended conversion frequency for mutual-capacitive sensing is 2 MHz.

For inductive sensing, please refer to the following table to determine the *Period* value for the desired conversion frequency. The *Dead Time* setting must be disabled.

Table A.10: Supported Conversion Frequency Parameters for Inductive Sensing

FRACTION	PERIOD	Conversion Frequency f_{xfer} 14 MHz f_{OSC}	18 MHz f_{OSC}
127	0	7.00 MHz	9.00 MHz
	1	3.50 MHz	4.50 MHz
	2	2.33 MHz	3.00 MHz
	3	1.75 MHz	2.25 MHz
	4	1.40 MHz	1.80 MHz
	6	1.00 MHz	1.29 MHz
	8	778 kHz	1.00 MHz
	13	500 kHz	643 kHz

Table A.11: Cycle Setup 1

Register: 0x8001, 0x8101, 0x8201, 0x8301, 0x8401, 0x8501, 0x8601, 0x8701, 0x8801, 0x8901

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1	CTX0	Ground Inactive Rx's	Dead time enabled	FOSC TX Freq	Vbias enable	PXS Mode		

- Bit 15: **CTx8**
  - 0: CTx8 disabled
  - 1: CTx8 enabled
- Bit 14: **CTx7**
  - 0: CTx7 disabled
  - 1: CTx7 enabled
- Bit 13: **CTx6**
  - 0: CTx6 disabled
  - 1: CTx6 enabled
- Bit 12: **CTx5**
  - 0: CTx5 disabled
  - 1: CTx5 enabled
- Bit 11: **CTx4**
  - 0: CTx4 disabled
  - 1: CTx4 enabled
- Bit 10: **CTx3**
  - 0: CTx3 disabled

  - 1: CTx3 enabled
- Bit 9: **CTx2**
  - 0: CTx2 disabled
  - 1: CTx2 enabled
- Bit 8: **CTx1**
  - 0: CTx1 disabled
  - 1: CTx1 enabled
- Bit 7: **CTx0**
  - 0: CTx0 disabled
  - 1: CTx0 enabled
- Bit 6: **Ground Inactive Rx’s**
  - 0: Inactive Rx floating
  - 1: Inactive Rx Grounded
- Bit 5: **Dead Time Enabled**
  - 0: Deadtime disabled
  - 1: Deadtime enabled
- Bit 4: **FOSC TX Frequency**
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Vbias Enabled**
  - 0: Vbias disabled
  - 1: Vbias enabled
- Bit 0-2: **PXS Mode**
  - 000: None
  - 001: Self-capacitive
  - 010: Mutual capacitive[i]
  - 011: Mutual inductance

Table A.12: Global Cycle Setup

Register: 0x8A00

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	Maximum counts		0	1	0	1	1	1	1	0	0	Auto Mode		1	1

- Bit 13-14: **Maximum counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16383
- Bit 2-3: **Auto Mode**
  - Number of conversions created before each interrupt is generated
  - 00: 4
  - 01: 8
  - 10: 16
  - 11: 32

Table A.13: Coarse and Fine Multipliers Preload

Register: 0x8A01

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Divider Preload					Reserved				Coarse Divider Preload				

- Bit 0-4: **Coarse Divider Preload**
  - 5-bit coarse divider preload value
- Bit 9-13: **Fine Divider Preload**
  - 5-bit fine divider preload value

---

[i] Please note that the maximum allowed charge transfer frequency (see Table A.8) for mutual capacitive mode is 1MHz i.e frequency period ≥ 7

Table A.14: ATI Compensation Preload

Register: 0x8A02

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved						ATI Compensation Preload									

- Bit 0-9: **ATI Compensation Preload**
  - 10-bit preload value

Table A.15: Channel Setup 0

Register: 0x9000, 0x9100, 0x9200, 0x9300, 0x9400, 0x9500, 0x9600, 0x9700, 0x9800, 0x9900, 0x9A00, 0x9B00, 0x9C00, 0x9D00, 0x9E00, 0x9F00, 0xA000 0xA100, 0xA200, 0xA300

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit				Enter				Proximity Threshold							

- Bit 12-15: **Exit Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 8-11: **Enter Debounce Value**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 0-7: **Proximity Threshold**
  - 8-bit value

Table A.16: Channel Setup 1

Register: 0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501, 0x9601, 0x9701, 0x9801, 0x9901, 0x9A01, 0x9B01, 0x9C01, 0x9D01, 0x9E01, 0x9F01, 0xA001, 0xA101, 0xA201, 0xA301

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Hysteresis								Touch Threshold							

- Bit 8-15: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold. Release threshold can be determined as follows:
  - $\frac{\text{LTA * Threshold bit value}}{2^8} - \frac{\text{Threshold bit value * Hysteresis bit value * LTA}}{2^{16}}$
- Bit 0-7: **Touch Threshold**
  - $\frac{LTA}{256} * 8\text{bit value}$

Table A.17: CRX Select and General Channel Setup (CH0 – CH9)

Register: 0xB000, 0xB100, 0xB200, 0xB300, 0xB400, 0xB500, 0xB600, 0xB700, 0xB800, 0xB900

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	ATI Band		Global halt	Invert	Dual	Enabled	CRX3	CRX2	CRX1	CRX0	Cs Size	Vref 0v5	Proj Bias Select	

- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with global halt enabled is in a prox or touch state.
  - 0: Global halt disabled
  - 1: Global halt enabled
- Bit 10: **Invert direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional sensing**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled

- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx3**
  - 0: CRx3 disabled
  - 1: CRx3 enabled
- Bit 6: **CRx2**
  - 0: CRx2 disabled
  - 1: CRx2 enabled
- Bit 5: **CRx1**
  - 0: CRx1 disabled
  - 1: CRx1 enabled
- Bit 4: **CRx0**
  - 0: CRx0 disabled
  - 1: CRx0 enabled
- Bit 3: **Cs Size**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **Vref 0.5V Enable**
  - Decrease internal sampling capacitor size
  - 0: Vref 0v5 disabled - C_S = Value chosen in Cs 80pF bit (40pF/80pF)
  - 1: Vref 0.5V enabled - C_S = Half of the value chosen in Cs 80pF bit (40pF/80pF)
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.18: CRX Select and General Channel Setup (CH10 – CH19)

Register: 0xBA00, 0xBB00, 0xBC00, 0xBD00, 0xBE00, 0xBF00, 0xC000, 0xC100, 0xC200, 0xC300

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	ATI Band		Global halt	Invert	Dual	Enabled	CRX7	CRX6	CRX5	CRX4	Cs Size	Vref 0v5	Proj Bias Select	

- Bit 12-13: **ATI band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with golbal halt enabled, is in a prox/touch state. The function is aimed at slider/ wheel applications
  - 0: Halt disabled
  - 1: Halt enabled
- Bit 10: **Invert Direction**
  - If this bit is enabled, the direction in which a touch will be triggered, is inverted. Bit must be enabled for mutual capacitive mode
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional sensing**
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx7**
  - 0: CRx7 disabled
  - 1: CRx7 enabled
- Bit 6: **CRx6**
  - 0: CRx6 disabled

  - 1: CRx6 enabled
- Bit 5: **CRx5**
  - 0: CRx5 disabled
  - 1: CRx5 enabled
- Bit 4: **CRx4**
  - 0: CRx4 disabled
  - 1: CRx4 enabled
- Bit 3: **Cs Size**
  - 0: 40pF
  - 1: 80pF
- Bit 2: **Vref 0.5V Enable**
  - Decrease internal sampling capacitor size
  - 0: Vref 0.5V disabled - C_S = Value chosen in Cs 80pF bit (40pF/80pF)
  - 1: Vref 0.5V enabled - C_S = Half of the value chosen in Cs 80pF bit (40pF/80pF)
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.19: ATI Base and Target

Register: 0xB001, 0xB101, 0xB201, 0xB301, 0xB401, 0xB501, 0xB601, 0xB701, 0xB801, 0xB901, 0xBA01, 0xBB01, 0xBC01, 0xBD01, 0xBE01, 0xBF01, 0xC001,0xC101,0xC201, 0xC301

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target								ATI Base					ATI Mode		

- Bit 8-15: **ATI Target**
  - 8-bit value * 8
- Bit 3-7: **ATI Base**
  - 5-bit value * 16
- Bit 0-2: **ATI Mode**
  - 000: ATI Disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI

Table A.20: Fine and Coarse Multipliers

Register: 0xB002, 0xB102, 0xB202, 0xB302, 0xB402, 0xB502, 0xB602, 0xB702, 0xB802, 0xB902, 0xBA02, 0xBB02, 0xBC02, 0xBD02, 0xBE02, 0xBF02, 0xC002,0xC102,0xC202, 0xC302

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.21: ATI Compensation

Register: 0xB003, 0xB103, 0xB203, 0xB303, 0xB403, 0xB503, 0xB603, 0xB703, 0xB803, 0xB903, 0xBA03, 0xBB03, 0xBC03, 0xBD03, 0xBE03, 0xBF03, 0xC003,0xC103,0xC203, 0xC303

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value

- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.22: Filter Betas

Register: 0xC400

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Low Power Beta				LTA Normal Power Beta				Counts Low Power Beta				Counts Normal Power Beta			

- Bit 12-15: **LTA Low Power Beta Filter Value**
  - 4-bit value
- Bit 8-11: **LTA Normal Power Beta Filter Value**
  - 4-bit value
- Bit 4-7: **Counts Low Power Beta Filter Value**
  - 4-bit value
- Bit 0-3: **Counts Normal Power Beta Filter Value**
  - 4-bit value

Table A.23: Fast Filter Betas

Register: 0xC401

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

- Bit 4-7: **LTA Low Power Fast Beta Filter Value**
  - 4-bit value
- Bit 0-3: **LTA Normal Power Fast Beta Filter Value**
  - 4-bit value

Table A.24: Control Settings

Register: 0xD0

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Interface type		Power mode		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 6-7: **Interface Selection**
  - 00: I^{2}C streaming
  - 01: I^{2}C event mode
  - 10: I^{2}C Stream in touch
- Bit 4-5: **Power Mode Selection**
  - 00: Normal power
  - 01: Low power
  - 10: Ultra-low Power
  - 11: Automatic power mode switching
- Bit 3: **Execute Reseed Command**
  - 0: Do not reseed
  - 1: Reseed
- Bit 2: **Execute ATI Command**
  - 0: Do not ATI
  - 1: ATI
- Bit 1: **Soft Reset**
  - 0: Do not reset device
  - 1: Reset device
- Bit 0: **Acknowledge Reset Command**
  - 0: Do not acknowledge reset
  - 1: Acknowledge reset

Table A.25: Event Timeouts

Register: 0xD9

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Touch Event Timeout								Prox Event Timeout							

- Bit 8-15: **Touch Event Timeout**
  - 8-bit value * 500 ms
  - 0: Never timeout (Required for ULP entry channels retaining an active state in ULP)
- Bit 0-7: **Proximity Event Timeout**
  - 8-bit value * 500 ms
  - 0: Never timeout

Table A.26: Event Enable

Register: 0xDA

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Power event	ATI event	Reserved										Touch event	Prox event

- Bit 13: **Power Event**
  - 0: Power event masked
  - 1: Power event enabled
- Bit 12: **ATI Event**
  - 0: ATI event masked
  - 1: ATI event enabled
- Bit 1: **Touch Event**
  - 0: Touch event masked
  - 1: Touch event enabled
- Bit 0: **Prox Event**
  - 0: Prox event masked
  - 1: Prox event enabled

Table A.27: I^{2}C Communication

Register: 0xDB

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														RW check disabled	Stop bit disabled

- Bit 1: **RW Check Disabled**
  - 0: Write not allowed to read only registers
  - 1: Read and write allowed to read only registers
- Bit 0: **Stop Bit Disabled**
  - 0: I^{2}C communication window terminated by stop bit
  - 1: I^{2}C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window

Table A.28: I^{2}C Communication Timeout

Register: 0xDC

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I^{2}C Communication Timeout															

- Note: To write to this register, the register's address (0xDC) must be commanded explicitly before writing data i.e. in a separate I^{2}C write setup command.
- Bit 0-15: **I^{2}C Communication Timeout**
  - 16-bit value [ms]
  - Default = 500 ms
  - Range: 0 - 65535 ms

B Known Issues

B.1 I^{2}C Polling During Start-up

V1.43 and earlier

Polling during start-up may result in device lockup. Suspend polling for at least 25ms after receiving a NACK.

The I^{2}C initialize can fail if one of the I^{2}C lines have been kept low for longer than 50ms.

B.2 ATI Power Mode Issue

- When signal drift is present in a low-power mode, an auto-ATI event is possible to ensure the signal is in an optimal operating range.
- In order code version "201", "202" and above, the auto-ATI event will wake the IC from LP or ULP mode, causing it to spend the preset times to step down to low power modes again. In cases where significant signal drift is expected, this effect could affect battery life calculations.
- For optimal battery life it is recommended to use the ATI events to manually put the IC back into the lowest power mode and reinstate auto power modes after that. Please contact Azoteq for sample code to achieve this.

B.3 Force Communication Request may Close a Communication Window

A force communication request (0xFF command) may unintentionally close a communication window instead of opening it. This occurs if the IQS7222A receives the force communication request while the RDY is low. The I^{2}C STOP condition at the end of the 0xFF byte triggers the IQS7222A to close its communication window, causing the RDY to go back high immediately. This may also happen if the communication window automatically opens during the transmission of the 0xFF byte, as shown in Figure B.1.

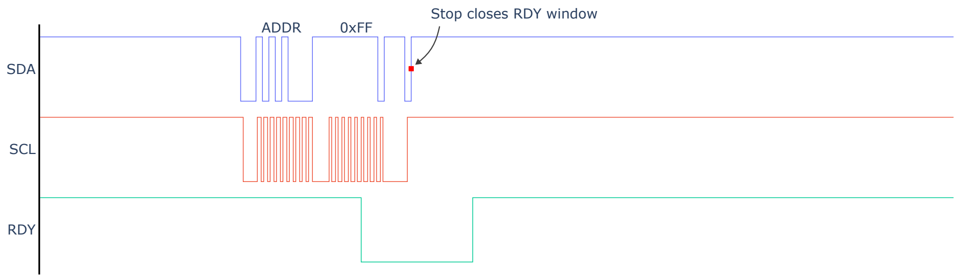

Figure B.1: Force Communication Closing a Communication Window

As a result, the MCU may observe the RDY pin change, and then attempt to communicate with the IC as soon as the force communication transaction is complete. This will cause the IQS7222A to respond with the error code 0xEE.

The following protocol can be used to minimise the likelihood of this error condition.

Step 1: Before sending the 0xFF command, read the state of the RDY pin and verify that it is high (the communication window is closed). If the RDY pin is already low, the communications window is open and can be handled as normal.
Step 2: If the RDY pin is high, issue the force communication I^{2}C command.

Step 3: As soon as the I^{2}C transmission of the force communication command has started, wait for the RDY window.

Step 4: Once the RDY is received, the MCU should wait at least 300 µs, then re-check the state of the RDY pin.

  (a) If the RDY pin is high, then the window was closed due to the STOP condition. Re-issue the 0xFF command, repeating the above procedure.
  (b) If the RDY pin is low, the communication window is still open, and normal I^{2}C operations may resume.

Figure B.2 shows an example of this process. The first force communication request occurred simultaneously with a RDY window, and the RDY window was closed due to the STOP condition. The MCU detected the RDY window, waited 300 µs, then checked the RDY pin state. The pin was HIGH, and the force communication request was repeated.

The second request opened the RDY window after some time, and the MCU waited 300 µs again before checking the RDY pin state. The RDY was low, and normal communication could continue.

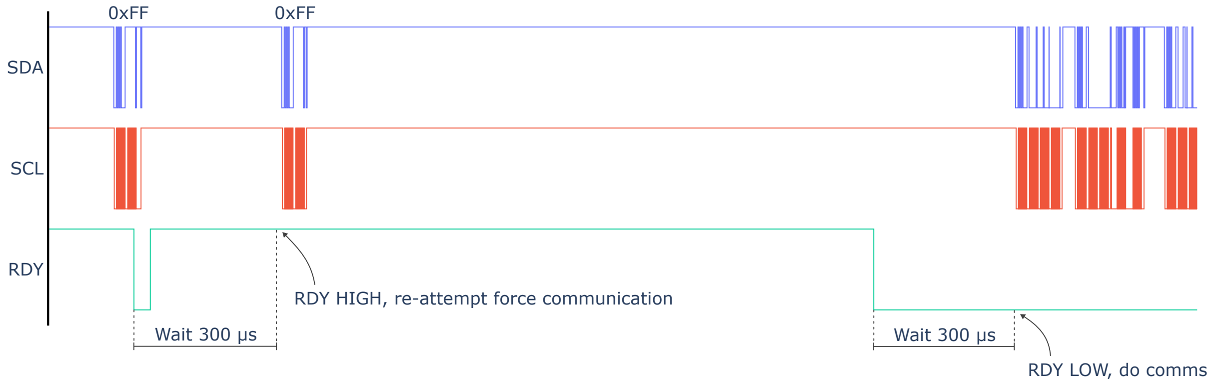

Figure B.2: Force Communication With RDY Check

B.4 Force Communication Request May Be Missed

There is a possibility of a force communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period (described in Section 8.8.2). However, it is essential to retry at different timings that are not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional recovery mechanism, the IC can be reset using the MCLR pin and reinitialised if there is no response after a specified number of retries.

C Revision History

Release	Date	Changes
v0.3	April 2021	› Initial release
v1.0	January 2022	› Tape and Reel information added › Firmware version changed to v1.45 › Bit definition for Read-write check corrected › Changed Communication protocol description › Read-write permissions added in memory map › Stop-bit disable bit definition corrected › Revision history added › Force communication section added › Register 0xDC added
v1.1	April 2022	› VREGA electrical characteristics corrected › Bit and register names changed to follow user guide and GUI conventions › Example of h file from GUI and program flow diagram added. › 14MHz option and order code 102 added › VDD capacitor values updated on reference schematic
v1.2	March 2023	› Firmware version updated to v1.46/v1.47 › Added order code 201 and 202 › Changes implemented for IQS7222B 201 and 202 IC options according to "PIN-230172" › Updated current consumption tables › Updated capacitive channels section › Updated power mode and mode timeout section › Removed QFR option › Update Memory Map version information table › Memory Map reserved bits corrected
v1.3	May 2024	› Added QFR option › Updated Force communication section › Added ATI-low power known issue › Fixed incorrect product number
v1.4	Febuary 2026	› Overhauled ProxFusion Module section, expanding descriptions and including a list of all relevant settings › Re-ordered I^{2}C Interface section › Added recommended Conversion Frequency settings to Memory Map Descriptions › Removed ATI Active from Program Flow Diagram › Added Default Values to Memory Map Register › Updated Tape and Reel drawings to include additional dimensions › Removed all GPIO labels from Reference Schematics and Block Diagram › Added known issues regarding I^{2}C force communication › Corrected Digital I/O Characteristics

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