IQS7222A DATASHEET

12-channel mutual-/self-capacitive, inductive, and Hall sensing controller with I²C communications interface and low power options

1 Device Overview

The IQS7222A ProxFusion® IC is a sensor fusion device for applications that require multiple sensing capabilities from a single sensor IC. The sensor is fully I²C compatible, and on-chip calculations enable multiple application options. Various UIs, from gestures to power mode switching, allow the IC to respond effectively in the intended application with ultra-low power consumption.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) / 8 (WLCSP) external sensor pad connections
- Self-/Mutual capacitive sensors configuration for display wake-up
- ULP wake-up on touch
  - Dedicated ultra-low-power wake-up touch sensor
- Configure up to 12[i] Channels using the external connections or internal sensor
- External sensor options:
  - Up to 8 self-capacitive buttons
  - Up to 4 self-capacitive wear detection pairs (with physical reference)
  - Up to 10 mutual capacitive touch/proximity sensors
  - Up to 4 inductive sensor elements (metal detection/force sensing)
- Internal sensor options:
  - Hall Switch[ii]
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Active environment tracking with reference sensor
  - Debounce and Hysteresis
  - Dual direction trigger indication
- Built-in Signal processing options:
  - Slider output
  - Up to 4 elements per slider
  - Up to 2 sliders simultaneously
  - Slider gesture outputs
- Design simplicity:
  - PC software for debugging and obtaining optimal settings and performance
  - One-time programmable settings for custom power-on IC configuration
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I²C communication interface with IRQ/RDY (up to Fast-Mode Plus – 1 MHz)
- Event and streaming modes
- Configurable dedicated output pin
- Supply Voltage 1.71 V to 3.6 V
- Package options:
  - WLCSP18 (1.62 x 1.62 x 0.5 mm) - interleaved 0.4 mm x 0.6 mm ball pitch
  - QFN20 (3 x 3 x 0.5 mm) - 0.4 mm pitch

QFN20 Package

WLCSP18 Package

1.2 Applications

- SAR Compliance in Mobile devices.
- Low power wakeup events on proximity or touch.
- User interfaces:
  - Capacitive sliders
  - Capacitive buttons
  - Inductive buttons
  - Can be made waterproof
- Wear Detection.
- Hall-effect Dock Detection.
- TWS Earphones:
  - Touch controls
  - Slider with gestures
  - Wear detection
  - Force/squeeze controls
  - Hall-effect dock detection

1.3 Block Diagram

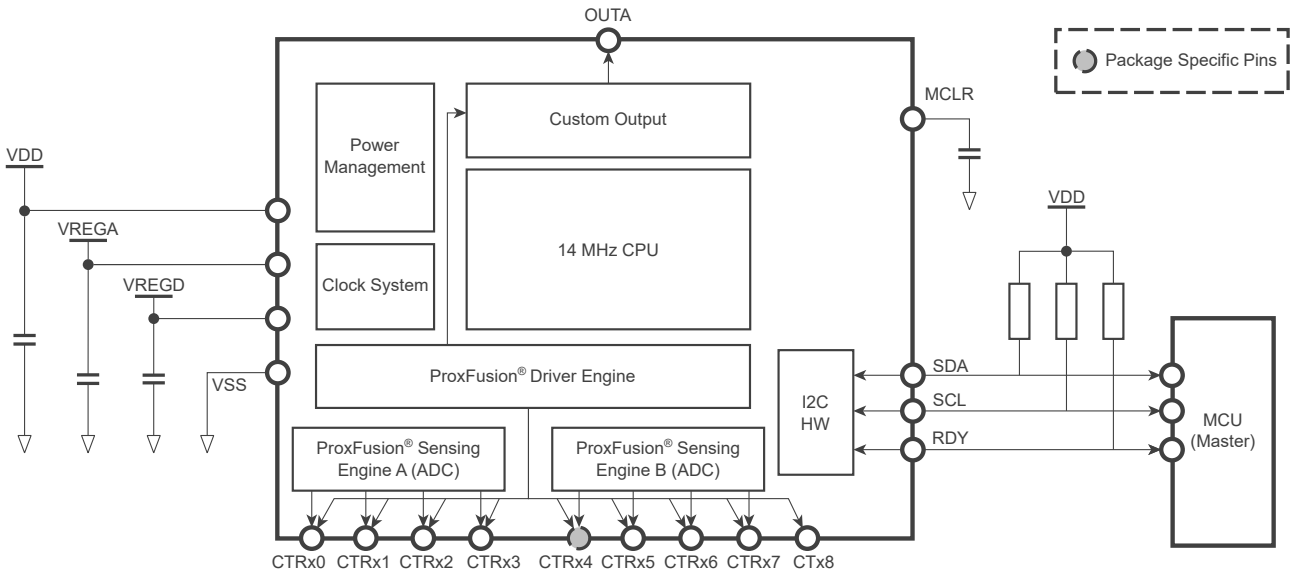


Figure 1.3: Functional Block Diagram[iii]

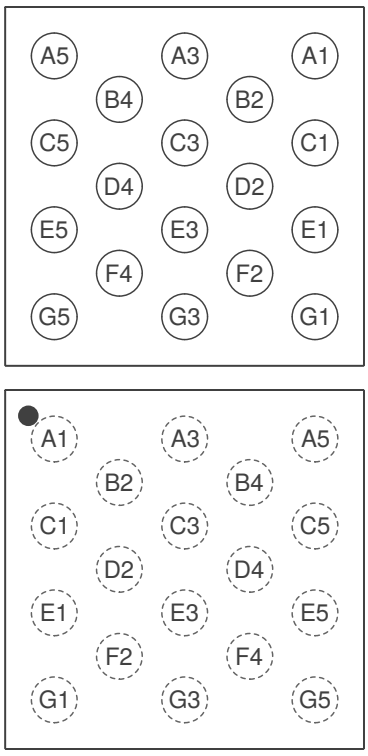
[i] WLCSP18 package has 1 less external pad connection and the maximum amount of buttons that can be configured are less than QFN20 package.
[ii] IQS7222E is recommended for complex HALL switch applications. IQS7222A is ideal for detecting relative changes.
[iii] WLCSP18 packages do not have a CRX4 pin.

Contents

2 Hardware Connection

2.1 WLCSP18 Pin Diagrams

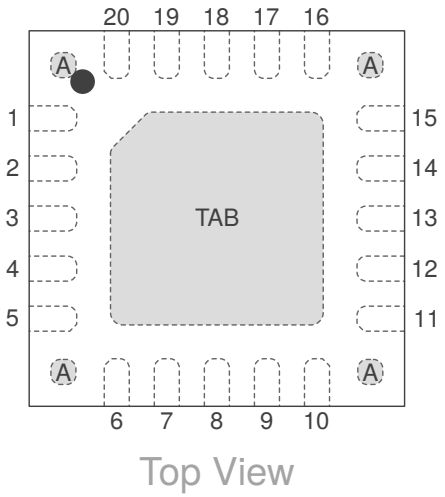
Table 2.1: 18-pin WLCSP18 Package



Pin no.	Signal
A1	OUTA
A3	SCL
A5	MCLR
B2	NC
B4	SDA
C1	CTx8
C3	RDY
C5	VDD
D2	CRx2/CTx2
D4	VSS
E1	CRx6/CTx6
E3	CRx1/CTx1
E5	VREGD
F2	CRx5/CTx5
F4	CRx0/CTx0
G1	CRx7/CTx7
G3	CRx3/CTx3
G5	VREGA

2.2 QFN20 Pin Diagram

Table 2.2: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8
4	VREGA	14	OUTA
5	CRx0/CTx0	15	NC
6	CRx1/CTx1	16	NC
7	CRx2/CTx2	17	RDY
8	CRx3/CTx3	18	SCL
9	CRx4/CTx4	19	SDA
10	CRx5/CTx5	20	MCLR

Area name	Signal name
TAB[i]	Thermal pad (floating)
A[ii]	Thermal pad (floating)

[i] It is recommended to connect the thermal pad (TAB) to VSS.
[ii] Electrically connected to TAB. These exposed pads are only present on *–QNR* order codes.

2.3 Pin Attributes

Table 2.3: Pin Attributes

Pin no.		Signal name	Signal type	Buffer type	Power source
WLCSP18	QFN20				
C5	1	VDD	Power	Power	N/A
E5	2	VREGD	Power	Power	N/A
D4	3	VSS	Power	Power	N/A
G5	4	VREGA	Power	Power	N/A
F4	5	CRx0/CTx0	Analog		VREGA
E3	6	CRx1/CTx1	Analog		VREGA
D2	7	CRx2/CTx2	Analog		VREGA
G3	8	CRx3/CTx3	Analog		VREGA
-	9	CRx4/CTx4	Analog		VREGA
F2	10	CRx5/CTx5	Analog		VREGA
E1	11	CRx6/CTx6	Analog		VREGA
G1	12	CRx7/CTx7	Analog		VREGA
C1	13	CTx8	Analog		VREGA
A1	14	OUTA	Digital		VREGA/VDD
B4	19	SDA	Digital		VDD
A3	18	SCL	Digital		VDD
-	15	NC	-		-
B2	16	NC	-		-
C3	17	RDY	Digital		VDD
A5	20	MCLR	Digital		VDD

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal name	Pin no.		Pin type[iii]	Description
		WLCSP18	QFN20		
ProxFusion®	CRx0/CTx0	F4	5	IO	ProxFusion® channel
	CRx1/CTx1	E3	6	IO	
	CRx2/CTx2	D2	7	IO	
	CRx3/CTx3	G3	8	IO	
	CRx4/CTx4	-	9	IO	
	CRx5/CTx5	F2	10	IO	
	CRx6/CTx6	E1	11	IO	
	CRx7/CTx7	G1	12	IO	
	CTx8	C1	13	O	CTx8 pad
GPIO	OUTA	A1	14	O	Configurable digital output
	NC	-	15	-	Not Connected
	NC	B2	16	-	Not Connected
	RDY	C3	17	O	RDY pad
	MCLR	A5	20	I	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP.
I^2C	SDA	B4	19	IO	I^2C data
	SCL	A3	18	IO	I^2C clock
Power	VDD	C5	1	P	Power supply input voltage
	VREGD	E5	2	P	Internal regulated supply output for digital domain
	VSS	D4	3	P	Analog/digital ground
	VREGA	G5	4	P	Internal regulated supply output for analog domain

[iii] Pin Types: I = Input, O = Output, IO = Input or Output, P = Power.

2.5 Reference Schematic

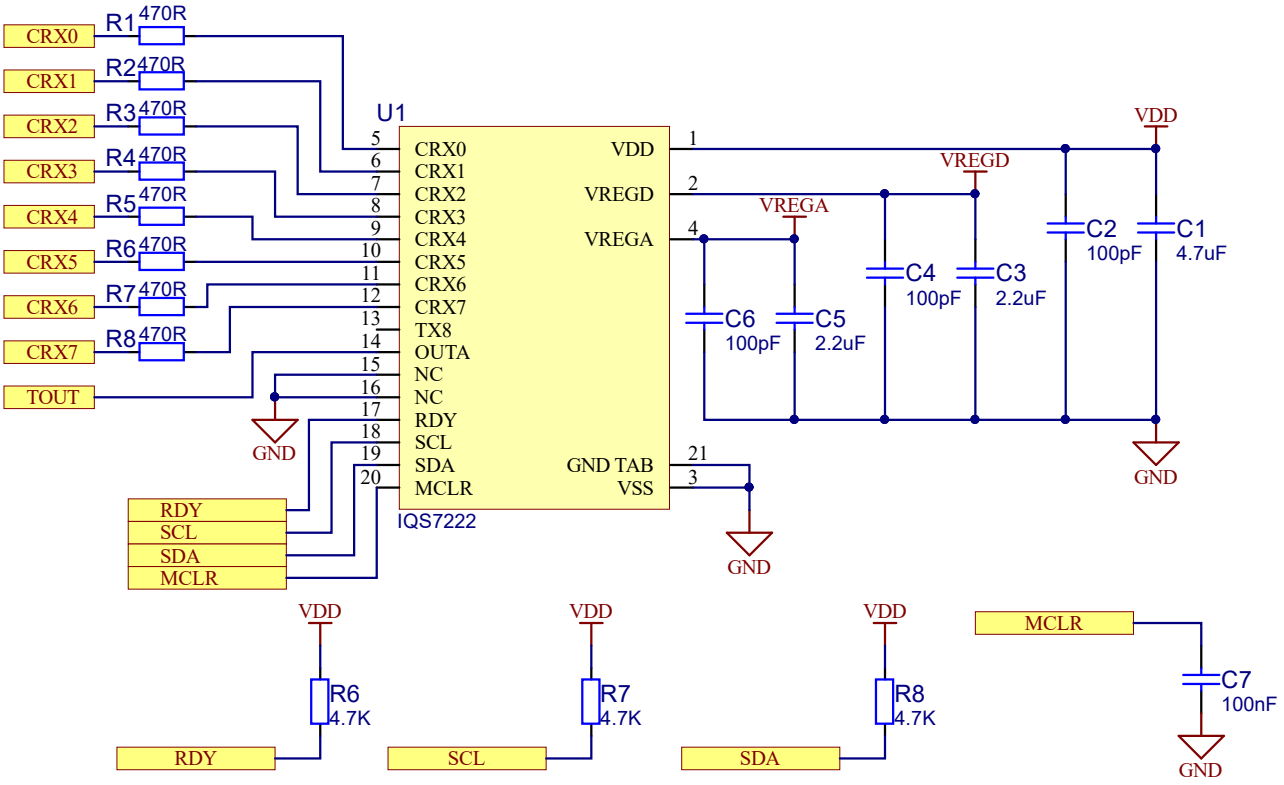


Figure 2.1: 8 Button Self Capacitance Reference Schematic

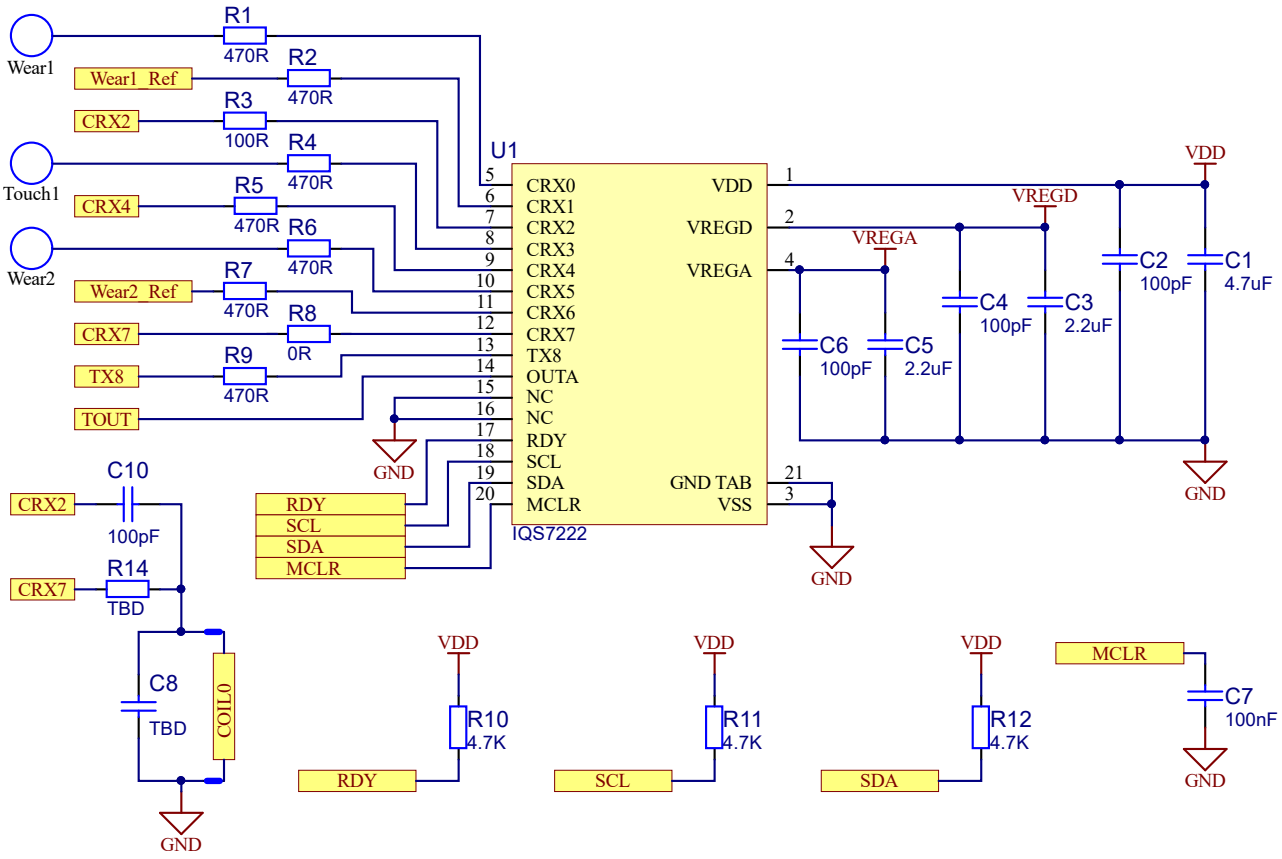


Figure 2.2: Wear, Reference and Inductive Sensing Reference Schematic

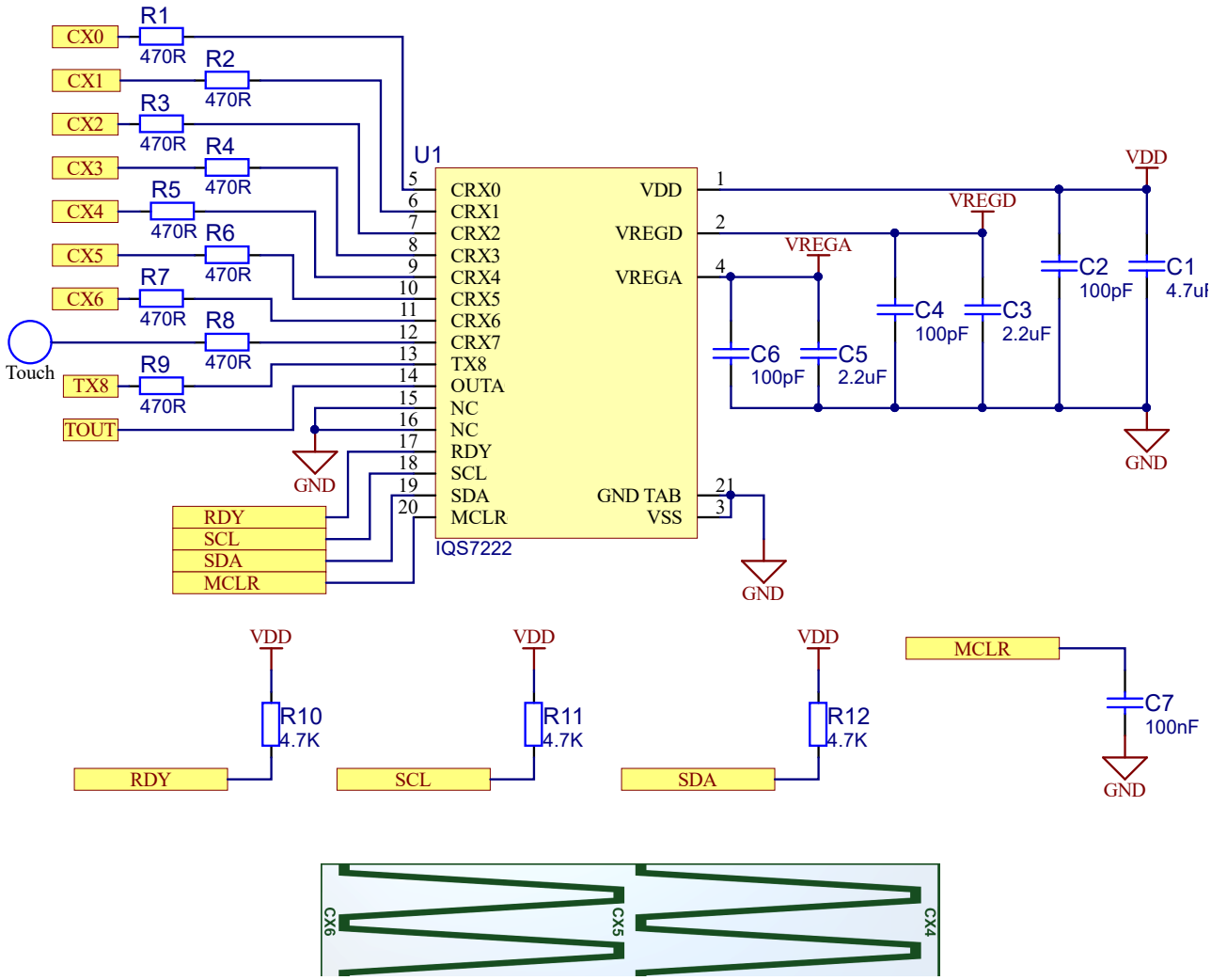


Figure 2.3: 3 Channel Slider with Touch Sensor Reference Schematic

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin (referenced to VSS)	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	–40	85	°C

3.2 Recommended Operating Conditions

Table 3.2: Recommended Operating Conditions

		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: f_{OSC} = 14 MHz	1.71		3.6	V
VREGA	Internal regulated supply output for analog domain: f_{OSC} = 14 MHz	1.49	1.53	1.57	V
VREGD	Internal regulated supply output for digital domain: f_{OSC} = 14 MHz	1.56	1.59	1.64	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREGA}$	$3\times C_{VREGA}$		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR $\leq$ 200 mΩ	2[i]	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1		400[ii]	pF
$Cm_{CTx–CRx}$	Capacitance between receiving and transmitting electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.2		9[ii]	pF
$Cp_{CRx–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode at f_{xfer} = 1 MHz)			100[ii]	pF
$\frac{Cp_{CRx–VSS}}{Cm_{CTx–CRx}}$	Capacitance ratio for optimal SNR in mutual-capacitance mode[iii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iv]	0.47	10[v]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iv]	0.47	10[v]	kΩ

3.3 ESD Rating

Table 3.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[vi]	±4000	V

3.4 Current Consumption

Table 3.4: Typical Current Consumption for Order Code 001

Power mode	Active channels	Report rate	Current [µA]	
		(Sampling rate) [ms]	3.3 V	1.8 V
NP	Defaults (10 channels self-capacitance & Hall)	16	450	445
	TWS: Wear, slider, inductive resonant without bias, Hall	16	484	480
LP	Defaults (10 channels self-capacitance & Hall)	60	126	124
	TWS: Wear, slider, inductive resonant without bias, Hall	60	126	125
ULP	Distributed (2 self-capacitance auto-prox channels), default setup	150	6.7	6.1
	Distributed (2 self-capacitance auto-prox channels), TWS setup	150	5.8	5.5

Table 3.5: Typical Current Consumption for Order Code 102

Power mode	Active channels	Report rate	Current [µA]	
		(Sampling rate) [ms]	3.3 V	1.8 V
NP	Defaults (10 channels self-capacitance & Hall)	16	426	421
LP	Defaults (10 channels self-capacitance & Hall)	60	110	107
ULP	Distributed (2 self-capacitance auto-prox channels), default setup	150	9.8	9.6

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.
[ii] RCx = 0 Ω.
[iii] Please note that the maximum values for Cp and Cm are subject to this ratio.
[iv] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.
[v] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times f_{xfer})}$ where C is the pin capacitance to VSS.
[vi] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

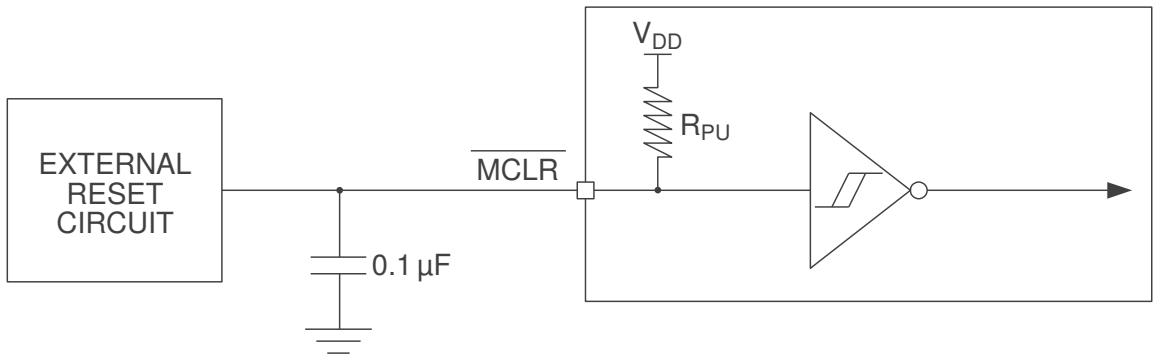


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	55	500 – 1500	7000	kHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions[i]	Min	Max	Unit
V_{OL}	Output low voltage of SDA and SCL pins	I_{OL} = 20 mA $V_{DD} > 2$ V		0.4	V
		I_{OL} = 20 mA $V_{DD} \leq 2$ V		0.2 V_{DD}	
	Output low voltage of SDA and SCL pins in GPIO output mode	I_{OL} = 10 mA		0.1 V_{DD}	
	Output low voltage of MCLR	I_{OL} = 5 mA			
	Output low voltage of any other GPIO pin	I_{OL} = 10 mA			
V_{OH}	Output high voltage	I_{OH} = −5 mA	0.9 V_{DD}		V
V_{IL}	Input low voltage		V_{SS} − 0.3	0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}	V_{DD} + 0.3	V
C_b	SDA and SCL bus capacitance			550	pF

[i] Standard operating conditions:
V_{DD}: 1.8 V to 3.6 V, unless otherwise stated.
Operating temperature: −20 °C to 80 °C.

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

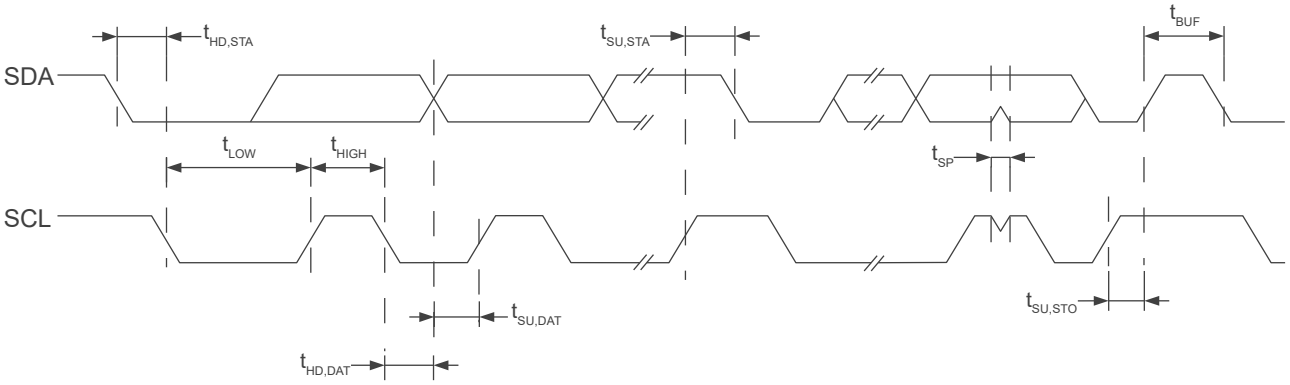


Figure 4.2: I^2C Mode Timing Diagram

5 ProxFusion® Module

The IQS7222A contains dual ProxFusion® modules which use patented technology to measure and process relative changes in capacitive, inductive, and Hall sensors. It supports up to 12 sensing channels. The two modules allow for simultaneous sensing of two channels at a time, ensuring a rapid response from multi-channel implementations. Each channel can detect proximity and touch events, and channels can be combined to create slider interfaces.

5.1 Overview

Self-capacitance, mutual capacitance, reference tracking, inductive designs and Hall-effect sensing are possible with the IQS7222A.

Please refer to the following application notes for more information:

- AZD004: Azoteq Sensing Technology
- AZD125: Capacitive Sensing Design Guide
- AZD036: Mutual Capacitance Button Layout Guide
- AZD115: Inductive Sensing Design Guide
- AZD137: User Interfaces Application Note

5.2 Counts

Each ProxFusion module reports a sensing measurement as a relative, unit-less value referred to as “Counts”, which are stored as *16-bit values*. These counts report the number of charge transfer cycles necessary to charge an internal sampling capacitor, and are typically inversely proportional to the signal measured on the external sensor. Count values are thus inversely proportional to capacitance/inductance. All further outputs are derived from these counts values.

User interaction is detected by comparing the measured count values to some reference value. The reference value, known as the *Long-Term Average* (LTA), is slowly updated using a low-pass filter to track changes in the environment. Detected proximity and touch events are then reported for each channel in the *Proximity* and *Touch* Event registers.

5.3 Cycle and Channel Relationship

The IQS7222A has 2 Prox engines, A and B, that perform sensing simultaneously. Sensing is performed across 7 time slots, labelled cycle 0 to cycle 6, where each cycle is associated with two channels, one for each Prox engine. The relationship between the cycles and channels is shown in Table 5.1 below. Cycle 5 and Cycle 6 (channel 10 and channel 11, respectively) are reserved for Hall-effect sensing, as described in Section 5.7.

Table 5.1: Cycle and Channel Relationship

Cycle	Channel on Prox Engine A	Channel on Prox Engine B
Cycle 0	Channel 0	Channel 5
Cycle 1	Channel 1	Channel 6
Cycle 2	Channel 2	Channel 7
Cycle 3	Channel 3	Channel 8
Cycle 4	Channel 4	Channel 9
Cycle 5	-	Channel 10
Cycle 6	-	Channel 11

ProxFusion sensing settings can be either channel-specific or cycle-specific (i.e. applies to both channels in the same cycle). It is important to note that both channels of a particular cycle must use the same sensing mode (self-capacitance, inductive, etc). Refer to Section 5.8.1 for a list of cycle-specific settings, and Section 5.8.2 for a list of channel-specific settings.

5.4 ProxFusion Hardware Settings

5.4.1 Sensing Mode

Each channel can be independently enabled via the *Channel Enable* bit of the respective channel's *General Channel Setup* register. Additionally, the sensing mode (or *PXS Mode*) of the channel must be specified for the associated cycle in the *Cycle Setup 1* register. Cycle and channel associations are given in Table 5.1.

5.4.2 Rx and Tx Selection

Each sensor must have an associated Rx and Tx selected. Tx pins are assigned per cycle in the *Cycle Setup 1* register, while Rx pins are assigned per channel in the *CRX Select* register.

While any pin may be used as Tx for either prox engine, only certain pins may be used as Rx for each prox engine, as shown in Table 5.2

Table 5.2: Rx Prox Engine Relationship

CRx	Prox Engine A	Prox Engine B
CRx0	✓	-
CRx1	✓	-
CRx2	✓	-
CRx3	✓	-
CRx4	-	✓
CRx5	-	✓
CRx6	-	✓
CRx7	-	✓

Additional notes:

- For self-capacitive sensors, both Rx and Tx must be assigned to the same pin.
- Rx and Tx pin assignments are not required for Hall-effect sensing.

5.4.3 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}), also known as the conversion frequency, is set using the *Conversion Frequency Fraction* and *Conversion Frequency Period* fields in the *Cycle Setup 0* register. This frequency is derived from the system clock, f_{OSC}.

For capacitive sensing, a lower frequency allows the capacitive electrode to charge and discharge completely. For inductive sensing, this frequency should be selected based on the resonant frequency of the LC circuit, unless *FOSC Tx Frequency* is used. Lower frequencies may provide more stable measurements, but increase sensing duration and current consumption. For Hall-effect channels, the highest frequency (7 MHz) is recommended.

It is recommended to always set the *Conversion Frequency Fraction* to '127' and to select the conversion frequency with the *Conversion Frequency Period*. Please refer to Tables A.1 and A.2 to select suitable *Conversion Frequency Period* values for the desired conversion frequency.

The *Dead Time Enable* option in the *Cycle Setup 1* register must be considered when setting the conversion frequency. Dead time should always be enabled for capacitance measurements, and disabled for inductive measurements.

5.4.4 FOSC Tx Frequency

The *FOSC Tx Frequency* setting in the *Cycle Setup 1* register enables f_{OSC} (14 MHz) as output on the associated Tx pins during sensing.

This can be used to excite resonated inductive sensors at a frequency higher than can be achieved using the charge transfer frequency. This is beneficial for certain inductive sensing applications, but is not supported for capacitive sensing.

5.4.5 Maximum Counts

The *Maximum Counts* setting in the *Global Cycle Setup* register sets the maximum counts value that the Proxfusion engine will allow a particular measurement or channel to reach. This acts as a timeout, stopping the measurement early if the sensing takes too long to complete. The resulting counts stored for that measurement will be set to the maximum counts value. Available values are:

- 1023 counts
- 2047 counts
- 4095 counts
- 16383 counts

The maximum counts should be increased if a high target value is used on a particular channel. (For example, 2047 or 4095 should be used for a channel with a target of 1000). However, this may (situationally) increase current consumption and increase ATI duration.

5.4.6 Cs Size

The *Cs Size* setting in the *CRX Select and General Channel Setup* register sets the size of the internal sampling capacitor to either 40 pF or 80 pF. It is recommended to use the 80 pF capacitor wherever possible. However, the 40 pF capacitor requires only half the amount of charge to reach its threshold voltage, and may therefore be used in designs where the load/signal is very small.

The effective size of the internal sampling capacitor may be further reduced by enabling *Vref 0.5 V Enable* in the *CRX Select and General Channel Setup* register. This setting lowers the threshold voltage on the sampling capacitor. It is recommended to keep this disabled.

5.5 ProxFusion UI Settings

5.5.1 Filtering

Raw counts obtained from the ProxFusion engines are filtered using a low-pass IIR filter to reduce the high-frequency noise in the measurement. The response of the filter can be adjusted with the *Filter Beta* values. Higher beta values result in a slower filter response, with less noise on the measurement. Note that the selected filter beta values apply to all channels.

Separate beta values are used for normal power and lower power modes. It may be beneficial to use a lower beta value for low power modes, which have lower sampling rates, in order to maintain responsiveness to user inputs.

Each beta setting is a 4-bit value, with a range of '0' – '15', where '0' is no filtering, and '15' is maximum filtering. Counts filtering typically uses low values, under '3', to ensure responsiveness.

5.5.2 Long Term Average

The *Long Term Average* (LTA) is derived from the *filtered counts*, and acts as a stable reference value. While the channel is not in activation, the LTA is slowly updated to track changes in the environment using a low-pass filter. During activation, the LTA is kept fixed (halted). The LTA filter response is controlled by the *LTA Beta* values. LTA beta values should typically be '8' or higher.

The difference between the filtered counts and the LTA is stored as the Delta value. The IQS7222A uses this delta value to detect proximity and touch activations.

$$\text{Delta} = \text{LTA} - \text{Counts} \tag{1}$$

5.5.3 Reseed

The *Reseed* function of the device will replace the filtered counts and the LTA value of the channel with the latest sampled raw counts value to reset the environmental reference of the channel. This may be necessary in certain instances when a channel gets incorrectly stuck in an activation.

The *Reseed* command can be given manually by setting the corresponding bit in the *Control Settings* register.

5.5.4 Proximity Event

A proximity event occurs on a channel when the *Delta* exceeds the *Proximity Threshold*, which is set in the *Button Setup 0* register.

To reduce jitter and false events, debouncing is applied to the channel when the delta initially crosses the proximity threshold. Debouncing forces the IQS7222A to perform a number of quick measurements, checking that all measurements exceed the threshold. The number of high-frequency measurements that are executed during debouncing is controlled by the *Button Setup 0* register, and can be configured independently for entering or exiting proximity events. Setting the debounce values to '0' or '1' will disable debouncing.

The proximity threshold and debouncing settings can be configured separately for each channel. An active proximity activation is indicated in the *Proximity Event States* register.

5.5.5 Touch Event

A touch event occurs on a channel when the delta exceeds the touch threshold. The touch threshold is calculated on-chip as a function of the LTA and an 8-bit *Touch Threshold* value stored in the *Button Setup 1* register.

$$\text{T}_{\text{counts}} = \frac{\text{T}_{\text{reg}} \times \text{LTA}}{256} \tag{2}$$

where

- T_{reg} is the 8-bit value stored in the *Touch Threshold* setting, and
- T_{counts} is the resulting threshold value in counts (rounded down).

Touch enter and exit events are not debounced. However, hysteresis is applied on touch release in order to reduce jitter. The size of the hysteresis is controlled by the *Hysteresis* setting in the *Button Setup 1* register, and its value in counts (H_{counts}) is calculated as

$$H_{counts} = \frac{H_{reg} \times T_{counts}}{256} \tag{3}$$

where T_{counts} is obtained from Equation (2), and H_{reg} is the 8-bit *Hysteresis* setting value.

Therefore, taking on-chip integer division into account, the touch "exit" threshold can be calculated as

$$\text{Exit Threshold (counts)} = \text{floor}\left(\frac{\text{LTA} \times \left(T_{reg} - \text{floor}\left(\frac{T_{reg} \times H_{reg}}{256}\right)\right)}{256}\right). \tag{4}$$

For example, assume an LTA value of 500, threshold setting of '20', and a hysteresis setting of '50'. The touch enter threshold in counts is calculated as

$$T_{enter(counts)} = \text{floor}\left(\frac{20 \times 500}{256}\right) = 39 \text{ counts},$$

and the exit threshold is calculated as

$$T_{exit(counts)} = \text{floor}\left(\frac{500 \times \left(20 - \text{floor}\left(\frac{20 \times 50}{256}\right)\right)}{256}\right) = 33 \text{ counts}.$$

5.5.6 Event Direction

Negative delta values are typically ignored, as they typically indicate an unexpected decrease in signal. This can occur due to sudden environmental changes, or due to the user releasing the sensor after the sensor was calibrated while in a touch state. Proximity and touch events are therefore only registered if the delta is positive, or

$$\text{Counts} < \text{LTA} - \text{Threshold}. \tag{5}$$

When a large negative delta is detected, the IQS7222A switches the LTA filter beta to the Fast LTA beta, which can be configured to track the counts more quickly to exit the negative delta state.

This behaviour can be modified with the following settings from the *CRX Select and General Channel Setup* register:

- The *Invert* bit changes the sign of the delta, so events are set when

$$\text{Counts} > \text{LTA} + \text{Threshold}. \tag{6}$$

  This is required for mutual capacitive sensing and inductive sensing.
- Bi-directional sensing ignores the sign of the delta, so that events are detected for either positive or negative deltas. The Fast LTA beta is never used.

5.5.7 Event Timeouts

In order to prevent stuck states where a channel is incorrectly stuck in a proximity or touch event (when the LTA filter is halted), the IQS7222A provides timeouts for proximity and touch events. The duration of these timeouts are controlled by the *Proximity Event Timeout* and *Touch Event Timeout* values in the *Button Setup 2* register, and can be set in 500 ms increments. Once the timeout duration expires, the channel is automatically reseeded.

Event timeouts can be configured per-channel. A timeout may be disabled by setting the register value to '0'. Disabling the timeout may be necessary for follower and reference channels, and are required for ULP entry channels retaining an active state in ULP.

5.5.8 Global Halt

The global halt feature provides functionality to halt the LTA filters of certain channels if any of them are in activation.

Global halt can be enabled for any channel by setting the *Global Halt* bit in the channel's *General Channel Setup* register.

If any global-halt-enabled channels are in activation, the *Global Halt* flag in the *System Status* register is set. Once *Global Halt* is set, all channels that have global halt enabled will keep their LTA values static until all the relevant channels exit activation.

5.6 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in ProxFusion devices to allow optimal performance of the devices for a wide range of sensing electrode designs, without modification to external components. The ATI functionality ensures that sensor sensitivity is not affected by external influences such as temperature, parasitic capacitance, and ground reference changes.

In order for the ProxFusion engine to handle a wide range of capacitive loads and input signals, the IQS7222A provides two mechanisms to condition the input signal for a desired working counts range: gain and DC subtraction. Gain scales the sensor input to a desired range. The amount of gain is controlled by the *Multipliers and Dividers* register. After the gain stage, DC subtraction is performed to compensate for DC offsets and increase sensitivity to changes in the input signal. DC subtraction is controlled by the *Compensation* register. Multipliers, dividers, and compensation are adjusted on a per-channel basis.

The working range of each channel of the IQS7222A can be calibrated automatically using the on-chip ATI feature, which adjusts the *Multiplier and Divider* and *Compensation* registers until the reported counts from the sensor reaches a set of target counts values. These targets are known as the *ATI Base* and *ATI Target*.

The *ATI Base* value sets the desired nominal counts of a channel after the gain stage, and thus controls the amount of gain applied to the input signal. The *ATI Target* value sets the desired raw counts after both the gain and DC subtraction stages. The ATI algorithm first calibrates the multipliers to reach the Base counts, then calibrates the compensation to reach the target counts. Since counts are inversely proportional to signal strength, using DC subtraction will cause an increase in counts. Therefore the Target should always be higher than the Base value if compensation is required. Typical values for the Base value lie between 100 and 500 counts, while the Target is typically set to between 500 and 1000 counts.

Note that the Base value in counts is calculated from the 5-bit register value as Base counts $=$ $16 \times$ *Base Register Value*. The target value in counts is calculated from its 8-bit register value as Target counts $= 8 \times$ *Target Register Value*. Base and target selection also allows for fine adjustment of the sensitivity of the sensor to user interaction, following the relationship

$$\text{Sensitivity} \propto \frac{\text{Target}}{\text{Base}}.$$

Sensitivity can thus be increased by either increasing the Target value or decreasing the Base value. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility.

Compensation is typically not recommended for inductive sensing. Compensation may be disabled by setting Base $\geq$ Target.

ATI can be triggered manually by setting the *ATI* bit in the *Control Settings* register. ATI may also be triggered automatically under certain conditions, described in Section 5.6.4.

5.6.1 ATI Modes

The ATI algorithm calibrates the following properties in order:

1. Coarse Fractional Multiplier
2. Coarse Fractional Divider
3. Fine Fractional Divider
4. Compensation Divider
5. Compensation

The starting point of the ATI sequence can be set to one of the following modes:

- Full ATI (calibrate all properties, ATI to Base and Target)
- ATI From Coarse Fractional Divider (ATI to Base and Target)
- ATI From Fine Fractional Divider (ATI to Base and Target)
- ATI From Compensation Divider (ATI to Target)
- ATI From Compensation Only (ATI to Target)
- ATI Disabled

“Full ATI” will calibrate all the *Multipliers and Dividers* and the *Compensation*. “ATI From Compensation Divider” will only calibrate the Compensation register. This allows an application to use a fixed set of Multipliers for all devices across production. “ATI Disabled” will never allow the channel to perform an ATI calibration, even if an ATI command is given.

5.6.2 ATI Preloads

Given the sequence of ATI stages in Section 5.6.1, when calibrating the Base value, the *Coarse Fractional Divider* and *Fine Fractional Divider* can be preloaded using the Global *Dividers Preload* register. Similarly, the *Compensation* value can be preloaded during the *Compensation Divider* stage using the *Compensation Preload* register.

5.6.3 ATI Error

After the ATI algorithm has completed, a check is performed to verify that no errors occurred during the ATI execution. An *ATI Error* is reported in the *System Status* register if the reported counts are

already outside the Re-ATI range upon completion of the ATI algorithm. The *ATI Error* status is only updated the next time ATI executes.

5.6.4 Automatic Re-ATI

The Automatic Re-ATI feature allows for easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor, and can also automatically recalibrate the sensor if environmental drift is detected. It is always recommended to have the automatic Re-ATI functionality enabled. When a Re-ATI is performed on the IQS7222A, a status bit will be momentarily set to indicate that this has occurred.

A Re-ATI is automatically triggered under the following conditions:

- If an ATI Error occurs.
- When the reference of a channel drifts outside of the acceptable range around the ATI Target.

The threshold to trigger an ATI due to reference drift is controlled by the *ATI Band* setting, which is specified as a fraction of the ATI target. The band can be set to one of the following values in the *CRX Select and General Channel Setup* register:

- 1/2
- 1/4
- 1/8
- 1/16

The boundaries around the ATI Target where re-ATI occurs are calculated as $\pm(\text{ATI Target} \times \text{ATI Band})$.

For example, for an ATI Target of 800 counts and an ATI band of 1/8, the boundary value is $800 \times \frac{1}{8} = 100$ counts. If Re-ATI is enabled, the ATI algorithm will be triggered under the following conditions:

$$\text{Reference} < 700 \quad \text{or} \quad \text{Reference} > 900$$

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI Error Timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. The ATI Error Timeout is specified in increments of 0.5 seconds. An ATI error should, however, not occur under normal circumstances.

5.7 Hall Effect Switch UI

Hall-effect sensing is an internal sensing option that requires no external sensor design. The Hall-effect switch UI measures magnetic fields perpendicular to the Hall plate of the IC, and is enabled when both Hall-effect channels (channels 10 and 11) are enabled. It can be used for detection of the presence of a single magnet.

The UI uses two measurements to determine changes in the magnetic field, where the second measurement is inverted to the first. These two measurements allow for the calculation of a reference value and a differential value, from which the relative strength of the magnetic field can be inferred. As a result, the Hall switch UI can detect the presence of a magnet at startup and after an ATI calibration.

Channel 10's output is the differential Hall signal. This represents the magnitude of the magnetic field, and changes as the magnetic field changes. With no magnetic field present, its output is 0 counts. It is calculated using:

$$\text{CH10 Counts} = \frac{\text{Hall Counts} - \text{Hall Counts}_{\text{inv}}}{2}$$

Channel 11's output is the reference value, which acts as an LTA. This value stays constant, regardless of the presence of a magnet, and is calculated using:

$$\text{CH11 Counts} = \frac{\text{Hall Counts} + \text{Hall Counts}_{\text{inv}}}{2}$$

5.7.1 Hall Configuration

Channels 10 and 11 must be enabled, and each channel controls different parameters of the Hall switch UI. Please note that parameters not listed under the relevant channel's setting below must be left as default.

Since channel 10 provides the differential Hall signal, all the relevant settings are related to thresholds and event detection. (These settings for channel 11 have no effect.) Event detection for the Hall-effect sensor is therefore performed only on channel 10. Settings from channel 10 used for Hall-effect switch UI are:

- Touch Threshold
- Prox Threshold
- Touch Hysteresis
- Enter debounce
- Exit debounce

Channel 11 settings focus on sensor configuration. Settings from channel 11 used for Hall effect switch UI:

- ATI Mode
- ATI Band
- ATI Compensation
- ATI Compensation Divider
- ATI Coarse Fractional Divider
- ATI Coarse Fractional Multiplier
- ATI Fine Fractional Divider

Settings that should be the same on channel 10 and channel 11 are:

- Conversion Frequency Fraction
- Conversion Frequency Period
- Ground Inactive Rx's
- Vref 0v5 Enable
- Cs Size
- ATI Base
- ATI Target

5.8 Summary of ProxFusion® Settings

5.8.1 Summary of Cycle Settings

Cycle settings apply to both channels associated with that cycle. A list of settings related to cycle setup is given in Table 5.3 below.

Table 5.3: Cycle Settings

Setting	Description
PXS Mode	Sets the sensing mode for the cycle. See Section A.8.
Conversion Frequency Fraction	Sets the conversion frequency. See Section 5.4.3.
Conversion Frequency Period	
Dead Time Enable	Enable for capacitive sensing, disable for Hall and inductive sensing. See Section 5.4.3.
F_{OSC} Tx Frequency	Recommended for inductive sensing only. See Section 5.4.4.
Tx Selection	CTx0 to CTx8. See Section 5.4.2.
Maximum Counts	See Section 5.4.5.
Ground Inactive Rx's	Ground or float unused Rx pins. It is always recommended to ground inactive Rxs.
V_{bias} Enable	Enable V_{bias} (constant voltage drive onto CTx8) for resonant inductive sensing. Recommended to keep disabled.

5.8.2 Summary of Channel Settings

Settings related to channel setup are shown in Table 5.4 below.

Table 5.4: Channel Settings

Setting	Description
Channel Enable	Enables sensing on the channel.
Rx Selection	CRx0 to CRx7. See Section 5.4.2.
Cs Size	80 pF recommended. See Section 5.4.6.
Vref 0.5 V Enable	Recommended to keep this disabled. See Section 5.4.6.
Projected Bias Select	Selection of bias current for mutual capacitive mode. Set to 10 µA. See Section A.16.
Proximity Threshold	See Section 5.5.4.
Touch Threshold	See Section 5.5.5.
Proximity Enter Debounce	Section 5.5.4.
Proximity Exit Debounce	Section 5.5.4.
Touch Hysteresis	See Section 5.5.5.
Proximity Event Timeout	Section 5.5.7.
Touch Event Timeout	Section 5.5.7.
ATI Mode	Auto Tuning Implementation mode. See Section 5.6.1.
ATI Base	See Section 5.6.
ATI Target	See Section 5.6.
ATI Band	See Section 5.6.4.
Invert Direction	See Section 5.5.6.
Bi-directional Sensing	See Section 5.5.6.
Global Halt	See Section 5.5.8.

5.8.3 Summary of Global Settings

Global UI settings are listed in Table 5.5 below.

Table 5.5: Global Settings

Setting	Description
Counts Filter Beta	See Section 5.5.1.
Counts Low Power Filter Beta	
LTA Filter Beta	See Section 5.5.2.
LTA Low Power Filter Beta	
LTA Fast Filter Beta	See Section 5.5.6.
LTA Low Power Fast Filter Beta	

5.8.4 Summary of ProxFusion Outputs

ProxFusion sensor output registers are listed in Table 5.6 below.

Table 5.6: ProxFusion Sensor Outputs

Output	Description
Proximity Event States	Shows proximity state of each channel.
Touch Event States	Shows touch state of each channel.
Channel X Counts	Filtered counts value of each channel.
Channel X LTA	Reference value of each channel.

6 Slider User Interface

The IQS7222A is capable of processing a slider with on-chip gesture recognition. The IQS7222A supports processing two sliders simultaneously, with each slider consisting of up to four touch channels. The IQS7222A slider UI allows for the following combinations:

- 2 x 3 element mutual capacitive sliders
- 2 x 4 element self-capacitive sliders
- 1 x 4 element mutual capacitive slider

Enabled gestures are reported in the *Slider Gesture Status* register. The position of the touch on the slider is reported in the *Slider Position* register.

6.1 Slider Setup

The slider is enabled by setting the *Total Channels* field in the *Slider General Setup* register to a non-zero value and enabling the slider channels by setting the *Channel X Enable* bits in the *Slider Enable Mask* register.

The *Slider Enable Status Link* register must be linked to touch. This activates the slider when any of the enabled channels are in touch.

The *Delta Link* registers, from Delta Link 0 to Delta Link 3, determine the order in which the enabled channels are processed. For example, if channel 1 is the first element in the slider, the *Delta Link 0* register must be set to the appropriate value for channel 1. Refer to Section A.29 for specific values.

The *Slider Resolution* value defines the output range of the slider position, which are reported in "pixels". The touch position ranges from 0 to the *Slider Resolution*, where 0 is the start of the first slider element and the *Slider Resolution* is the end of the last slider element. The gesture setup registers (e.g., swipe distance) must be set in accordance with the *Slider Resolution*.

The slider's *Upper Calibration* value and the *Lower Calibration* value are used to offset the end-points of the slider position so that they match the end-points of the physical slider. These values are specified in pixels.

6.2 Slider Position Filtering

The slider output position is dynamically filtered based on the *Slow/Static Beta* in the *Slider General Setup* register, the *Bottom Speed* field in the *Slider Calibration and Bottom Speed* register, and the value in the *Slider Top Speed* register. The slider's *Top Speed* and *Bottom Speed* are specified in pixels per sample period (i.e., how far a finger moves between samples). Figure 6.1 shows the behaviour of the dynamic filter.

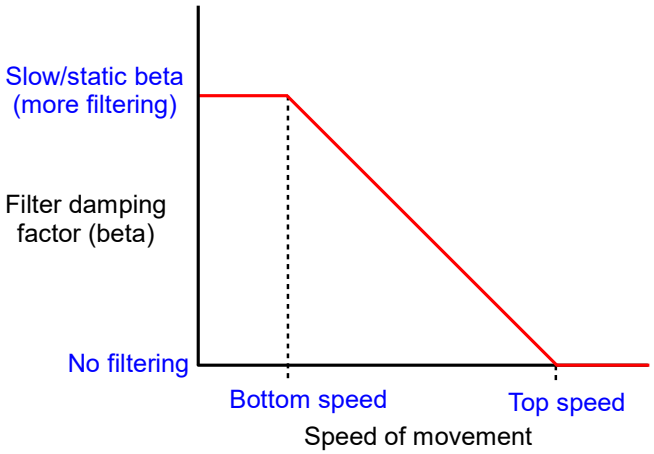


Figure 6.1: Slider Filtering When the Static Filter Bit is Not Set

Bottom and top speed parameters ensure stronger filtering when changes in slider position are slower, in the region of the bottom speed, while ensuring no filtering when the slider position changes rapidly as defined in the top speed parameter. This has value in precise slider applications with very fine adjustment requirements while not losing reactivity when larger movements are made.

If the *Static Filter* bit in the *Slider General Setup* register is set, the *Slow/Static Beta* is used to filter the slider position regardless of the touch's movement speed.

6.3 Gestures

The IQS7222A does on-chip gesture recognition when a slider is enabled.

All gestures are configurable and can be individually enabled using the *Gesture Setup 0* register. Gestures are reported in the *Slider Gesture Status* register.

The recognised gestures are:

- Single Tap
- Swipe
- Flick

Gesture parameters are specified in pixels and milliseconds.

For any gesture to be reported, a touch must be registered for at least as long as the value in the *Minimum Gesture Time* register. This prevents false touches from triggering the gestures.

6.3.1 Tap

A tap gesture will be reported if the touch lasts longer than the *Minimum Gesture Time* but less than the time specified by the *Maximum Tap Time* setting, and the touch does not move further than the value in the *Minimum Swipe Distance* setting from its starting point. The tap will be reported only for the cycle in which it is detected.

6.3.2 Swipe and Flick

Swipe and flick gestures are reported if there is a touch lasting longer than the *Minimum Gesture Time*, and the touch moves further from its starting point than the value in the *Minimum Swipe Distance*

register. Given that the above conditions have been met, if the touch is released before the time specified in the *Maximum Swipe Time* register, a flick is reported. Otherwise, a swipe is reported.

All gesture flags are cleared once a touch is no longer detected on the slider. This means that taps and flicks are reported once, in the cycle in which they are detected. Swipes are reported for as long as the slider remains in touch. Additionally, there is a 4 second timeout on the slider. All slider gesture events are cleared automatically if the touch on the slider lasts longer than 4 seconds.

6.3.3 Busy

The *Busy* flag in the *Slider Gesture Status* register is a simple indication that at least one of the channels in the slider is in activation.

6.4 Summary of Slider Registers

All registers and settings below can be uniquely configured for slider 0 and slider 1.

6.4.1 Slider Outputs

Slider read-only registers are listed in Table 6.1.

Table 6.1: Slider Outputs

Output	Description
Slider Position	Filtered coordinate of finger on slider, given in pixels.
Slider Gesture Status	Indicates gesture detection events.

6.4.2 Slider Configuration Summary

Slider channel registers are listed in Table 6.2.

Table 6.2: Slider Channel Configuration

Setting	Description
Total Channels	Number of touch elements/channels in slider.
Enable Mask	Sets which channels are used to enable slider processing.
Enable Status Link	Sets whether slider processing should start on proximity or touch event.
Delta Link 0 – 3	“Links” channel delta values to slider elements for position calculation.

Slider resolution registers are listed in Table 6.3.

Table 6.3: Slider Resolution Configuration

Setting	Description
Resolution	See Section 6.1.
Lower Calibration	
Upper Calibration	

Slider filter settings are listed in Table 6.4.

Table 6.4: Slider Filter Configuration

Setting	Description
Bottom/Static Beta	See Section 6.2.
Static Filter	
Bottom Filter Speed	
Top Speed	

Gesture settings are listed in Table 6.5. These are applicable to Slider 0 and 1.

Table 6.5: Slider Gesture Settings

Setting	Description
Gesture Enable	Individually enable tap, swipe, and flick gestures. See Section 6.3.
Maximum Tap Time	Sets gesture detection conditions. See Section 6.3.
Minimum Gesture Time	
Minimum Swipe Distance	
Maximum Swipe Time	

7 Power Modes

7.1 Power Mode Overview

The IQS7222A offers 3 power modes:

- Normal power mode (NP):
  - Flexible sampling rate.
  - Sampling rate is controlled by the *Normal Power Mode Report Rate*, specified in milliseconds.
  - Primarily used during, and shortly after, an activation.
- Lower power mode (LP):
  - Flexible sampling rate.
  - Typically set to a slower rate than NP.
  - Sampling rate is controlled by the *Low Power Mode Report Rate*, specified in milliseconds.
  - Primarily used after some period of inactivity.
- Ultra-low power mode (ULP):
  - Firmware setup optimised for minimal current consumption.
  - Only Cycle 0 (Channels 0 and 5) is sampled.
  - Intended for rapid wake-up on a single channel (e.g., distributed proximity event).
  - The wake-up channels are sampled at the *Ultra-low Power Mode Report Rate*. These channels' LTAs are processed after a set number of ULP samples, specified by the *ULP Conversion Count* setting in the *Global Cycle Setup* register.
  - The other channels are sampled at the rate specified in the *Normal Power Update Rate in ULP* register.

The power mode of the device can be controlled by the *Power Mode Selection* setting in the *Control Settings* register. The power mode can be forced into one of the above modes, or set to 'Automatic' mode.

7.2 Automatic Power Mode Switching

By default, the IQS7222A is set to use 'Automatic' power mode switching. This optimises power consumption by stepping the power modes, moving to more power-efficient modes when no interaction has been detected for a certain time. This time is known as the "Power Mode Timeout", and is uniquely configurable for *Normal Power* and *Low Power*. Setting a timeout to '0' will disable the timer, and prevent the device from automatically transitioning to a lower power mode.

When any channel enters or exits activation (i.e., on proximity or touch event), the IQS7222A will transition to normal power mode, and restart the normal power timeout. The IQS7222A may transition from NP to LP while a channel is in touch or activation. However, automatic entry into ultra-low power mode is dependent on the *ULP Entry Mask*. Enabling a specific channel in the ULP Entry Mask allows the IQS7222A to enter ULP while the channel is in activation.

The current power mode is reported in the *System Status* register.

7.3 Ultra-Low Power Mode

In ULP mode, only Cycle 0 (Channels 0 and 5) is sampled. These channels should be used as wake-up channels, allowing the IQS7222A to wake up and switch to a higher power mode when detecting any user interaction.

CH0 and CH5 are sampled at the *ULP report rate*. LTA and filter values for CH0 and CH5 are not processed every cycle, but are processed once every *N* cycles, based on the *ULP Conversion Count* setting in *Global Cycle Setup*.

The IQS7222A will also wake up periodically to perform a full “Normal Power” cycle. Here, all channels are sampled, and their respective LTAs updated, in order to maintain consistent environmental tracking. The rate at which the IQS7222A performs these “Normal Power” cycles is controlled by the *Normal Power Update Rate in ULP* parameter. After this cycle, the IQS7222A returns to ULP mode.

7.4 Summary of Power Mode Registers

Table 7.1: Power Mode Settings

Setting	Description
Current Power Mode	Set current power mode.
Normal Power Mode Report Rate	Set sampling rate of each power mode.
Low power Mode Report Rate	
Ultra-Low Power Mode Report Rate	
Normal Power Update Rate in ULP	Sets rate of full channel updates in ULP.
Normal Power Mode Timeout	Sets timeout until device transitions to lower power mode.
Low Power Mode Timeout	

8 GPIO Output

The IQS7222A provides a general-purpose output pin, labelled OUTA, and also referred to as the output channel. The output pin can be used to either represent the Proximity or Touch state of specific channels, or to indicate the Slider Tap, Flick or Swipe events.

8.1 Initial Setup

To enable the GPIO output channel (OUTA), the *Enable* bit in the *OUTA Control* register needs to be set. The output pin supports either push-pull active-high mode or open-drain active-low mode, which can be selected in the *OUTA Control* register.

8.2 ProxFusion State Output

The GPIO output can assign any number of ProxFusion channel (CH0 – CH10) states to the OUTA pin. The output channel needs to be set to Proximity or Touch mode by setting the output *Status Link* to either 'Prox' or 'Touch' in the *OUTA Status Link Control* register. This "links" either the *Proximity Event States* or the *Touch Event States* register to the output channel. The *OUTA Enable Mask* then sets which bits (sensing channels) are used to determine the output pin state.

As an example, consider the following application requirements for OUTA:

- Report the Touch state of ProxFusion Channel 3,
- Pin mode: Active-high (push-pull)

In other words, if CH3 experiences a touch event, the OUTA pin will be high for the duration of the touch event, and low otherwise. The necessary settings to meet these requirements are:

1. Enable the output by setting the *Enable* bit in the *OUTA Control* register.
2. Clear the *Output Configuration* bit in the *OUTA Control* register to set the pin to active-high.
3. Set Touch control mode in the *OUTA Status Link* register.
4. Set the *CH3* bit in the *OUTA Enable Mask* register.

It is possible to report the Prox or Touch state of multiple prox channels on the output channel by setting all the required channel bits in the *OUTA Enable Mask* register. For the example above, if both CH3 and CH9 bits are set then if either of those channels has an active touch event, the state will be reported on the OUTA pin.

8.3 Slider State Output

The GPIO output channel can assign the output state of either the Tap, Flick, or Swipe event state of either Slider 0 or Slider 1 to the OUTA pin. The output channel needs to be linked to either Slider 0 or Slider 1 by setting either 'Slider 0 Event' or 'Slider 1 Event' in the *OUTA Status Link Control* register. This "links" either the *Slider 0 Event States* or the *Slider 1 Event States* register to the output channel. The *OUTA Enable Mask* then sets which bits (Tap, Flick, or Swipe) are used to determine the output pin state.

As an example, consider the following application requirements for OUTA:

- Report the Tap state of Slider 0,
- Pin mode: Active-high (push-pull)

In other words, if Slider 0 experiences a tap event, OUTA pin will be high for the duration of the tap event, and low otherwise. The necessary settings to meet these requirements are:

1. Enable the output by setting the *Enable* bit in the *OUTA Control* register.
2. Clear the *Output Configuration* bit in the *OUTA Control* register to set the pin to active-high.
3. Set Slider 0 Event control mode in the *OUTA Status Link* register.
4. Set the *Tap* bit in the *OUTA Enable Mask* register.

It is possible to report the Tap, Flick, and Swipe state of the selected slider on the output channel by setting all the required channel bits in the *OUTA Enable Mask* register. For the example above, if both the Tap and Swipe bits are set then if either of those events occur, the state will be reported on the OUTA pin.

8.4 Summary of OUTA Registers

Table 8.1: IQS7222A GPIO Settings

Setting	Description
GPIO Enabled	Enable or disable GPIO output
Output Configuration	Select logic of the GPIO output, push-pull active high or open-drain active low.
Channel Enable Mask	Select channels or gesture events on which the GPIO output will trigger.
Enable Status Link	Set GPIO output to trigger on proximity, touch or slider event.

9 Additional Features

9.1 Debug and Display Software (GUI)

The Azoteq IQS7222A GUI can be utilised to configure the optimal settings required for a specific hardware setup or application. The device performance can be easily monitored and evaluated in the graphical environment until the optimal device configuration is obtained.

Once the IQS7222A is configured in the GUI as desired, a C header file (*.h* file) can be exported that stores the values of all the read-write registers of the IQS7222A. The *.h* file displays the start address of each block of data, with each address containing two bytes in little endian order. An example of the *.h* file exported by the GUI is shown below.

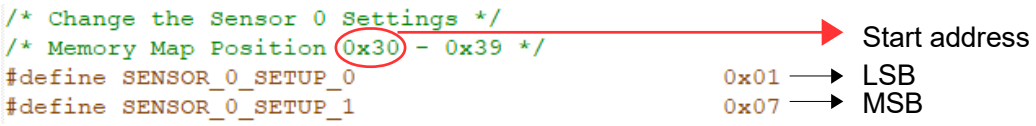


Figure 9.1: Example of an H file Exported by the GUI

9.2 Watchdog Timer (WDT)

A software watchdog timer is implemented to improve system reliability.

The working of this timer is as follows:

- A software timer t_{WDT} is linked to the LFTMR (Low frequency timer) running on the "always on" Low Frequency Oscillator (10 kHz).
- This timer is reset at a strategic point in the main loop.
- Failing to reset this timer will cause the appropriate ISR (interrupt service routine) to run.
- This ISR performs a software triggered POR (Power on Reset).
- The device will reset, performing a full cold boot.
- The default, fixed value of the watchdog timer is 1500 ms.

9.3 RF Immunity

The IQS7222A has immunity to high-power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100 pF in parallel with the 2.2 µF ceramic on V_{REG}. Place a 4.7 µF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sending pads. Normally these are in the range of 470 Ω – 1 kΩ. PCB ground planes also improve noise immunity.

9.4 Reset Indication

After a reset, the *Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*. If it becomes set again, the master will know a reset has occurred and can react appropriately.

While the *Reset* bit remains set:

- The device will not be able to enter into I²C Event mode operation (i.e. streaming communication behaviour will be maintained until the Reset bit is cleared).
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in much longer time to finish the ATI routine.

9.5 Software Reset

The IQS7222A can be reset by means of an I²C command (*Soft Reset*).

10 I²C Interface

10.1 I²C Module Specification

The device features a standard two-wire I²C interface, complemented by a RDY (ready interrupt) line, supporting a maximum bit rate of up to 1 Mbit/s. The IQS7222A implements a combination of 8-bit addressing and 16-bit addressing, with 2 data bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes, stored at each address in little-endian order, will be referred to as “byte 0” (least significant byte) and “byte 1” (most significant byte).

Features:

- Standard two-wire interface with RDY interrupt line
- *Fast-Mode Plus* I²C with up to 1 Mbit/s bit rate
- 7-bit device address
- Combination of 8-bit and 16-bit register addressing
- Two data bytes stored per register address, in little-endian order
- Streaming and Event modes

10.2 I²C Address

The 7-bit device address for order code 001 is 0x44 (0b01000100), while the 7-bit device address for order code 102 is 0x57 (0b01010111). The full address byte for address 0x44 will thus be 0x89 (read) or 0x88 (write), and the full address byte for address 0x57 will be 0xAF (read) or 0xAE (write).

Other address options exist on special request. Please contact Azoteq.

10.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

10.4 Memory Map Addressing

10.4.1 8-bit Address

Most of the memory map implements an 8-bit addressing scheme for the required user data. Extended memory map addresses implement a 16-bit addressing scheme.

10.4.2 Extended 16-bit Address

For development purposes, larger blocks of data are found in an extended 16-bit memory addressable location. It is possible to address each block as an 8-bit address and then continue to clock into the next address locations. Figure 10.1 depicts a hypothetical procedure to read data from address 0xE000 to 0xE003 by sending 0xE0 as the register address.

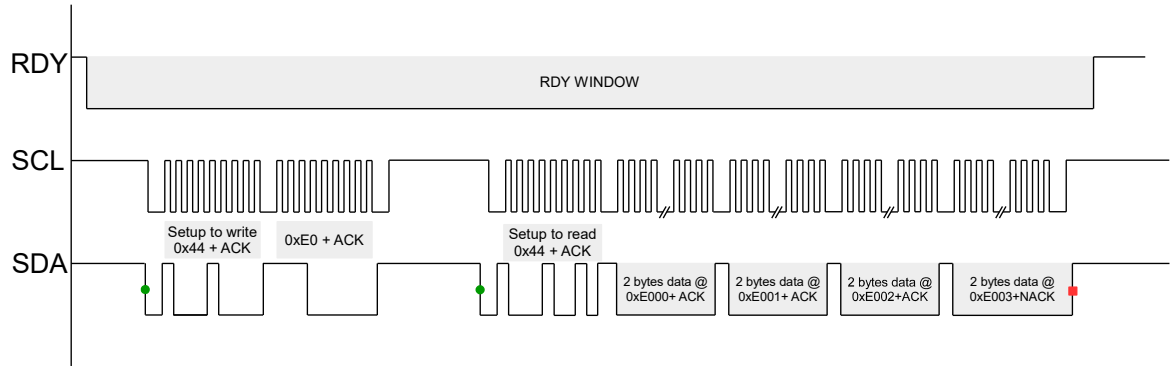


Figure 10.1: Extended 16-bit Addressing for Continuous Block

However, in order to address specific bytes in the extended memory map space, the full 16-bit address must be sent in big endian order (most significant byte first). Below is an example of reading data bytes from register 0xE003.

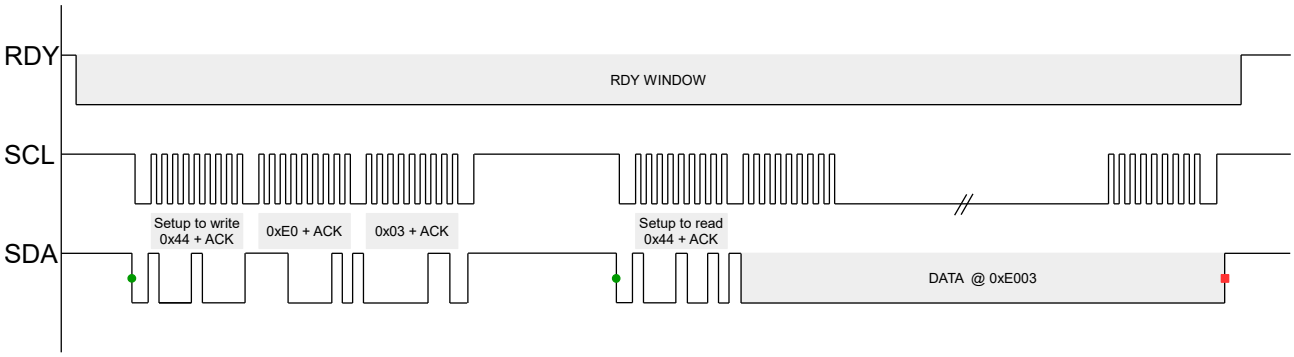


Figure 10.2: Extended 16-bit Addressing for a Specific Register

Note that extended 16-bit addresses are sent in big endian order, but data from those addresses is stored in little endian format.

10.5 Memory Map Data

Data is stored in 16-bit words, meaning that each address contains two bytes of data. For example, address 0x10 will provide two bytes, then the next two bytes read will be from address 0x11. The 16-bit data is sent in little endian byte order (least significant byte first).

10.6 RDY/IRQ

The IQS7222A has an open-drain active low RDY signal to inform the master that updated data is available. The IQS7222A will pull the RDY line low to indicate that it has opened a communications window, or “RDY window”, for the master to read the new updated data. While the master can communicate with the device at any time according to the *Force Communication Method*, it is recommended to use the RDY signal for optimal power consumption. Integrating the RDY signal as an interrupt input allows the master MCU to read and write data efficiently.

The IQS7222A will open a communication window when new data is available, and will typically close the window after an I^2C stop event is detected.

10.7 I²C Interface Modes

The IQS7222A has three *I²C interface options*:

- **Streaming Mode**: The IQS7222A opens a communication window (by pulling the RDY pin low) after every sensing cycle to report new data. This mode is useful for evaluation and debugging.
- **Event Mode**: A communication window is opened only if an enabled event occurs, and activity is detected. This reduces the amount of unnecessary I²C traffic and RDY interrupts, and is the recommended mode for normal operation.
- **Stream in Touch Mode**: Stream in Touch is a hybrid between Streaming Mode and Event Mode. The device follows the Event Mode I²C protocol. When a touch is registered on any channel, the device enters Streaming Mode until the touch is released. This mode is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

10.8 Event Mode Communication

Event Mode bypasses the communication window when no activity is sensed. This is usually enabled since the master does not need to be interrupted unnecessarily during every cycle if no activity occurs. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

Event Mode can only be entered if the following requirements are met:

- Events must be serviced by reading from the *Events* register to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every cycle, similar to streaming mode.
- The *Device Reset* bit in the *System Status* register has been cleared by setting the *Acknowledge Reset* bit in *Control Settings*.

10.8.1 Events

Numerous events can be individually enabled to trigger communication in Event Mode. Bit definitions can be found in Tables A.2 and A.3:

- Power mode change
- Prox or touch event
- Slider event
- ATI event

10.8.2 Force Communication

In Streaming Mode, the IQS7222A I²C will provide communication windows at regular intervals specified by the relevant power mode report rate. This will provide the master with regular opportunities to perform I²C communication as necessary.

If the device is placed in Event Mode, the IQS7222A will not open RDY windows unless certain conditions are met. A new RDY window can be requested by writing 0xFF over I²C, followed by a stop condition. After a short delay, the IQS7222A will pull the RDY line low and open a new communication window. This is shown in Figure 10.3.

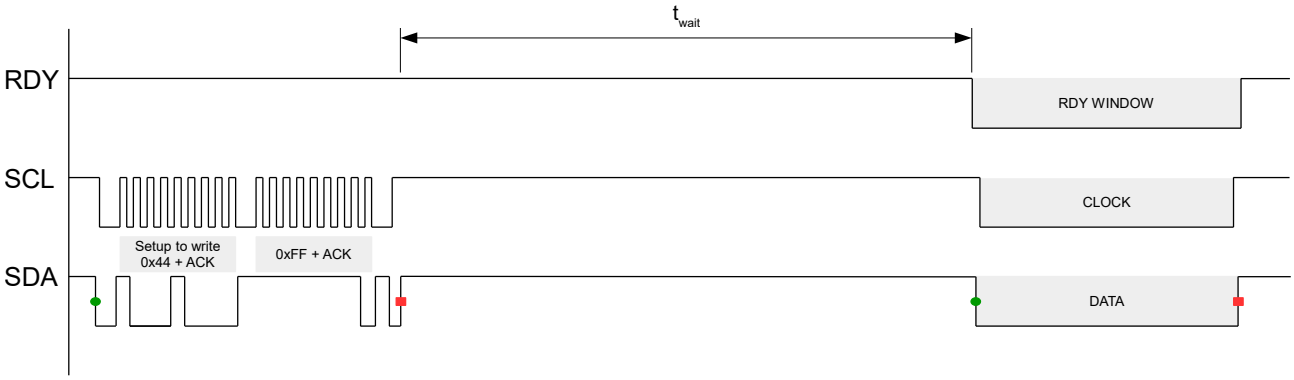


Figure 10.3: Force Communication Sequence

The time between the communication request and the opening of a RDY window (t_{wait}) is dependent on the specific application. Once the communication request is received, the IQS7222A wakes up from sleep mode, performs sampling and processing on all channels, and then opens a communication window. As a result, t_{wait} is dependent on channel and cycle settings, and may be on the order of 12 ms for a full 12-channel device.

Note: The IQS7222A may clock stretch (hold the SCL line low) for up to 400 µs after the 0xFF byte if the force communication command is received while the IQS7222A is in an internal sleep mode.

A force communication request should be avoided while RDY is held low, as the STOP condition after the 0xFF byte will cause an existing communication window to close immediately.

10.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside a communication window (while RDY is high).

10.10 I²C Timeout

If the communication window is not serviced within the *Communication Timeout* period (in milliseconds), the session is ended (RDY goes high), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be lost, so this should be avoided. The default I²C timeout period is set to 500 ms.

10.11 Terminate Communication

By default, a standard I²C STOP will end the current communication window. If multiple I²C transactions need to be performed within a single communication window, they should be strung together using repeated START conditions, with only the last transaction ending with a STOP. Allowing an I²C STOP to terminate the communication window is recommended.

However, for I²C controllers that cannot support repeated START conditions, the IQS7222A provides an option to ignore the STOP condition and keep the window open. This behaviour can be enabled by setting the *Stop Bit Disabled* bit in the *I²C Communication* register.

In this case, the communication window can be terminated as desired using one of the following methods:

- Writing a single 0xFF byte will close the communication window, as illustrated in Figure 10.4.

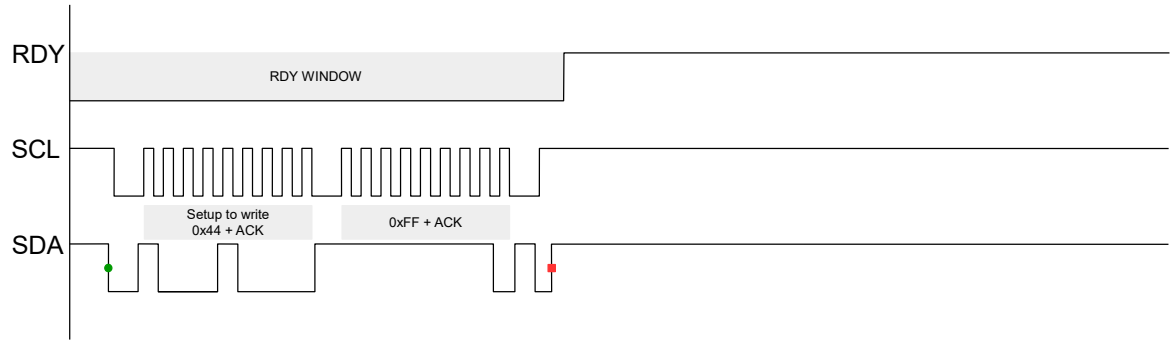


Figure 10.4: Force Stop Communication Sequence

- Alternatively, in each communication window, the stop bit check may be disabled in the first transaction, followed by normal I²C transactions. The window can be closed by re-enabling the check as the final transaction, followed by a STOP.

10.12 Summary of I²C Settings

Table 10.1: I²C Module Settings

Setting	Description
Interface selection	Enable Streaming or Event Mode. See Section 10.7.
Event Mask	Sets which system events should open a communication window if in Event mode. See Section 10.8.1.
Stop Bit Disabled	See Section 10.11.
RW Check Disabled	See Section A.39.
I²C Communication Timeout	See Section 10.10.

11 Program Flow Diagram

The program flow for event mode communication is shown in Figure 11.1.

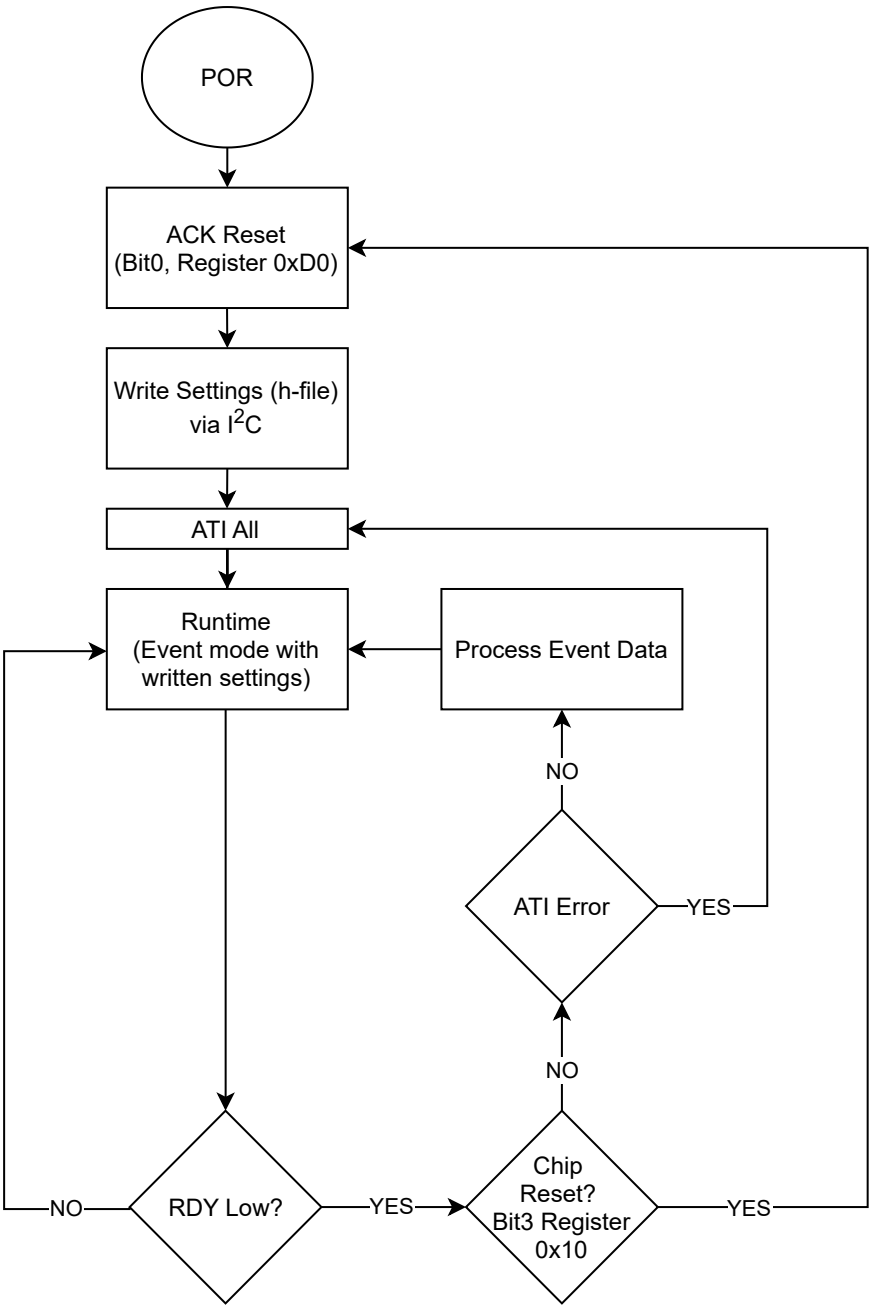


Figure 11.1: Program Flow Diagram

12 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions.

Address	Data (16bit)	Default	Notes
0x00 - 0x09	Version details		See Section A.1
Read Only		-	
0x10	System Status	-	See Section A.2
0x11	Events	-	See Section A.3
0x12	Proximity Event States	-	See Section A.4
0x13	Touch Event States	-	See Section A.5
0x14	Slider 0 Position	-	16-bit value
0x15	Slider 1 Position	-	
0x16	Slider 0 Gesture Status	-	See Section A.6
0x17	Slider 1 Gesture Status	-	
Read Only	**Channel Counts**		
0x20	Channel 0 Counts	-	16-bit value
0x21	Channel 1 Counts	-	
0x22	Channel 2 Counts	-	
0x23	Channel 3 Counts	-	
0x24	Channel 4 Counts	-	
0x25	Channel 5 Counts	-	
0x26	Channel 6 Counts	-	
0x27	Channel 7 Counts	-	
0x28	Channel 8 Counts	-	
0x29	Channel 9 Counts	-	
0x2A	Channel 10 Counts	-	
0x2B	Channel 11 Counts	-	
Read Only	**Channel LTA**		
0x30	Channel 0 LTA	-	16-bit value
0x31	Channel 1 LTA	-	
0x32	Channel 2 LTA	-	
0x33	Channel 3 LTA	-	
0x34	Channel 4 LTA	-	
0x35	Channel 5 LTA	-	
0x36	Channel 6 LTA	-	
0x37	Channel 7 LTA	-	
0x38	Channel 8 LTA	-	
0x39	Channel 9 LTA	-	
0x3A	Channel 10 LTA	-	
0x3B	Channel 11 LTA	-	
Read-Write	**Cycle Setup**		
0x8000	Cycle 0 Setup	0x0C7F	See Section A.7
0x8001		0x7FE1	See Section A.8
0x8002		0x0000	See Section A.9
0x8100	Cycle 1 Setup	0x0C7F	See Section A.7
0x8101		0x08E1	See Section A.8
0x8102		0x0000	See Section A.9
0x8200	Cycle 2 Setup	0x0C7F	See Section A.7
0x8201		0x1161	See Section A.8
0x8202		0x0000	See Section A.9
0x8300	Cycle 3 Setup	0x0C7F	See Section A.7
0x8301		0x2261	See Section A.8

0x8302		0x0000	See Section A.9
0x8400	Cycle 4 Setup	0x0C7F	See Section A.7
0x8401		0x4461	See Section A.8
0x8402		0x0000	See Section A.9
0x8500	Cycle 5 (Hall Switch) Setup	0x0200	See Section A.7
0x8501	Reserved	0x0045	
0x8502		0x0000	
0x8600	Cycle 6 (Hall Reference) Setup	0x0200	See Section A.7
0x8601	Reserved	0x0046	
0x8602		0x0000	
0x8700	Global Cycle Setup	0x2B8B	See Section A.10
0x8701	Coarse and Fine Divider Preloads	0x3010	See Section A.11
0x8702	Compensation Preload	0x0200	See Section A.12
Read-Write	**Button Setup - Thresholds, Hysteresis and Debounce**		
0x9000	Channel 0 Button Setup	0x120A	See Section A.13
0x9001		0x0019	See Section A.14
0x9002		0x3008	See Section A.15
0x9100	Channel 1 Button Setup	0x120A	See Section A.13
0x9101		0x0019	See Section A.14
0x9102		0x3008	See Section A.15
0x9200	Channel 2 Button Setup	0x120A	See Section A.13
0x9201		0x0019	See Section A.14
0x9202		0x3008	See Section A.15
0x9300	Channel 3 Button Setup	0x120A	See Section A.13
0x9301		0x0019	See Section A.14
0x9302		0x3008	See Section A.15
0x9400	Channel 4 Button Setup	0x120A	See Section A.13
0x9401		0x0019	See Section A.14
0x9402		0x3008	See Section A.15
0x9500	Channel 5 Button Setup	0x120A	See Section A.13
0x9501		0x0019	See Section A.14
0x9502		0x3008	See Section A.15
0x9600	Channel 6 Button Setup	0x120A	See Section A.13
0x9601		0x0019	See Section A.14
0x9602		0x3008	See Section A.15
0x9700	Channel 7 Button Setup	0x120A	See Section A.13
0x9701		0x0019	See Section A.14
0x9702		0x3008	See Section A.15
0x9800	Channel 8 Button Setup	0x120A	See Section A.13
0x9801		0x0019	See Section A.14
0x9802		0x3008	See Section A.15
0x9900	Channel 9 Button Setup	0x120A	See Section A.13
0x9901		0x0019	See Section A.14
0x9902		0x3008	See Section A.15
0x9A00	Channel 10 (Hall Switch) Button Setup	0x120A	See Section A.13
0x9A01		0x0019	See Section A.14
0x9A02		0x3008	See Section A.15
0x9B00	Reserved	0x120A	
0x9B01		0x0019	
0x9B02		0x3008	
Read-Write	**Channel Setup – ATI Parameters, Reference Channel and Rx Select**		

	Channel 0		
0xA000	CRX Select and General Channel Setup	0x11F3	See Section A.16
0xA001	ATI Base and Target	0x3E3D	See Section A.17
0xA002	Fine and Coarse Multipliers	-	See Section A.18
0xA003	ATI Compensation	-	See Section A.19
0xA004	Reference Channel Settings 0	0x0000	See Section A.20
0xA005	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 1		
0xA100	CRX Select and General Channel Setup	0x1113	See Section A.16
0xA101	ATI Base and Target	0x3E3D	See Section A.17
0xA102	Fine and Coarse Multipliers	-	See Section A.18
0xA103	ATI Compensation	-	See Section A.19
0xA104	Reference Channel Settings 0	0x0000	See Section A.20
0xA105	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 2		
0xA200	CRX Select and General Channel Setup	0x1123	See Section A.16
0xA201	ATI Base and Target	0x3E3D	See Section A.17
0xA202	Fine and Coarse Multipliers	-	See Section A.18
0xA203	ATI Compensation	-	See Section A.19
0xA204	Reference Channel Settings 0	0x0000	See Section A.20
0xA205	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 3		
0xA300	CRX Select and General Channel Setup	0x1143	See Section A.16
0xA301	ATI Base and Target	0x3E3D	See Section A.17
0xA302	Fine and Coarse Multipliers	-	See Section A.18
0xA303	ATI Compensation	-	See Section A.19
0xA304	Reference Channel Settings 0	0x0000	See Section A.20
0xA305	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 4		
0xA400	CRX Select and General Channel Setup	0x1183	See Section A.16
0xA401	ATI Base and Target	0x3E3D	See Section A.17
0xA402	Fine and Coarse Multipliers	-	See Section A.18
0xA403	ATI Compensation	-	See Section A.19
0xA404	Reference Channel Settings 0	0x0000	See Section A.20
0xA405	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 5		
0xA500	CRX Select and General Channel Setup	0x11F3	See Section A.16
0xA501	ATI Base and Target	0x3E3D	See Section A.17
0xA502	Fine and Coarse Multipliers	-	See Section A.18
0xA503	ATI Compensation	-	See Section A.19
0xA504	Reference Channel Settings 0	0x0000	See Section A.20
0xA505	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 6		
0xA600	CRX Select and General Channel Setup	0x1113	See Section A.16
0xA601	ATI Base and Target	0x3E3D	See Section A.17
0xA602	Fine and Coarse Multipliers	-	See Section A.18
0xA603	ATI Compensation	-	See Section A.19
0xA604	Reference Channel Settings 0	0x0000	See Section A.20
0xA605	Reference Channel Settings 1	0x0000	See Section A.21

	Channel 7		
0xA700	CRX Select and General Channel Setup	0x1123	See Section A.16
0xA701	ATI Base and Target	0x3E3D	See Section A.17
0xA702	Fine and Coarse Multipliers	-	See Section A.18
0xA703	ATI Compensation	-	See Section A.19
0xA704	Reference Channel Settings 0	0x0000	See Section A.20
0xA705	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 8		
0xA800	CRX Select and General Channel Setup	0x1143	See Section A.16
0xA801	ATI Base and Target	0x3E3D	See Section A.17
0xA802	Fine and Coarse Multipliers	-	See Section A.18
0xA803	ATI Compensation	-	See Section A.19
0xA804	Reference Channel Settings 0	0x0000	See Section A.20
0xA805	Reference Channel Settings 1	0x0000	See Section A.21
	Channel 9		
0xA900	CRX Select and General Channel Setup	0x1183	See Section A.16
0xA901	ATI Base and Target	0x3E3D	See Section A.17
0xA902	Fine and Coarse Multipliers	-	See Section A.18
0xA903	ATI Compensation	-	See Section A.19
0xA904	Reference Channel Settings 0	0x0000	See Section A.20
0xA905	Reference Channel Settings 1	0x0000	See Section A.21
	Hall Switch Channel		
0xAA00	Hall Sensor Setup	0x1103	See Section A.16
0xAA01	ATI Base and Target	0x3E38	See Section A.17
0xAA02	Fine and Coarse Multipliers	-	See Section A.18
0xAA03	ATI Compensation	-	See Section A.19
0xAA04	Reserved	0x0000	
0xAA05		0x0000	
	Hall Reference Channel		
0xAB00	Hall Sensor Setup	0x1103	See Section A.16
0xAB01	ATI Base and Target	0x3E3D	See Section A.17
0xAB02	Fine and Coarse Multipliers	-	See Section A.18
0xAB03	ATI Compensation	-	See Section A.19
0xAB04	Reserved	0x0000	
0xAB05		0x0000	
Read-Write	**Filter Betas**		
0xAC00	Filter Beta	0x7812	See Section A.22
0xAC01	Fast Filter Beta	0x0034	See Section A.23
Read-Write	**Slider 0 Setup**		
0xB000	Slider 0 General Setup	0x0000	See Section A.24
0xB001	Calibration and Bottom Speed	0x0000	See Section A.25
0xB002	Top Speed and Resolution	0x0000	See Section A.26
0xB003	Slider Enable Mask	0x0000	See Section A.27
0xB004	Slider Enable Status Link	0x0000	See Section A.28
0xB005	Delta Link 0	0x0000	See Section A.29
0xB006	Delta Link 1	0x0000	
0xB007	Delta Link 2	0x0000	
0xB008	Delta Link 3	0x0000	
0xB009	Gesture Setup 0	0x0000	See Section A.30
0xB00A	Gesture Setup 1	0x0000	See Section A.31
Read-Write	**Slider 1 Setup**		

0xB100	Slider 1 General Setup	0x0000	See Section A.24
0xB101	Calibration and Bottom Speed	0x0000	See Section A.25
0xB102	Top Speed and Resolution	0x0000	See Section A.26
0xB103	Slider Enable Mask	0x0000	See Section A.27
0xB104	Slider Enable Status Link	0x0000	See Section A.28
0xB105	Delta Link 0	0x0000	See Section A.29
0xB106	Delta Link 1	0x0000	
0xB107	Delta Link 2	0x0000	
0xB108	Delta Link 3	0x0000	
0xB109	Gesture Setup 0	0x0000	See Section A.30
0xB10A	Gesture Setup 1	0x0000	See Section A.31
Read-Write	**OUTA Settings**		
0xC000	OUTA Enable and Configuration Settings	0x0001	See Section A.32
0xC001	OUTA Mask	0x0021	See Section A.33
0xC002	OUTA Enable Status Link	0x06E8	See Section A.28
Read-Write	**PMU and System Settings**		
0xD0	Control settings	0x0030	See Section A.35
0xD1	ATI Error Timeout	0x0002	16-bit value * 0.5 (s)
0xD2	ATI Report Rate	0x0000	16-bit value (ms)
0xD3	Normal Power Mode Timeout	0x1388	16-bit value (ms)
0xD4	Normal Power Mode Report Rate	0x0010	16-bit value (ms) Range: 0 - 3000
0xD5	Low Power Mode Timeout	0x1388	16-bit value (ms)
0xD6	Low Power Mode Report Rate	0x003C	16-bit value (ms) Range: 0 - 3000
0xD7	Normal Power Update Rate in Ultra-low Power Mode	0x2710	16-bit value (ms)
0xD8	Ultra-low Power Mode Report Rate	0x0096	16-bit value (ms) Range: 0 - 3000
0xD9	ULP Entry Mask	0xFBDE	See Section A.36
0xDA	Event Enable Mask	0xFFFF	See Section A.37
0xDB	Hall Offset and Bias Current	0x20F0	See Section A.38
0xDC	I^2C Communication Settings	0x000C	See Section A.39
0xDD	I^2C Communication Timeout	0x01F4	See Section A.40

13 Implementation and Layout

13.1 Layout Fundamentals

Note: Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining the suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

13.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

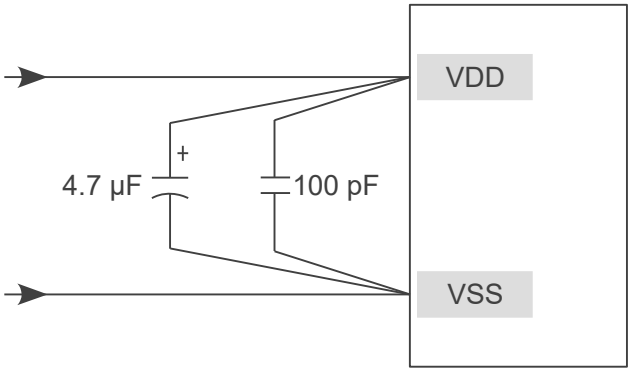


Figure 13.1: Recommended Power Supply Decoupling

13.1.2 VREG Capacitors

Each VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the IC. Figure 13.2 below shows an example placement of the VREG capacitors.

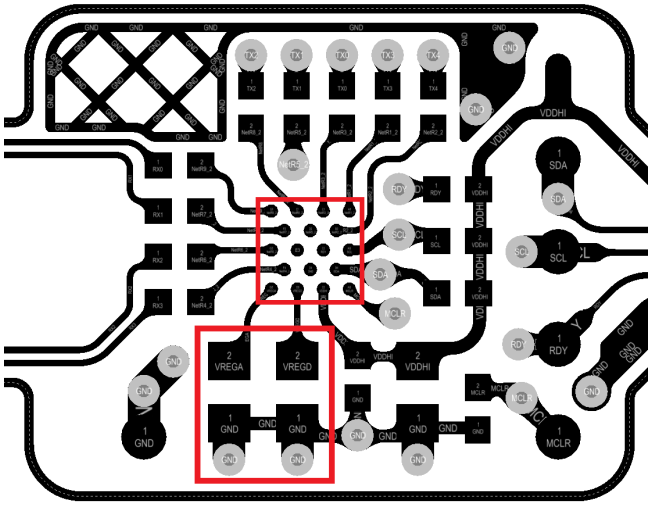


Figure 13.2: VREG Capacitor Placement Close to IC

13.1.3 WLCSP Light Sensitivity

The CSP package is sensitive to infrared light. When the silicon IC is subject to the photo-electric effect, an increase in leakage current is experienced. Due to the low power consumption of the IC this causes a change in signal and is common in the semiconductor industry with CSP devices.

If the IC could be exposed to IR in the product, then a dark glob-top epoxy material should cover the complete package to block infrared light. It is important to use sufficient material to completely cover the corners of the package. The glob-top also provides further advantages such as mechanical strength and shock absorption.

14 Ordering Information

14.1 Ordering Code

IQS7222A zzz ppb

Table 14.1: Order Code Description

IC NAME			IQS7222A IQS722xy[i]
POWER-ON CONFIGURATION	zzz	= 000 = 001 = 102	Blank device[i] I²C address 0x44 I²C address 0x57[ii]
PACKAGE TYPE	pp	= CS = QN = QF	WLCSP-18 package QFN-20 package QFN-20 package
BULK PACKAGING	b	= R	WLCSP-18 Reel (3000pcs/reel) QFN-20 Reel (2000pcs/reel)

Example : IQS7222A001QFR

14.2 Top Marking

14.2.1 WLCSP18 Package Marking

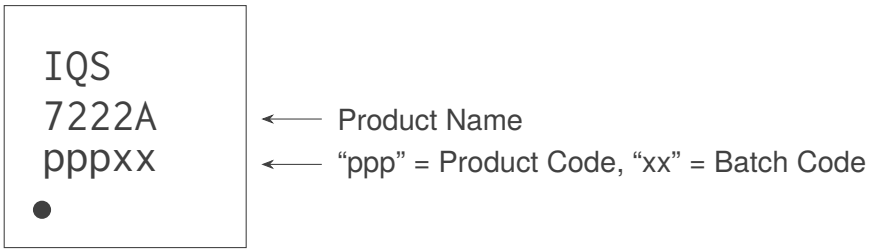


Figure 14.1: IQS7222A-WLCSP18 Package Top Marking

14.2.2 QFN20 Package Marking Option (IQS7222AzzzQNR)

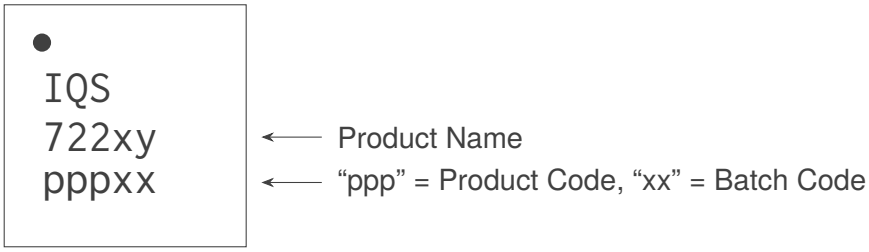


Figure 14.2: IQS722xy-QFN20 Package Top Marking

[i] Unprogrammed device. Can be configured with IQS7222A firmware.
[ii] Please refer to product information notice PIN-230172 for more details

14.2.3 QFN20 Package Marking Option (IQS7222AzzzQFR)

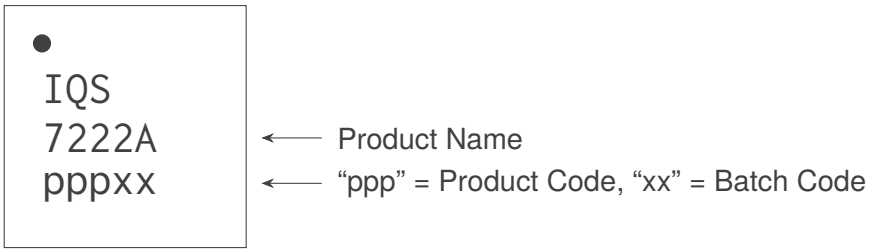


Figure 14.3: IQS7222A-QFN20 Package Top Marking

14.2.4 QFN20 Package Marking Option (IQS7222AzzzQFR, IQS722xy000QFR)

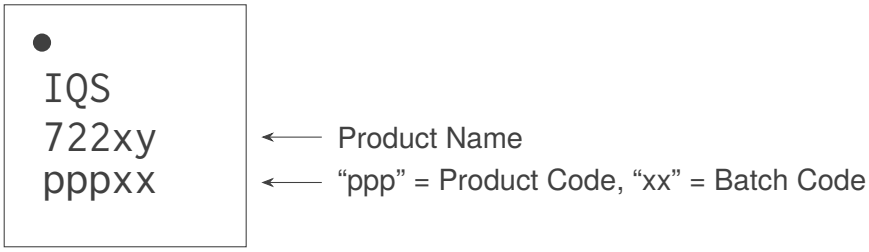


Figure 14.4: IQS722xy-QFN20 Package Top Marking

15 Package Specification

15.1 Package Outline Description – QFN20 (QFR)

This package outline is specific to order codes ending in *QFR*.

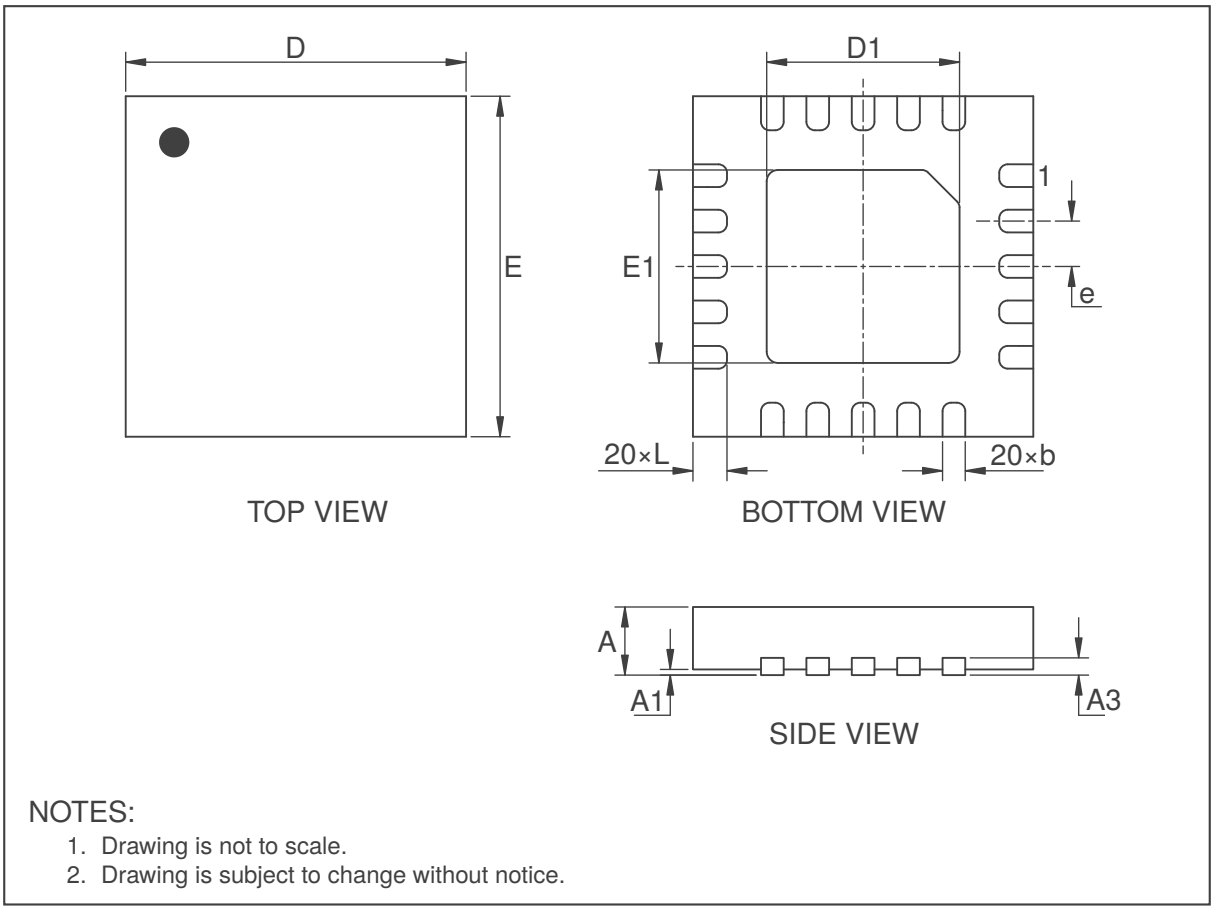
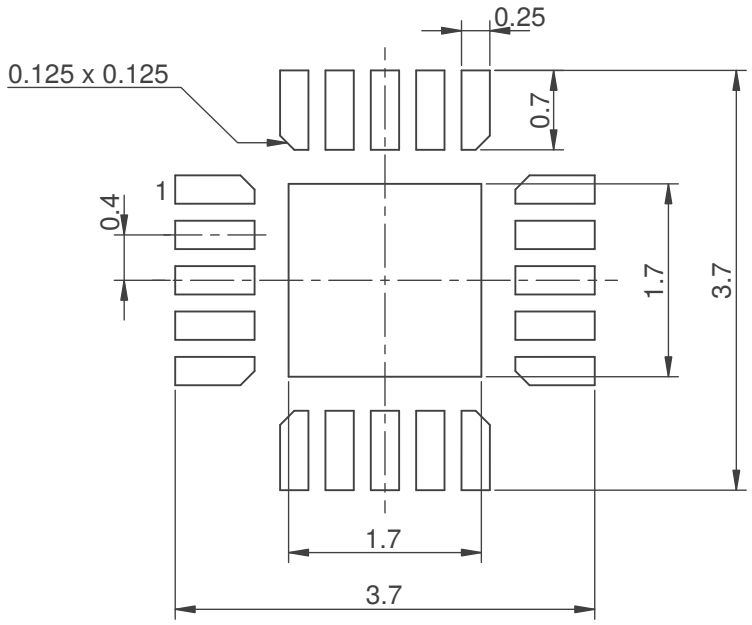


Figure 15.1: QFN (3x3)-20 (QFR) Package Outline Visual Description

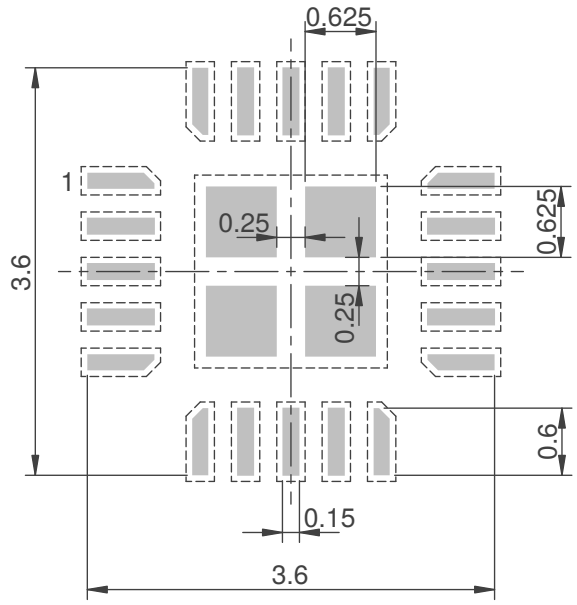
Table 15.1: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

15.2 Recommended PCB Footprint – QFN20 (QFR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 15.2: QFN (3x3)-20 (QFR) Recommended Footprint

15.3 Package Outline Description – QFN20 (QNR)

This package outline is specific to order codes ending in *QNR*.

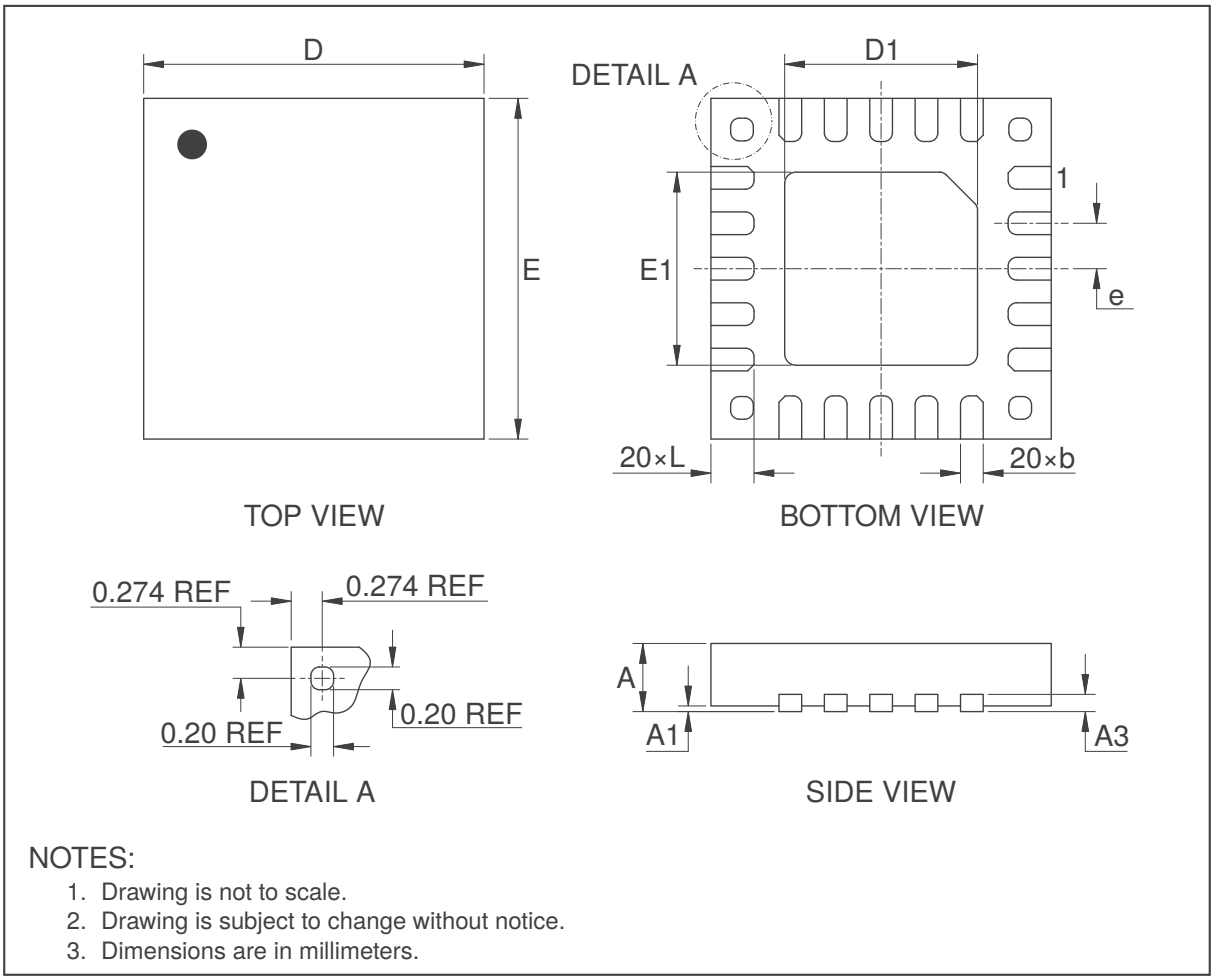
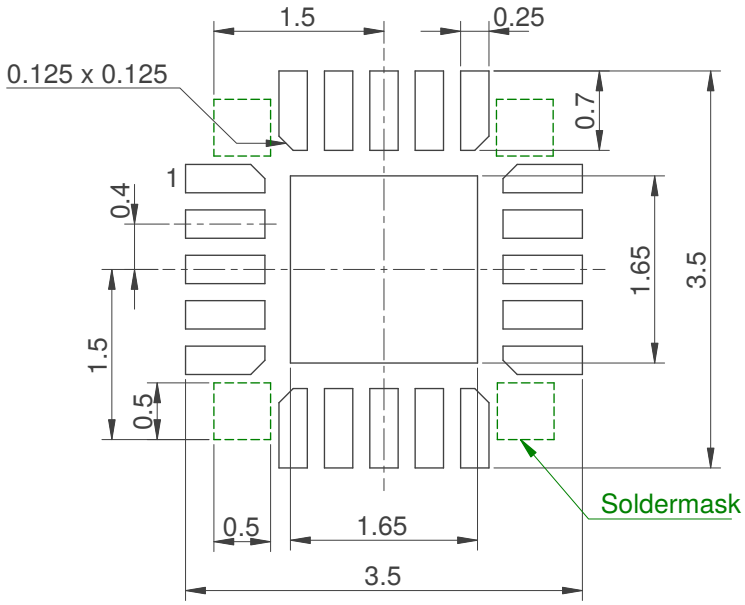


Figure 15.3: QFN (3x3)-20 (QNR) Package Outline Visual Description

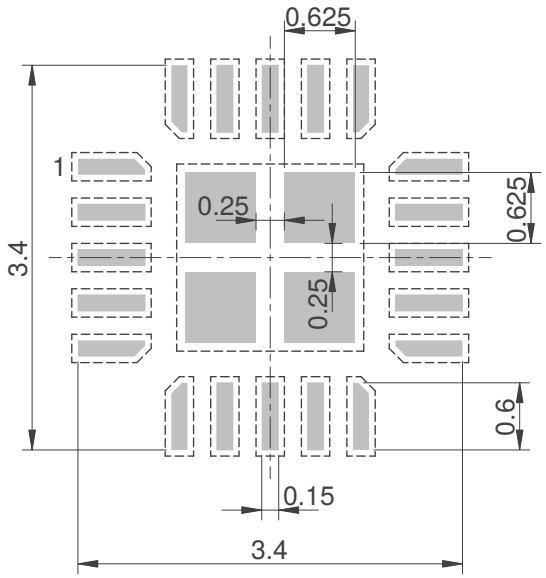
Table 15.2: QNR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0		0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
e		0.40 BSC	
L	0.33	0.38	0.43

15.4 Recommended PCB Footprint – QFN20 (QNR)



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board assembly site for solder paste stencil design recommendations.
6. Solder mask (or exposed copper keep-out) areas necessary to avoid any traces shorting to exposed corner pads.

Figure 15.4: QFN (3x3)-20 (QNR) Recommended Footprint

15.5 Package Outline Description – WLCSP18

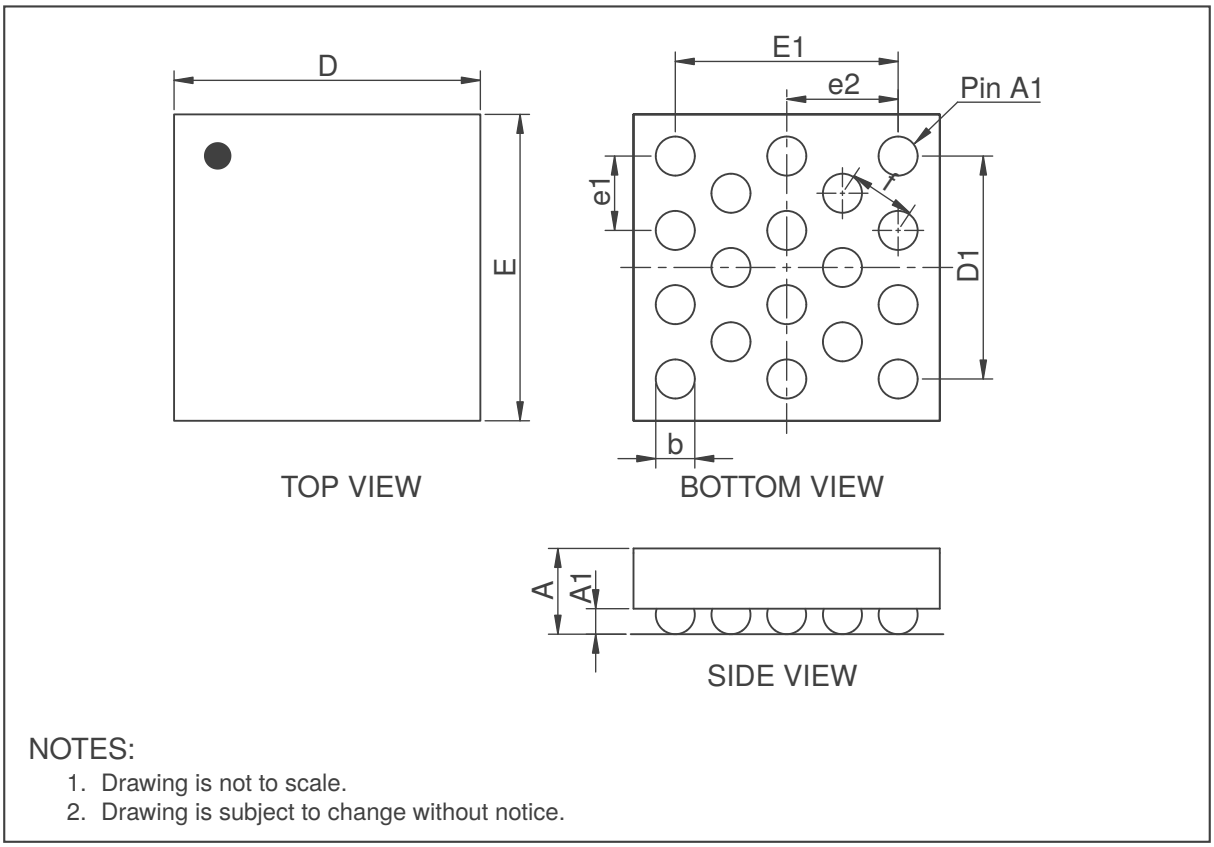
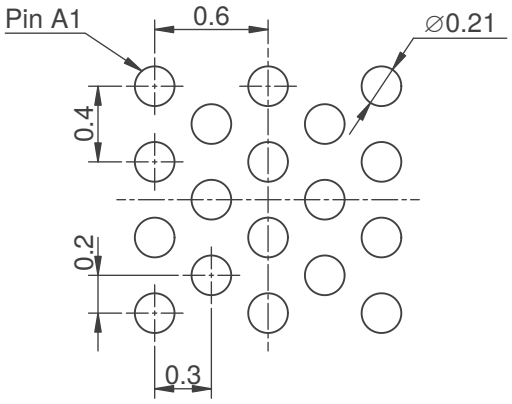


Figure 15.5: WLCSP (1.62x1.62)-18 Package Outline Visual Description

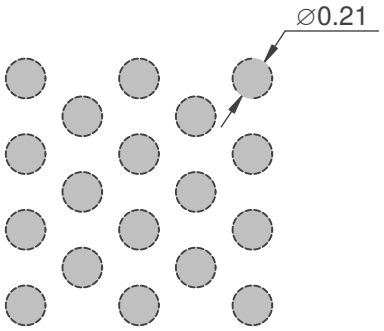
Table 15.3: WLCSP (1.62x1.62)-18 Package Dimensions [mm]

Dimension	Min	Nom	Max
A	0.477	0.525	0.573
A1	0.180	0.200	0.220
b	0.221	0.260	0.299
D	1.605	1.620	1.635
E	1.605	1.620	1.635
D1	1.200 BSC		
E1	1.200 BSC		
e1	0.400 BSC		
e2	0.600 BSC		
f	0.360 REF		

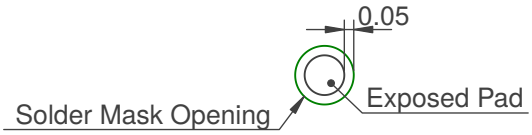
15.6 Recommended PCB Footprint – WLCSP18



RECOMMENDED FOOTPRINT



RECOMMENDED SOLDER PASTE APPLICATION



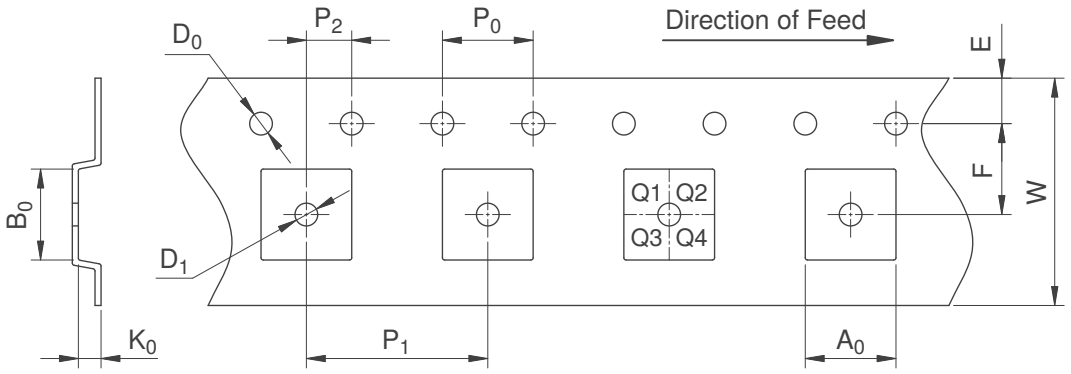
SOLDER MASK BACK-OFF

NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.
5. Customers should consult their board manufacturer for solder mask tolerances.
6. Customers should consult their board assembly site for solder paste stencil design recommendations.

Figure 15.6: WLCSP18 Recommended Footprint

15.7 Tape and Reel Specifications

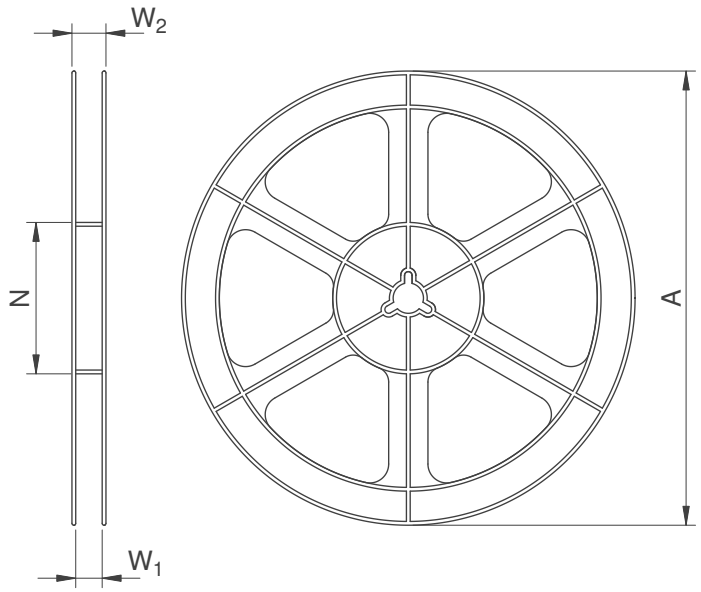


NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 15.7: Carrier Tape Specification

Table 15.4: Carrier Tape Dimensions [mm]

Dimension	Package		
	WLCSP18	QFN20 (QFR)	QFN20 (QNR)
A_0	1.78	3.30	3.30
B_0	1.78	3.30	3.30
K_0	0.69	0.75	0.80
D_0	1.50	1.50	1.55
D_1	0.50	1.55	1.50
E	1.75	1.75	1.75
F	3.50	5.50	5.50
P_0	4.00	4.00	4.00
P_1	4.00	8.00	8.00
P_2	2.00	2.00	2.00
W	8.00	12.00	12.00
Pin 1 Quadrant	Q1	Q2	Q2



NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 15.8: Reel Specification

Table 15.5: Reel Dimensions [mm]

Dimension	Package		
	WLCSP18	QFN20 (QFR)	QFN20 (QNR)
A	179	178	180
N	55	60	60
W_1	8.4	12.4	12.4
W_2 (Max)	14.4	18.4	18.4

15.8 Moisture Sensitivity Levels

Table 15.6: Moisture Sensitivity Levels

Package	MSL
QFN20	1
WLCSP18	1

15.9 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Please note: The value of all read-write bits marked as “Reserved”, unless otherwise specified, should not be modified. Individual bit fields should be modified using a read-modify-write procedure.

A.1 Version Information (0x00 – 0x09)

Address	Category	Name	Value	Order Code	
0x00	Application Version Info	Product Number	840		16-bit value
0x01		Major Version	1		
0x02		Minor Version	15	001	
			18	102[i]	
0x03		Patch Number (commit hash)	Reserved		
0x04					
0x05	ROM Library Version Info	Library Number	Reserved		
0x06		Major Version	Reserved		
0x07		Minor Version	Reserved		
0x08		Patch Number (commit hash)	Reserved		
0x09					

A.2 System Status (0x10)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Global Halt	Normal Power Update	Current Power Mode		Device Reset	Reserved	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global Halt not active
  - 1: Global Halt active. A channel with *Global Halt* setting enabled is in activation, and all other channels with *Global Halt* enabled have their LTAs halted.
- Bit 6: **Normal Power Update**
  - 0: No event
  - 1: Current report cycle is a normal power update cycle during ultra-low power mode. All channels were sampled and UIs updated.
- Bit 4-5: **Current Power Mode**
  - 0: Normal power mode
  - 1: Low power mode
  - 2: Ultra-low power mode
- Bit 3: **Device Reset**
  - 0: No event
  - 1: System reset occurred.
  - Bit cleared by setting the *Acknowledge Reset* bit in the *Control Settings* register.
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred. A channel failed to calibrate correctly.
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

[i] Please refer to product information notice PIN-230172 for more details

A.3 Events (0x11)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Power Event	ATI Event	Slider 1 Event	Slider 0 Event	Reserved	

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Touch Event	Proximity Event

- Bit 13: **Power Event**
  - 0: No event
  - 1: Power event occurred
  - Bit cleared on read
- Bit 12: **ATI Event**
  - 0: No event
  - 1: ATI event occurred
  - Bit cleared on read
- Bit 11: **Slider 1 Event**
  - 0: No event
  - 1: Gesture occurred on Slider 1
  - Bit cleared on read
- Bit 10: **Slider 0 Event**
  - 0: No event
  - 1: Gesture occurred on Slider 0
  - Bit cleared on read
- Bit 1: **Touch Event**
  - 0: No event
  - 1: Touch event occurred
  - Bit cleared on read
- Bit 0: **Proximity Event**
  - 0: No event
  - 1: Proximity event occurred
  - Bit cleared on read

A.4 Proximity Event States (0x12)

Bit	15	14	13	12	11	10	9	8
Description	Reserved					Hall	CH9	CH8

Bit	7	6	5	4	3	2	1	0
Description	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Proximity State**
  - 0: No event
  - 1: Proximity event active on respective channel

A.5 Touch Event States (0x13)

Bit	15	14	13	12	11	10	9	8
Description	Reserved					Hall	CH9	CH8

Bit	7	6	5	4	3	2	1	0
Description	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-10: **Channel Touch State**
  - 0: No event
  - 1: Touch event active on respective channel

A.6 Slider Gesture Status (0x16, 0x17)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Busy	Gesture Event	Negative	Reserved		Flick	Swipe	Tap

- Bit 7: **Busy**
  - 0: Slider not busy
  - 1: Slider busy. This is set as long as at least one of the slider channels is in activation (proximity or touch).
- Bit 6: **Gesture Event**
  - 0: No event
  - 1: Slider gesture event occurred. Cleared automatically after 1 report cycle.
- Bit 5: **Negative**
  - 0: Gesture event occurred in positive direction
  - 1: Gesture event occurred in negative direction
- Bit 2: **Flick**
  - 0: No event
  - 1: Flick event occurred. Cleared when *Busy* is cleared.
- Bit 1: **Swipe**
  - 0: No event
  - 1: Swipe event occurred. Cleared when *Busy* is cleared.
- Bit 0: **Tap**
  - 0: No event
  - 1: Tap event occurred. Cleared when *Busy* is cleared.

A.7 Cycle Setup 0 (0x8000, 0x8100, ...)

Applicable registers:

- Cycle 0: 0x8000
- Cycle 1: 0x8100
- Cycle 2: 0x8200
- Cycle 3: 0x8300
- Cycle 4: 0x8400
- Cycle 5: 0x8500
- Cycle 6: 0x8600

Bit	15	14	13	12	11	10	9	8
Description	Conversion Frequency Period							

Bit	7	6	5	4	3	2	1	0
Description	Conversion Frequency Fraction							

- Bit 8-15: **Conversion Frequency Period**
  - Controls the sensor conversion frequency
  - Range: 0 – 127

- Bit 0-7: **Conversion Frequency Fraction**
  - Fix to 127

It is recommended to fix the *Fraction* value to 127. For capacitive sensing, please refer to the following table to determine the *Period* value for the desired conversion frequency. The *Dead Time* setting must be enabled.

Table A.1: Supported Conversion Frequency Parameters for Capacitive Sensing

FRACTION	PERIOD	Conversion Frequency f_{xfer}
127	2	1.75 MHz
	3	1.40 MHz
	5	1.00 MHz
	7	778 kHz
	12	500 kHz
	16	389 kHz
	23	280 kHz

* The maximum recommended conversion frequency for self-capacitive sensing is 1 MHz. The maximum recommended conversion frequency for mutual-capacitive sensing is 2 MHz.

For inductive sensing, please refer to the following table to determine the *Period* value for the desired conversion frequency. The *Dead Time* setting must be disabled.

Table A.2: Supported Conversion Frequency Parameters for Inductive Sensing

FRACTION	PERIOD	Conversion Frequency f_{xfer}
127	0	7.00 MHz
	1	3.50 MHz
	2	2.33 MHz
	3	1.75 MHz
	4	1.40 MHz
	6	1.00 MHz
	8	778 kHz
	13	500 kHz

A.8 Cycle Setup 1 (0x8001, 0x8101, ...)

Applicable registers:

- Cycle 0: 0x8001
- Cycle 1: 0x8101
- Cycle 2: 0x8201
- Cycle 3: 0x8301
- Cycle 4: 0x8401

Bit	15	14	13	12	11	10	9	8
Description	CTX8	CTX7	CTX6	CTX5	CTX4	CTX3	CTX2	CTX1

Bit	7	6	5	4	3	2	1	0
Description	CTX0	Ground Inactive Rx Pins	Dead Time Enabled	FOSC Tx Frequency	Vbias Enabled	PXS Mode		

- Bit 7-15: **Tx Selection**
  - Selects which pin(s) provide the sensor excitation signal for the corresponding cycle/channels. For self-capacitive sensing, the same pin must be enabled for Tx and Rx. Not required for Hall sensing.
  - 0: CTx disabled
  - 1: CTx enabled
- Bit 6: **Ground Inactive Rx Pins**
  - 0: Float inactive Rx pins
  - 1: Ground inactive Rx pins (recommended)
- Bit 5: **Dead Time Enabled**
  - Adds a dead-time period during the sensor conversion. Must be *enabled* for self- and mutual-capacitive sensing, and *disabled* for inductive and Hall sensing.
  - 0: Dead time disabled
  - 1: Dead time enabled
- Bit 4: **FOSC Tx Frequency**
  - Use the system clock (f_{OSC}) as the excitation signal on the CTx pin (instead of using the configured conversion frequency). Recommended for inductive sensing only.
  - 0: Disabled
  - 1: Enabled
- Bit 3: **Vbias Enabled**
  - Enables a bias voltage output on CTx8 for biasing inductive sensing circuits. Generally not recommended.
  - 0: V_{bias} disabled
  - 1: V_{bias} enabled
- Bit 0-2: **PXS Mode**
  - Sets cycle sensing mode.
  - 0: None
  - 1: Self-capacitive
  - 2: Mutual capacitive
  - 3: Resonant inductance

A.9 Cycle Setup 2 (0x8002, 0x8102, ...)

Applicable registers:

- Cycle 0: 0x8002
- Cycle 1: 0x8102
- Cycle 2: 0x8202
- Cycle 3: 0x8302
- Cycle 4: 0x8402

Bit	15	14	13	12	11	10	9	8
Description	Reserved					Current Reference Enable	Current Reference Output	

Bit	7	6	5	4	3	2	1	0
Description	Current Reference Level				Current Reference Trim			

These settings are generally not used.

- Bit 10: **Current Reference Enable**
  - 0: Disable current reference
  - 1: Enable current reference
- Bit 8-9: **Current Reference Output**
  - 00: Disabled
- Bit 4-7: **Current Reference Level**
  - 4 bit value to scale current output
  - Higher values will result in a higher output current
- Bit 0-3: **Current Reference Trim**
  - 4 bit value to adjust current supply output
  - Higher values will result in a higher output current

A.10 Global Cycle Setup (0x8700)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	Maximum counts		Reserved				

Bit	7	6	5	4	3	2	1	0
Description	Reserved				ULP Conversion Count		Reserved	

- Bit 13-14: **Maximum Counts**
  - Sets the maximum counts of each conversion. This acts as a timeout, preventing a measurement from taking too long.
  - 0: 1023 counts
  - 1: 2047 counts
  - 2: 4095 counts
  - 3: 16383 counts
- Bit 2-3: **ULP Conversion Count**
  - When in ULP mode, this defines how many samples will be done by an autonomous circuit (sensing only CH0 and CH5) before waking up and processing the CH0 and CH5 LTAs. A higher value will ensure lowest possible power consumption where, e.g., 32 samples will be taken of CH0 and CH5 before the device wakes up to process LTAs.
  - 0: 4 samples
  - 1: 8 samples
  - 2: 16 samples
  - 3: 32 samples

A.11 ATI Coarse and Fine Dividers Preload (0x8701)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Fine Divider Preload					Reserved

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Coarse Divider Preload				

- Bit 9-13: **Fine Divider Preload**
  - 5-bit fine divider preload value.
  - This value is loaded into the *Fine Fractional Divider* field before an ATI event starts calibrating the *Coarse Fractional Multiplier*.
- Bit 0-4: **Coarse Divider Preload**
  - 5-bit coarse divider preload value.
  - This value is loaded into the *Coarse Fractional Divider* field before an ATI event starts calibrating the *Coarse Fractional Multiplier*.

A.12 ATI Compensation Preload (0x8702)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						ATI Compensation Preload	

Bit	7	6	5	4	3	2	1	0
Description	ATI Compensation Preload							

- Bit 0-9: **Compensation Preload**
  - 10-bit preload value.
  - This value is loaded into the *Compensation* field before an ATI event starts calibrating the *Compensation Divider*.

A.13 Button Setup 0 (0x9000, 0x9100, ...)

Applicable registers:

- Channel 0: 0x9000
- Channel 1: 0x9100
- Channel 2: 0x9200
- Channel 3: 0x9300
- Channel 4: 0x9400
- Channel 5: 0x9500
- Channel 6: 0x9600
- Channel 7: 0x9700
- Channel 8: 0x9800
- Channel 9: 0x9900
- Channel 10: 0x9A00

Bit	15	14	13	12	11	10	9	8
Description	Exit Debounce Value				Enter Debounce Value			

Bit	7	6	5	4	3	2	1	0
Description	Proximity Threshold							

- Bit 12-15: **Exit Debounce Value**
  - Sets the number of rapid conversions to perform before clearing a proximity event.
  - Range: 0 – 15
- Bit 8-11: **Enter Debounce Value**
  - Sets the number of rapid conversions to perform before setting a proximity event.
  - Range: 0 – 15
- Bit 0-7: **Proximity Threshold**
  - Sets the threshold (in counts) for proximity detection on a channel.
  - Range: 0 – 255 counts

A.14 Button Setup 1 (0x9001, 0x9101, ...)

Applicable registers:

- Channel 0: 0x9001
- Channel 1: 0x9101
- Channel 2: 0x9201

- Channel 3: 0x9301
- Channel 4: 0x9401
- Channel 5: 0x9501
- Channel 6: 0x9601
- Channel 7: 0x9701
- Channel 8: 0x9801
- Channel 9: 0x9901
- Channel 10: 0x9A01

Bit	15	14	13	12	11	10	9	8
Description	Touch Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Touch Threshold							

- Bit 8-15: **Touch Hysteresis**
  - Touch hysteresis value determines the release threshold, as a fraction of the touch threshold.
  - Range: 0 – 255 (maps to 0% to 100% hysteresis)
  - Release threshold can be determined as follows:

$$\frac{\text{LTA} \times \text{Threshold bit value}}{2^8} - \frac{\text{Threshold bit value} \times \text{Hysteresis bit value} \times \text{LTA}}{2^{16}}$$

- Bit 0-7: **Touch Threshold**
  - Sets the threshold for touch detection on a channel.
  - Range: 0 – 255
  - This threshold is specified as a fraction of the LTA:

$$\frac{\text{LTA}}{256} \times \text{8-bit value}$$

A.15 Button Setup 2 (0x9002, 0x9102, ...)

Applicable registers:

- Channel 0: 0x9002
- Channel 1: 0x9102
- Channel 2: 0x9202
- Channel 3: 0x9302
- Channel 4: 0x9402
- Channel 5: 0x9502
- Channel 6: 0x9602
- Channel 7: 0x9702
- Channel 8: 0x9802
- Channel 9: 0x9902

Bit	15	14	13	12	11	10	9	8
Description	Touch Event Timeout							

Bit	7	6	5	4	3	2	1	0
Description	Prox Event Timeout							

- Bit 8-15: **Touch Event Timeout**
  - Specifies how long a channel may be in a touch activation before the channel is automatically reseeded.
  - Range: 0 – 255
  - Timeout (ms) = 8-bit value × 500 ms

- 0: Never timeout (recommended for use with follower and reference channels and required for ULP entry channels retaining an active state in ULP).

- Bit 0-7: **Proximity Event Timeout**
  - Specifies how long a channel may be in a proximity state before the channel is automatically reseeded.
  - Range: 0 – 255
  - Timeout (ms) = 8-bit value × 500 ms
  - 0: Never timeout (recommended for use with follower and reference channels).

A.16 CRX Select and General Channel Setup (0xA000, 0xA100, ...)

Applicable registers:

- Channel 0: 0xA000
- Channel 1: 0xA100
- Channel 2: 0xA200
- Channel 3: 0xA300
- Channel 4: 0xA400

Bit	15	14	13	12	11	10	9	8
Description	Reference Mode		ATI Band		Global halt	Invert	Dual	Enabled

Bit	7	6	5	4	3	2	1	0
Description	CRX3	CRX2	CRX1	CRX0	Cs Size	Vref 0.5 V	Projected Bias	

Applicable registers:

- Channel 5: 0xA500
- Channel 6: 0xA600
- Channel 7: 0xA700
- Channel 8: 0xA800
- Channel 9: 0xA900

Bit	15	14	13	12	11	10	9	8
Description	Reference Mode		ATI Band		Global Halt	Invert	Dual	Enabled

Bit	7	6	5	4	3	2	1	0
Description	CRX7	CRX6	CRX5	CRX4	Cs Size	Vref 0.5 V	Projected Bias	

Applicable registers:

- Channel 10: 0xAA00
- Channel 11: 0xAB00

Bit	15	14	13	12	11	10	9	8
Description	Reserved		ATI Band		Global Halt	Invert	Dual	Enabled

Bit	7	6	5	4	3	2	1	0
Description	Reserved				Cs Size	Vref 0.5 V	Projected Bias	

- Bit 14-15: **Reference Mode**
  - 0: Independent

- 1: Reference
- 2: Follower
- Not applicable to Hall channels

- Bit 12-13: **ATI band**
  - Sets boundaries around the target value. If the LTA of the channel drifts outside these boundaries, the channel will automatically reseed.
  - Additionally, if the channel's counts are outside these boundaries directly after an ATI is complete, an *ATI Error* is raised.
  - 0: Target / 16
  - 1: Target / 8
  - 2: Target / 4
  - 3: Target / 2
- Bit 11: **Global halt**
  - If enabled, the LTA on the channel will halt when any other channel with global halt enabled is in a proximity/touch state. The function is aimed at slider applications.
  - 0: Global halt disabled
  - 1: Global halt enabled
- Bit 10: **Invert Direction**
  - Changes the direction of the channel's delta calculation, allowing events to be detected on an *increase* in counts. Must be enabled for mutual capacitive and inductive sensing mode.
  - 0: Invert direction disabled
  - 1: Invert direction enabled
- Bit 9: **Bi-directional Sensing**
  - Allows events to be detected for *increase and decrease* in counts.
  - 0: Bi-directional sensing disabled
  - 1: Bi-directional sensing enabled
- Bit 8: **Channel Enabled**
  - 0: Channel disabled
  - 1: Channel sensing and processing enabled
- Bit 4-7: **CRx Selection**
  - Assigns a sensing pin to the channel.
  - Pin assignments are dependent on channel/prox engine selection.
    - Channels 0 – 4 may use CRx0 – CRx3.
    - Channels 5 – 9 may use CRx4 – CRx7.
    - Channels 10 and 11 do not require external pin connections.
  - 0: CRx disabled
  - 1: CRx enabled
- Bit 3: **Cs Size**
  - Sets the size of the internal sampling capacitor.
  - 0: 40 pF
  - 1: 80 pF (recommended)
- Bit 2: **Vref 0.5V**
  - Decreases threshold voltage of internal sampling capacitor, effectively halving its size.
  - 0: Vref 0.5 V disabled (Recommended)
  - 1: Vref 0.5 V enabled
- Bit 0-1: **Projected Bias Select**
  - 0: 2 µA
  - 1: 5 µA
  - 2: 7 µA
  - 3: 10 µA (Recommended)

A.17 ATI Base and Target (0xA001, 0xA101, ...)

Applicable registers:

- Channel 0: 0xA001
- Channel 1: 0xA101

- Channel 2: 0xA201
- Channel 3: 0xA301
- Channel 4: 0xA401
- Channel 5: 0xA501
- Channel 6: 0xA601
- Channel 7: 0xA701
- Channel 8: 0xA801
- Channel 9: 0xA901
- Channel 10: 0xAA01
- Channel 11: 0xAB01

Bit	15	14	13	12	11	10	9	8
Description	ATI Target							

Bit	7	6	5	4	3	2	1	0
Description	ATI Base					ATI Mode		

- Bit 8-15: **ATI Target**
  - Range: 0 – 255
  - Target (counts) = 8-bit value × 8
- Bit 3-7: **ATI Base**
  - Range: 0 – 31
  - Base (counts) = 5-bit value × 16
- Bit 0-2: **ATI Mode**
  - 0: ATI Disabled
  - 1: Compensation only
  - 2: ATI from compensation divider
  - 3: ATI from fine fractional divider
  - 4: ATI from coarse fractional divider
  - 5: Full ATI

A.18 Fine and Coarse Multipliers (0xA002, 0xA102, ...)

Applicable registers:

- Channel 0: 0xA002
- Channel 1: 0xA102
- Channel 2: 0xA202
- Channel 3: 0xA302
- Channel 4: 0xA402
- Channel 5: 0xA502
- Channel 6: 0xA602
- Channel 7: 0xA702
- Channel 8: 0xA802
- Channel 9: 0xA902
- Channel 10: 0xAA02
- Channel 11: 0xAB02

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Fine Fractional Divider					Coarse Fractional Multiplier

Bit	7	6	5	4	3	2	1	0
Description	Coarse Fractional Multiplier			Coarse Fractional Divider				

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

A.19 ATI Compensation (0xA003, 0xA103, ...)

Applicable registers:

- Channel 0: 0xA003
- Channel 1: 0xA103
- Channel 2: 0xA203
- Channel 3: 0xA303
- Channel 4: 0xA403
- Channel 5: 0xA503
- Channel 6: 0xA603
- Channel 7: 0xA703
- Channel 8: 0xA803
- Channel 9: 0xA903
- Channel 10: 0xAA03
- Channel 11: 0xAB03

Bit	15	14	13	12	11	10	9	8
Description	Compensation Divider					Reserved	Compensation Selection	

Bit	7	6	5	4	3	2	1	0
Description	Compensation Selection							

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

A.20 Reference Channel Settings 0 (0xA004, 0xA104, ...)

Applicable registers:

- Channel 0: 0xA004
- Channel 1: 0xA104
- Channel 2: 0xA204
- Channel 3: 0xA304
- Channel 4: 0xA404

- Channel 5: 0xA504
- Channel 6: 0xA604
- Channel 7: 0xA704
- Channel 8: 0xA804
- Channel 9: 0xA904

Bit	15	14	13	12	11	10	9	8
Description	Reference Follower Mask Link Ptr/ Sensor Mask							

Bit	7	6	5	4	3	2	1	0
Description	Reference Follower Mask Link Ptr/ Sensor Mask							

- The register value is used for either Follower Mask Link Ptr or Reference Sensor Ptr based on the *Mode* selected in Section A.16, bit 14-15.
- Bit 0-15: **Reference Follower Mask Link Ptr**
  - Applicable if *Mode* = 'Reference'
  - 0x6E6 (decimal = 1766): Proximity
  - 0x6E8 (decimal = 1768): Touch
- Bit 0-15: **Sensor Mask**
  - Applicable if *Mode* = 'Follower'
  - 0x000 (decimal = 0): None
  - 0x418 (decimal = 1048): Channel 0
  - 0x442 (decimal = 1090): Channel 1
  - 0x46C (decimal = 1132): Channel 2
  - 0x496 (decimal = 1174): Channel 3
  - 0x4C0 (decimal = 1216): Channel 4
  - 0x4EA (decimal = 1258): Channel 5
  - 0x514 (decimal = 1300): Channel 6
  - 0x53E (decimal = 1342): Channel 7
  - 0x568 (decimal = 1384): Channel 8
  - 0x592 (decimal = 1426): Channel 9

A.21 Reference Channel Settings 1 (0xA005, 0xA105, ...)

Applicable registers:

- Channel 0: 0xA005
- Channel 1: 0xA105
- Channel 2: 0xA205
- Channel 3: 0xA305
- Channel 4: 0xA405
- Channel 5: 0xA505
- Channel 6: 0xA605
- Channel 7: 0xA705
- Channel 8: 0xA805
- Channel 9: 0xA905

The register value is used for either Follower Mask or Reference Weight based on the *Mode* selected in Section A.16, bit 14-15.

If *Mode* = 'Reference':

Bit	15	14	13	12	11	10	9	8
Description	Reference Follower Mask/ Reference Sensor Weight							

Bit	7	6	5	4	3	2	1	0
Description	Reference Follower Mask/ Reference Sensor Weight							

- Bit 0-9: **Reference Follower Mask**
  - Used to enable current sensor as a reference channel for the selected channel.
  - E.g., if CH6 bit is set, this channel is used as a reference for channel 6.

If *Mode* = 'Follower':

Bit	15	14	13	12	11	10	9	8
Description	Reference Follower Mask/ Reference Sensor Weight							

Bit	7	6	5	4	3	2	1	0
Description	Reference Follower Mask/ Reference Sensor Weight							

- Bit 0-15: **Reference Weight**
  - Range: 0 – 255
  - 16-bit decimal value / 256

A.22 Filter Betas (0xAC00)

Bit	15	14	13	12	11	10	9	8
Description	LTA Low Power Beta				LTA Normal Power Beta			

Bit	7	6	5	4	3	2	1	0
Description	Counts Low Power Beta				Counts Normal Power Beta			

- Bit 12-15: **LTA Filter Low Power Beta**
  - Sets the responsiveness of the LTA filter in low power mode.
  - Higher values filter out more noise at the expense of responsiveness.
  - Range: 0 – 15
  - 0: No filtering
- Bit 8-11: **LTA Filter Normal Power Beta**
  - Sets the responsiveness of the LTA filter in normal power mode.
  - Higher values filter out more noise at the expense of responsiveness.
  - Range: 0 – 15
  - 0: No filtering
- Bit 4-7: **Counts Filter Low Power Beta**
  - Sets the responsiveness of the counts filter in low power mode.
  - Higher values filter out more noise at the expense of responsiveness.
  - Range: 0 – 15
  - 0: No filtering
- Bit 0-3: **Counts Filter Normal Power Beta**
  - Sets the responsiveness of the counts filter in normal power mode.
  - Higher values filter out more noise at the expense of responsiveness.
  - Range: 0 – 15
  - 0: No filtering

A.23 Fast Filter Betas (0xAC01)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	LTA Low Power Fast Beta				LTA Normal Power Fast Beta			

- Bit 4-7: **LTA Filter Low Power Fast Beta**
  - LTA filter beta value used for negative deltas.
  - Negative deltas suggest an unexpected decrease in signal, and such events are typically ignored. It is recommended to use a small value here to allow the LTA to effectively reseed to the raw counts value.
  - Unused if *Bi-Directional Sensing* is enabled.
  - Range: 0 – 15
  - 0: No filtering
- Bit 0-3: **LTA Filter Normal Power Fast Beta**
  - LTA filter beta value used for negative deltas.
  - Negative deltas suggest an unexpected decrease in signal, and such events are typically ignored. It is recommended to use a small value here to allow the LTA to effectively reseed to the raw counts value.
  - Unused if *Bi-Directional Sensing* is enabled.
  - Range: 0 – 15
  - 0: No filtering

1

A.24 Slider General Setup (0xB000, 0xB100)

Bit	15	14	13	12	11	10	9	8
Description	Lower Calibration							

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Static Filter	Bottom/Static Beta			Total Channels		

- Bit 8-15: **Lower Calibration**
  - Lower Calibration Value is used to offset the end-points of the slider position so that they match the end-points of the physical slider.
  - Range: 0 – 255 (pixels)
- Bit 6: **Static Filter**
  - If the Static Filter bit is set, the *Bottom/Static Beta* is used to filter the slider position regardless of the touch's movement speed. This is an IIR filter beta value as described in AZD004.
  - 0: Static filter disabled
  - 1: Static filter enabled
- Bit 3-5: **Bottom/Static Beta**
  - Sets the filter beta value to use when filtering the slider position at low speeds.
  - Range: 0 – 7
  - 0: No filtering
- Bit 0-2: **Total Channels**
  - Sets the total number of channels used to create the slider.
  - 0: Disabled
  - 2: 2 Channels
  - 3: 3 Channels
  - 4: 4 Channels

A.25 Slider Calibration and Bottom Speed (0xB001, 0xB101)

Bit	15	14	13	12	11	10	9	8
Description	Bottom Filter Speed							

Bit	7	6	5	4	3	2	1	0
Description	Upper Calibration							

- Bit 8-15: **Bottom Filter Speed**
  - If the speed of the slider gesture is below this value, the slider position is filtered using the *Bottom/Static Beta*.
  - Range: 0 – 255 (speed value, pixels per sample)
- Bit 0-7: **Upper Calibration**
  - Upper Calibration Value is used to offset the end-points of the slider position so that they match the end-points of the physical slider.
  - Range: 0 – 255 (pixels)

A.26 Slider Top Speed and Resolution (0xB002, 0xB102)

Bit	15	14	13	12	11	10	9	8
Description	Resolution							

Bit	7	6	5	4	3	2	1	0
Description	Top Speed							

- Bit 8-15: **Resolution**
  - Sets the resolution of the filter position calculation
  - Range: 0 – 255
  - Resolution = 8-bit value × 16 (pixels)
- Bit 0-7: **Top Speed**
  - Sets speed at which the slider tops filtering the position, and uses the raw position value.
  - Range: 0 – 255
  - Top speed = 8-bit value × 4 (pixels per sample)
  - 0: Disables all slider filtering

A.27 Slider Enable Mask (0xB003, 0xB103)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						CH9	CH8

Bit	7	6	5	4	3	2	1	0
Description	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-9: **Slider Channel Enable Mask**
  - Enable channels for slider processing. The IQS7222A performs slider calculations only when one of the enabled channels are in a proximity/touch state. If none of the enabled channels are in activation, slider processing is skipped.
  - All channels required for slider application must be selected.

A.28 Slider Enable Status Link (0xB004, 0xB104)

Bit	15	14	13	12	11	10	9	8
Description	Enable Status Link							

Bit	7	6	5	4	3	2	1	0
Description	Enable Status Link							

- Bit 0-15: **Slider Enable Status Link**
  - Sets whether slider channels should be in proximity or in touch state in order for slider processing to occur.
  - 0x6E6 (decimal = 1766): Output linked to channel prox
  - 0x6E8 (decimal = 1768): Output linked to channel touch

A.29 Delta Link (0xB005, 0xB105)

Applicable registers:

- Slider 0: 0xB004, 0xB005, 0xB006, 0xB007
- Slider 1: 0xB104, 0xB105, 0xB106, 0xB107

Bit	15	14	13	12	11	10	9	8
Description	Delta Link							

Bit	7	6	5	4	3	2	1	0
Description	Delta Link							

- Bit 0-15: **Delta Link**
  - Sets which channels' delta values are used to calculate slider position.
  - Delta link number (e.g. *Delta Link 0* or *Delta Link 2*) corresponds with slider element order.
  - 0x000 (decimal = 0): Disabled
  - 0x438 (decimal = 1080): Channel 0 enabled for element
  - 0x462 (decimal = 1122): Channel 1 enabled for element
  - 0x48C (decimal = 1164): Channel 2 enabled for element
  - 0x4B6 (decimal = 1206): Channel 3 enabled for element
  - 0x4E0 (decimal = 1248): Channel 4 enabled for element
  - 0x50A (decimal = 1290): Channel 5 enabled for element
  - 0x534 (decimal = 1332): Channel 6 enabled for element
  - 0x55E (decimal = 1374): Channel 7 enabled for element
  - 0x588 (decimal = 1416): Channel 8 enabled for element
  - 0x5B2 (decimal = 1458): Channel 9 enabled for element

A.30 Gesture Setup 0 (0xB009, 0xB109)

Bit	15	14	13	12	11	10	9	8
Description	Maximum Tap Time							

Bit	7	6	5	4	3	2	1	0
Description	Minimum Gesture Time					Flick Gesture Enable	Swipe Gesture Enable	Tap Gesture Enable

- Bit 8-15: **Maximum Tap Time**
  - Sets the maximum duration of a touch on the slider for a valid tap gesture. If a touch lasts longer than this time, the tap is rejected.
  - Range: 0 – 255

- Maximum tap time = 8-bit value × 16 (ms)

› Bit 3-7: **Minimum Gesture Time**
- Sets the minimum duration of a touch on the slider for a valid gesture. If a touch is shorter than this time, the gesture is rejected.
- This minimum duration is applicable for tap, swipe, and flick gestures.
- Range: 0 – 31
- Minimum time = 5-bit value × 16 (ms)

› Bit 2: **Flick Gesture Enable**
- A flick gesture will be reported if the touch lasts longer than the *Minimum Gesture Time* but less than the *Maximum Swipe Time*. (i.e. *Minimum Gesture Time* ≤ Touch Duration ≤ *Maximum Swipe Time*.) Additionally, the total distance travelled by the finger during the touch must be greater than the *Minimum Swipe Distance*.
- 0: Flick Disabled
- 1: Flick Enabled

› Bit 1: **Swipe Gesture Enable**
- A swipe gesture will be reported if the touch lasts longer than the *Minimum Gesture Time*, and the total distance travelled by the finger during the touch is greater than the *Minimum Swipe Distance*.
- 0: Swipe Disabled
- 1: Swipe Enabled

› Bit 0: **Tap Gesture Enable**
- A tap gesture will be reported if the touch lasts longer than the *Minimum Gesture Time* but less than the *Maximum Tap Time*. (i.e. *Minimum Gesture Time* ≤ Touch Duration ≤ *Maximum Tap Time*.) Additionally, the total distance travelled by the finger during the touch must be less than the *Minimum Swipe Distance*.
- 0: Tap Disabled
- 1: Tap Enabled

A.31 Gesture Setup 1 (0xB00A, 0xB10A)

Bit	15	14	13	12	11	10	9	8
Description	Minimum Swipe Distance							

Bit	7	6	5	4	3	2	1	0
Description	Maximum Swipe Time							

› Bit 8-15: **Minimum Swipe Distance**
- Minimum distance from the touch starting location for a valid swipe gesture. A swipe is reported as soon as this minimum distance is reached, provided the duration of the touch is longer than the *Minimum Gesture Time* and shorter than the *Maximum Swipe Time*.
- This also sets an upper bound for the total movement during a tap event.
- Range: 0 – 255
- Distance = 8-bit value × 16 (pixels)

› Bit 0-7: **Maximum Swipe Time**
- If the touch is released before the time specified in Maximum Swipe Time, a flick is reported. Otherwise, a swipe is reported.
- Once this time expires, a swipe or flick will no longer be reported until a new touch event begins.
- Range: 0 – 255
- Maximum Swipe Time = 8-bit value × 16 (ms)

A.32 OUTA Enable and Configuration Settings (0xC000)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Configuration	Enable

- Bit 1: **Output Configuration**
  - 0: Push-pull active high logic
  - 1: Open-drain active low logic (requires additional pull-up resistance to VDD level, no internal pull-up)
- Bit 0: **Enable**
  - Allows the state of a channel (or multiple channels, or a slider gesture) to be given on the OUTA pin. The active state of the pin (during an event) is controlled by the *Output Configuration* bit.
  - 0: OUTA Output disabled
  - 1: OUTA Output Enabled

A.33 OUTA Enable Mask (0xC001)

If *OUTA Status Link* is set to channel Prox/Touch (0x06E6/0x06E8), the enable mask format is as follows:

Bit	15	14	13	12	11	10	9	8
Description	Reserved					CH10	CH9	CH8

Bit	7	6	5	4	3	2	1	0
Description	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

- Bit 0-9: **Channel Enable Mask**
  - OUTA pin is active when any of the enabled channels are in activation.
  - More than one channel can be selected as an output.

If *OUTA Status Link* is set to slider events (0x0620/0x063E), the enable mask format is as follows:

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved					Flick	Swipe	Tap

- Bit 2: **Flick Enable**
  - Set OUTA pin active when a flick event is detected.
- Bit 1: **Swipe Enable**
  - Set OUTA pin active when a swipe event is detected.
- Bit 0: **Tap Enable**
  - Set OUTA pin active when a tap event is detected.

A.34 OUTA Enable Status Link (0xC002)

Bit	15	14	13	12	11	10	9	8
Description	Enable Status Link							

Bit	7	6	5	4	3	2	1	0
Description	Enable Status Link							

- Bit 0-15: **OUTA Enable Status Link**
  - 0x06E6 (decimal = 1766): Output linked to channel proximity states
  - 0x06E8 (decimal = 1768): Output linked to channel touch states
  - 0x0620 (decimal = 1568): Output linked to Slider 0 events
  - 0x063E (decimal = 1598): Output linked to Slider 1 events

A.35 Control Settings (0xD0)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Interface Type		Power Mode		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bit 6-7: **Interface Selection**
  - 0: I²C streaming
  - 1: I²C event mode
  - 2: I²C streaming in touch
- Bit 4-5: **Power Mode Selection**
  - 0: Normal power
  - 1: Low power
  - 2: Ultra-low Power
  - 3: Automatic power mode switching
- Bit 3: **Execute Reseed Command**
  - 0: No action
  - 1: Reseed
  - Bit cleared automatically
- Bit 2: **Execute ATI Command**
  - 0: No action
  - 1: ATI
  - Bit cleared automatically
- Bit 1: **Soft Reset**
  - 0: No action
  - 1: Reset device
  - Bit cleared automatically
- Bit 0: **Acknowledge Reset**
  - 0: No action
  - 1: Acknowledge reset
  - Bit cleared automatically

A.36 Channel ULP Entry Mask (0xD9)

Bit	15	14	13	12	11	10	9	8
Description	Reserved					Ch10	Ch9	Ch8

Bit	7	6	5	4	3	2	1	0
Description	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

- Bit 0-9: **Channel ULP Entry Mask**
  - If entry is masked (bit is set), then the touch/proximity event on a specific channel will keep the device in a higher power mode for quick reaction speed. In such case, only when there is no touch/proximity, the device will enter lowest power mode.
  - If the entry is unmasked (bit is cleared), the device will be allowed to enter ULP even in proximity or touch state. In some applications like wear detection, unmasked behaviour is best to track long term wear and get best power consumption.
  - All channels required to enter ULP with an active prox/touch state must be unmasked.

A.37 Event Mask (0xDA)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Power Event	ATI Event	Slider 1	Slider 0	Reserved	

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Touch Event	Prox Event

- This sets which events (from the *Events* register) will open an automatic communication window when in event mode.
- Bit 13: **Power Event**
  - 0: Power event disabled
  - 1: Power event enabled
- Bit 12: **ATI Event**
  - 0: ATI event disabled
  - 1: ATI event enabled
- Bit 11: **Slider 1 Event**
  - 0: Slider 1 event disabled
  - 1: Slider 1 event enabled
- Bit 10: **Slider 0 Event**
  - 0: Slider 0 event disabled
  - 1: Slider 0 event enabled
- Bit 1: **Touch Event**
  - 0: Touch event disabled
  - 1: Touch event enabled
- Bit 0: **Prox Event**
  - 0: Prox event disabled
  - 1: Prox event enabled

A.38 Hall Bias and Offset Current (0xDB)

Bit	15	14	13	12	11	10	9	8
Description	Hall Coarse Offset				Hall Fine Offset			

Bit	7	6	5	4	3	2	1	0
Description	Boost Gain	Hall Bias						

- Bit 12-15: **Hall Coarse Offset**
  - Coarse offset current in 3 µA steps.
  - Range -21 µA to 21 µA
- Bit 8-11: **Hall Fine Offset**
  - 4 bit value * 200 (nA)
- Bit 7: **Boost Gain**
  - 0: Boost gain disabled
  - 1: Boost gain enabled
- Bit 0-6: **Hall Bias Current**
  - 7 bit value

A.39 I²C Communication Settings (0xDC)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved						RW Check Disabled	Stop Bit Disabled

- Bit 1: **RW Check Disabled**
  - 0: Write protection enabled on all read-only registers
  - 1: Writes allowed to read only registers
- Bit 0: **Stop Bit Disabled**
  - 0: I²C communication window terminated by stop bit.
  - 1: I²C communication window not terminated by stop bit. Send 0xFF to slave address to terminate window.

A.40 I²C Communication Timeout (0xDD)

Bit	15	14	13	12	11	10	9	8
Description	I²C Communication Timeout							

Bit	7	6	5	4	3	2	1	0
Description	I²C Communication Timeout							

- **Note:** To write to this register over I²C, the register's address (0xDD) must be commanded explicitly before writing data i.e. in a separate I²C write setup command.
- Bit 0-15: **I²C Communication Timeout**
  - Range: 0 - 65535 (ms)
  - Default = 500 ms

B Known Issues

B.1 I²C Polling During Start-up

Polling during start-up may result in device lockup. Suspend polling for at least 25ms after receiving a NACK.

The I²C initialize can fail if one of the I²C lines have been kept low for longer than 50ms.

B.2 Tap Gestures Reported During Swipes

A Tap and Swipe Event is possible at the same time under the following conditions:

- Swipe is made above the minimum swipe distance – then the swipe flag gets set.
- Without lifting off the slider, the swipe is retracted towards the original start position, reducing the total distance moved to less than the minimum swipe distance – the swipe flag remains set from before.
- The slider is then released. If this is all done under the maximum tap time, the tap flag is also set.
- In such case, both a SWIPE and TAP event will be reported.
- Maximum Tap Time may be adapted to limit accidental triggers of both events.

B.3 ATI Power Mode Issue

- When signal drift is present in a low-power mode, an auto-ATI event is possible to ensure the signal is in an optimal operating range.
- In order code version "102" and above, the auto-ATI event will wake the IC from LP or ULP mode, causing it to spend the preset times to step down to low power modes again. In cases where significant signal drift is expected, this effect could affect battery life calculations.
- For optimal battery life it is recommended to use the ATI events to manually put the IC back into the lowest power mode and reinstate auto power modes after that. Please contact Azoteq for sample code to achieve this.

B.4 Force Communication Request may Close a Communication Window

A force communication request (0xFF command) may unintentionally close a communication window instead of opening it. This occurs if the IQS7222A receives the force communication request while the RDY is low. The I²C STOP condition at the end of the 0xFF byte triggers the IQS7222A to close its communication window, causing the RDY to go back high immediately. This may also happen if the communication window automatically opens during the transmission of the 0xFF byte, as shown in Figure B.1.

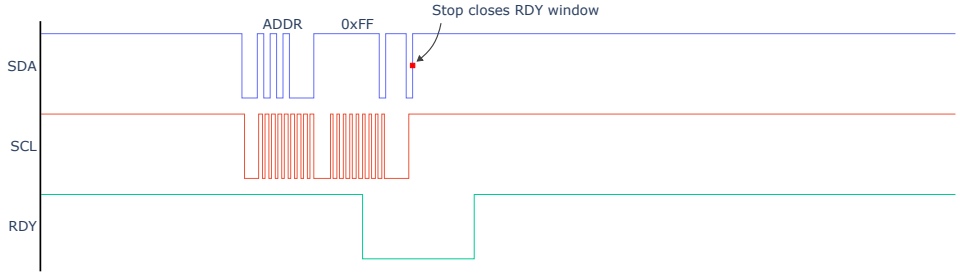


Figure B.1: Force Communication Closing a Communication Window

As a result, the MCU may observe the RDY pin change, and then attempt to communicate with the IC as soon as the force communication transaction is complete. This will cause the IQS7222A to respond with the error code 0xEE.

The following protocol can be used to minimise the likelihood of this error condition.

Step 1: Before sending the 0xFF command, read the state of the RDY pin and verify that it is high (the communication window is closed). If the RDY pin is already low, the communications window is open and can be handled as normal.
Step 2: If the RDY pin is high, issue the force communication I^2C command.
Step 3: As soon as the I^2C transmission of the force communication command has started, wait for the RDY window.
Step 4: Once the RDY is received, the MCU should wait at least 300 µs, then re-check the state of the RDY pin.
  (a) If the RDY pin is high, then the window was closed due to the STOP condition. Re-issue the 0xFF command, repeating the above procedure.
  (b) If the RDY pin is low, the communication window is still open, and normal I^2C operations may resume.

Figure B.2 shows an example of this process. The first force communication request occurred simultaneously with a RDY window, and the RDY window was closed due to the STOP condition. The MCU detected the RDY window, waited 300 µs, then checked the RDY pin state. The pin was HIGH, and the force communication request was repeated.

The second request opened the RDY window after some time, and the MCU waited 300 µs again before checking the RDY pin state. The RDY was low, and normal communication could continue.

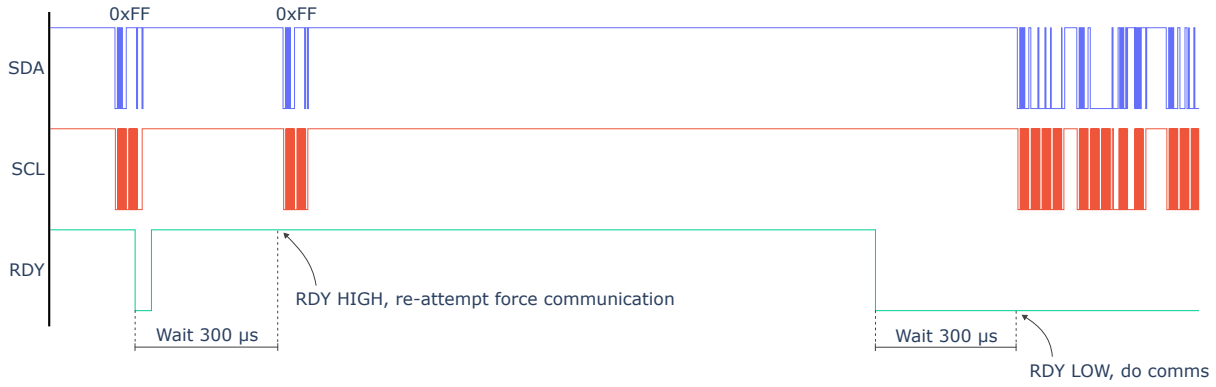


Figure B.2: Force Communication With RDY Check

B.5 Force Communication Request May Be Missed

There is a possibility of a force communication request being missed if the request occurs precisely when interrupts are disabled. To overcome this issue, a recommended workaround is to retry the communication after waiting for the t_{wait} period (described in Section 10.8.2). However, it is essential to retry at different timings that are not multiples of the report rate. This approach guarantees that the communication request will not be missed again by avoiding sending the request at the precise moment when interrupts are disabled. As an additional recovery mechanism, the IC can be reset using the MCLR pin and reinitialised if there is no response after a specified number of retries.

C Revision History

Release	Date	Changes
v0.3	April 2021	› Preliminary release
v1.0	September 2021	› Initial release
v1.1	March 2022	› Tape and Reel information added › Slider events added to Table A.3 › Hall boost gain bit definition corrected › Firmware version changed to v1.15 › Reference schematic updated › Bit definition for Read-write check corrected › Changed Communication protocol description › Read-write permissions added in memory map › Stop-bit disable bit definition corrected › Revision history added › I^2C section extended to include force communication and invalid communication request information › Register 0xDD added › VREGA electrical characteristics corrected › Bit and register names changed to follow user guide and GUI conventions › Example of h file from GUI and program flow diagram added › Schematic capacitor values corrected
v1.2	August 2022	› Add order code QFR and relevant documentation › All instances of projected capacitive sensing changed to mutual capacitive sensing
v1.3	September 2022	› Updated QFN lead dimensions
v1.4	March 2023	› Firmware version updated to v1.18 › Added order code 102 › Changes implemented for IQS7222A 102 IC option according to “PIN-230172” › Updated current consumption tables › Updated channel options section › Updated addressing information for order code 102 › Updated power mode and mode timeout section › Update Memory Map version information table › Memory Map reserved bits corrected
v1.5	February 2025	› Updated Force Communications section › Fixed product number in Section A.1

Release	Date	Changes
v1.6	May 2025	› Updated pin names › Added Section 6.1.1 describing Ultra-Low Power Mode › Added Section 8.1 regarding the Slider UI › Added more detailed descriptions of Slider configuration registers in Appendix A › Updated supply voltage values in Section 1.1 › Added more information in Known Issues Section › Style and formatting changes
v1.6.1	October 2025	› Added IQS722xy000QFR order code
v1.7	February 2026	› Overhauled ProxFusion Module section, expanding descriptions and including a list of all relevant settings › Re-ordered I^2C Interface section › Added recommended Conversion Frequency settings to Memory Map Descriptions › Added Program Flow Diagram › Updated Tape and Reel dimensions to include additional dimensions › Changed name of GPIO0 pin to OUTA to match GUI › Corrected CTx10 and CTx11 pins to "Not Connected" › Added Default Values to Memory Map Register › Added known issue regarding power mode changes after ATI › Added known issues regarding I^2C force communication
v1.8	August 2026	› Corrected ATI error conditions. › Added section regarding GPIO (OUTA) output. › Updated formatting and descriptions of memory map bitfields in Appendix A. › Expanded power mode descriptions.

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