IQS396 Datasheet

An Inductive/Capacitive ProxFusion® sensing device with an integrated haptics driver. The haptics LRA driver features internal H-bridge and H-bridge protection. Standalone operation offers efficient integration without the need for a master device. An optional I²C mode allows the configuration of multiple haptics settings including autoresonance.

1 Device Overview

The IQS396 is a ProxFusion® sensing device with an integrated haptics driver capable of driving Linear Resonant Actuator (LRA) motors. A ProxFusion channel event will trigger the haptic driver to allow effective feedback to the user. Standalone operation allows basic configuration via external strap options. The device also offers an I²C mode featuring configurable composite waveforms. The I²C mode features a closed-loop autoresonance algorithm. The autoresonance algorithm matches the resonant frequency of the driven motor in real time. Power consumption is optimised by automatic power mode management and an ultra-low power mode.

1.1 Main Features

- Standalone Mode
  - Sensor event triggers haptic feedback
  - Strap options allow for:
    - Sensitivity adjustment
    - Report rate adjustment
  - Digital output (active low, push-pull)
- I²C Mode
  - I²C interface - Up to Fast Mode Plus (1 MHz)
  - Strap option for I²Caddress selection
  - Convert to a standalone mode after power-on configuration
  - Fire-and-forget interface
  - Trigger haptic via sensor event or I²C command
  - Real-time closed loop autoresonance
  - Internal H-bridge
  - Selectable LRA drive frequency
- Internal H-bridge protections
- Ultra low power mode
- Automatic power mode management
- Design simplicity
  - PC software for configuration and debugging
- Supply Voltage: 1.71 V to 3.6 V
- QFN20 Package (3 × 3 × 0.55 mm) - 0.4 mm pitch

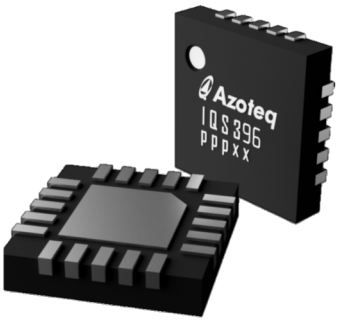

Figure 1.1: IQS396 QFN20 Package

1.2 Applications

- User interface touch buttons
- Doorbells and keypads

1.3 Block Diagram

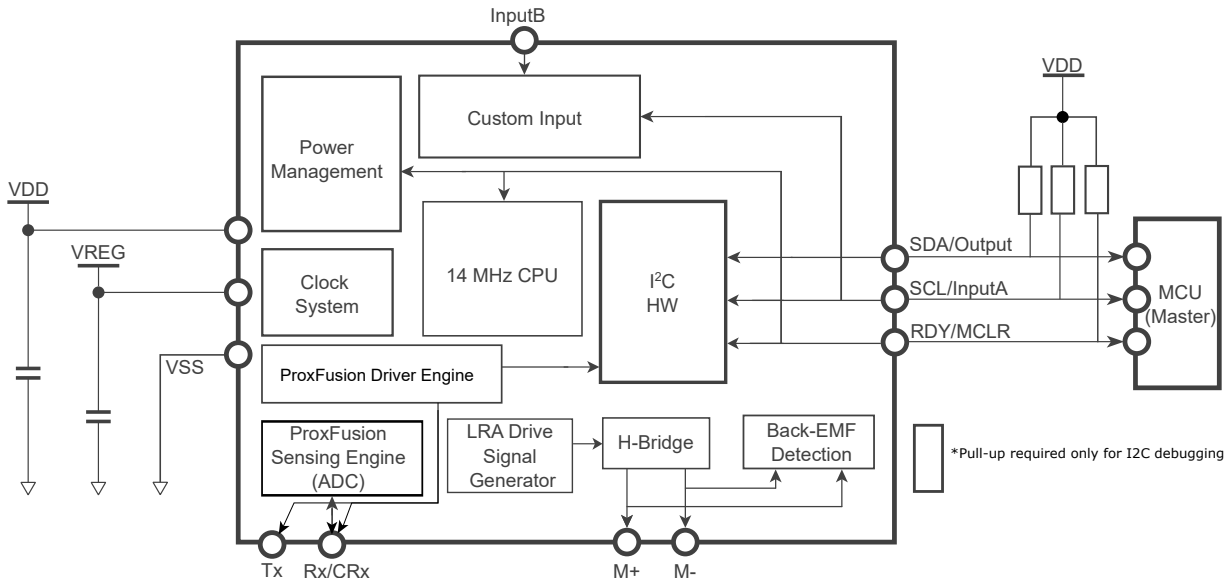

Figure 1.2: IQS396 Block Diagram

2 Usage Disclaimer

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2.1 Order Code Description

2.1.1 IQS396-0xx

The IQS396-0xx is a single channel I^2C application with an integrated haptics driver capable of driving Linear Resonant Actuator (LRA) motors. The IQS396-0xx can be switched to a standalone operating mode.

Applications of the IQS396-0xx order codes include general-use inductive buttons and Doorbells (touch and release detection).

2.1.2 IQS396-1xx

The IQS396-1xx is a single channel standalone inductive button application with an integrated haptics driver capable of driving Linear Resonant Actuator (LRA) motors. The IQS396-1xx can be switched to the I^2C operating mode for debugging.

Applications of the IQS396-1xx order codes include general-use inductive buttons and Doorbells (touch and release detection).

2.1.3 IQS396-2xx

The IQS396-2xx is a single channel standalone capacitive button application with an integrated noise filtering algorithm. The IQS396-2xx can be switched to the I^2C operating mode for debugging.

Applications of the IQS396-2xx order codes include user interface touch buttons and keypads.

Contents

3 Hardware Connections

3.1 QFN20 Pinout

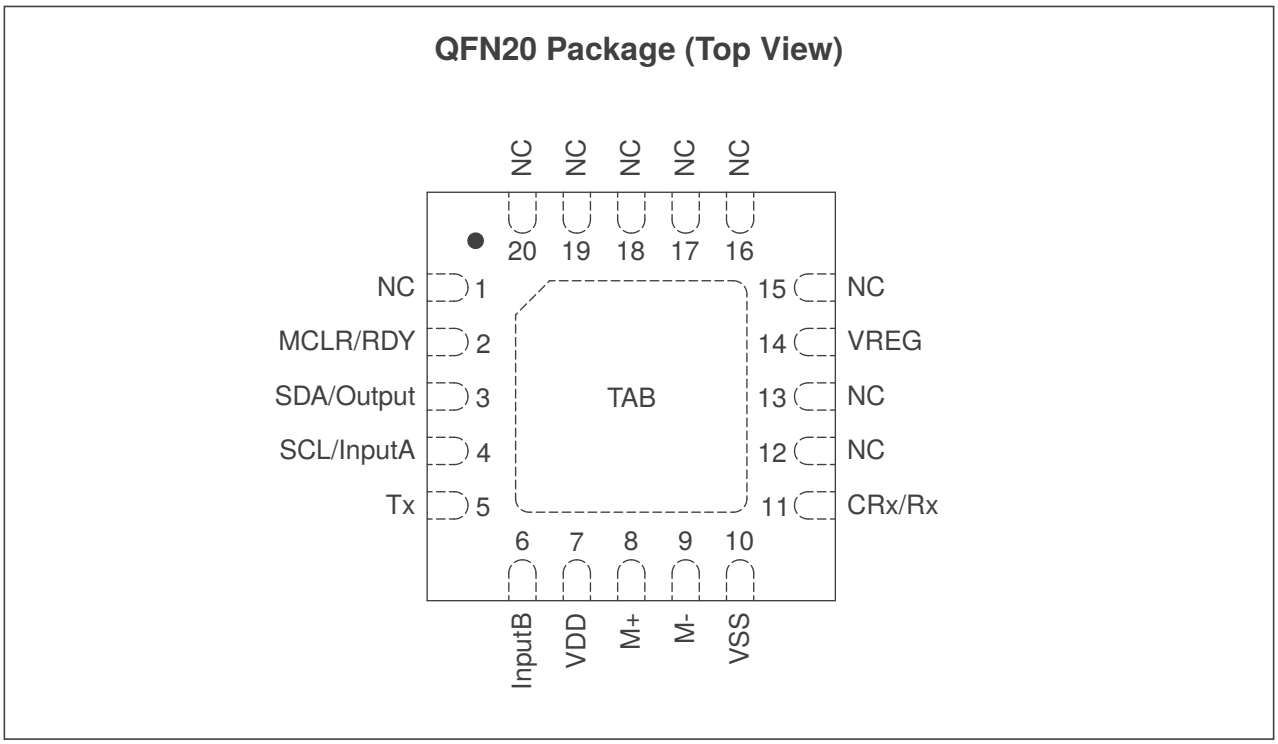


Figure 3.1: QFN20 Pinout

Table 3.1: QFN20 Pin Descriptions

Pin	Name	Type[i]	Function	Description
2	MCLR/RDY	I/O	GPIO	I^2C interrupt request / standalone MCLR functionality
3	SDA/Output	I/O	I^2C	I^2C data / standalone output
4	SCL/InputA	I/O	I^2C	I^2C clock / standalone InputA (sensitivity selection)
5	Tx	O	ProxFusion®	ProxFusion® inductive Tx pad
6	InputB	O		Report rate / I^2C address selection
7	VDD	P	Power	Power supply input voltage
8	M+	O	H-Bridge	Haptics H-Bridge
9	M-	O	H-Bridge	Haptics H-Bridge
10	VSS	P	Power	Analog/digital ground
11	CRx/Rx	I/O	ProxFusion®	ProxFusion® sensing pad
14	VREG	P	Power	Internally-regulated supply voltage
*	NC	-	-	Not connected
	TAB	-	-	Thermal pad (floating). It is recommended to connect this to VSS.

[i] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

3.2 Reference Schematic

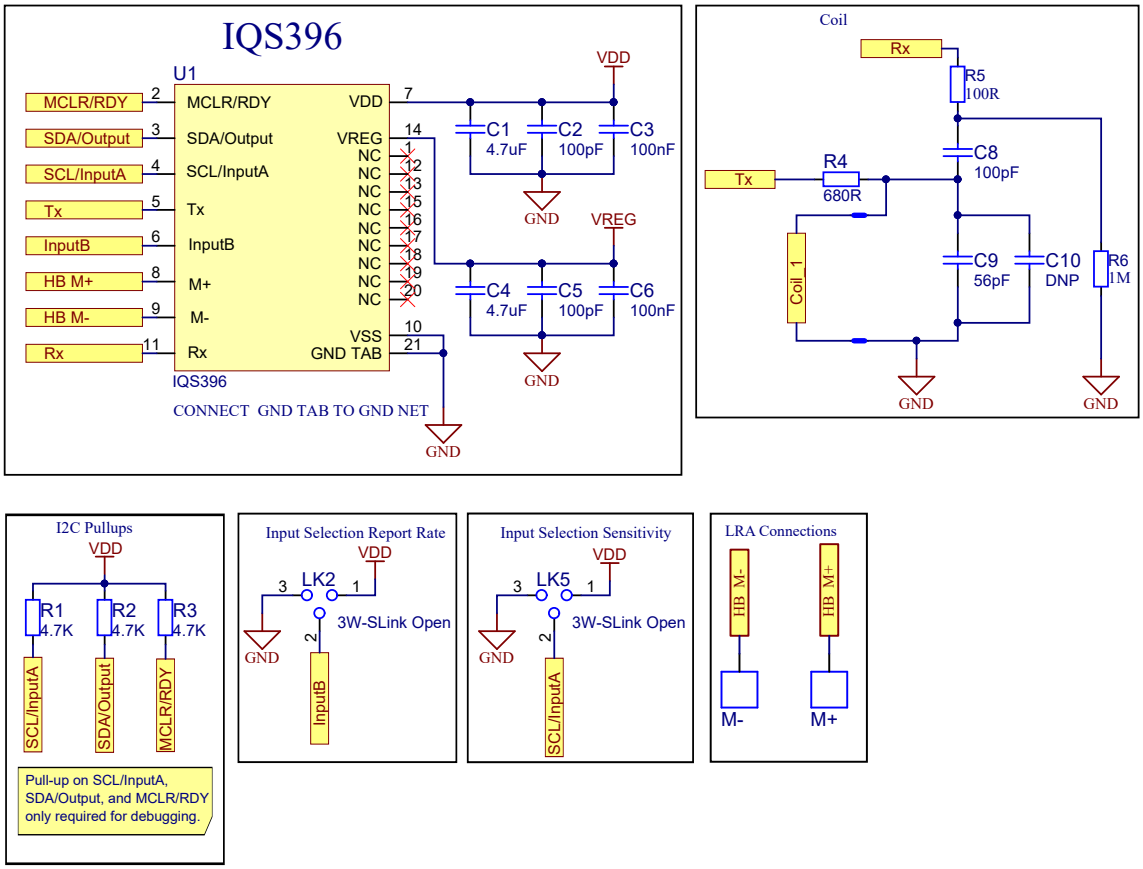


Figure 3.2: QFN20 Inductive Reference Schematic

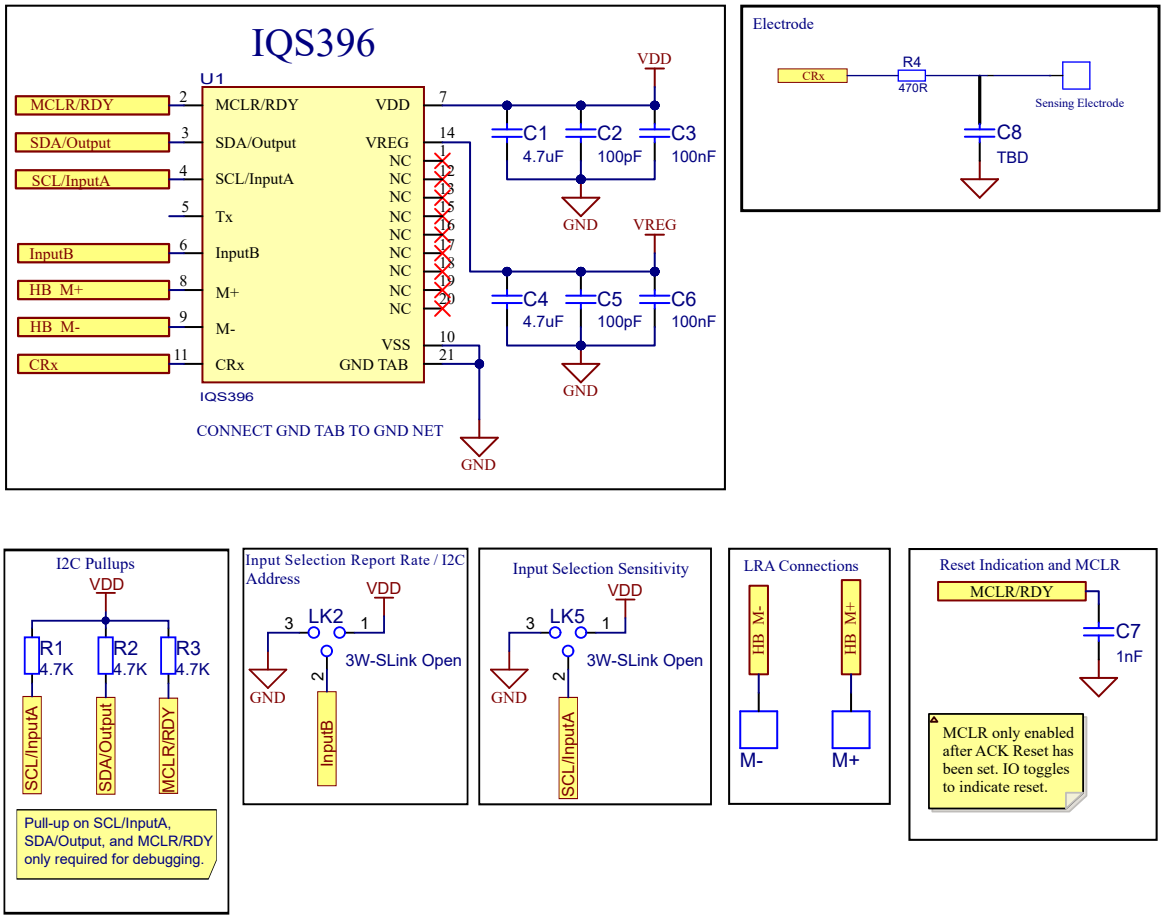


Figure 3.3: QFN20 Self-Capacitive Reference Schematic

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 4.1: Absolute Maximum Ratings

Symbol	Rating	Min	Max	Unit
V_{DD}	Voltage applied at VDD pin (referenced to VSS)	−0.3	3.6	V
V_{IN}	Voltage applied to any ProxFusion® pin (referenced to VSS)	−0.3	V_{REG}	V
	Voltage applied to any other pin (referenced to VSS)	−0.3	V_{DD} + 0.3 (3.6 V max)	V
T_{stg}	Storage temperature	−40	85	°C

4.2 General Operating Conditions

Table 4.2: General Operating Conditions

Symbol	Parameter	Typ	Unit
f_{OSC}	Master clock frequency	14	MHz
f_{PROX}	ProxFusion® engine clock frequency	14	MHz
V_{REG}	Internally-regulated supply output	1.53	V

4.3 Recommended Operating Conditions

Table 4.3: Recommended Operating Conditions

Symbol	Parameter	Min	Recommended	Max	Unit
V_{DD}	Standard operating voltage, applied at VDD pin	1.71		3.6	V
T_A	Operating free-air temperature	−20		85	°C
C_{VDD}	Recommended capacitor at VDD	C_{VREG}	$2 \times C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG (ESR $\leq$ 200 mΩ)	2.2[i]	4.7	10	µF

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to AZD004 for more information regarding capacitor derating.

4.4 ProxFusion® Electrical Characteristics

Table 4.4: Recommended Operating Conditions for ProxFusion® Pins

Symbol	Parameter	Min	Max	Unit
$Cx_{SELF–VSS}$	Capacitance between ground and external electrodes, in self-capacitance mode	1	400[i]	pF
$R_{Cx(SELF)}$	Series in-line resistance of self-capacitance electrodes	0	1[ii]	kΩ

[i] R_{Cx} = 0 Ω
[ii] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = 1/(10 \times f_{xfer})$, where C is the pin capacitance to VSS.

4.5 ESD Rating

Table 4.5: ESD Rating

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge voltage	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[i]	±4000	V

[i] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

4.6 Reset Levels

Table 4.6: Reset Levels

Parameter		Min	Max	Unit
V_{DD}	Power-up (Reset trigger) – slope > 100 V/s	1.65		V
	Power-down (Reset trigger) – slope < –100 V/s		0.9	

4.7 MCLR Pin Levels and Characteristics

Table 4.7: MCLR Pin Characteristics

Parameter		Min	Typ	Max	Unit
V_{IL}	MCLR input low level voltage	V_{SS} – 0.3		0.25 × V_{DD}	V
V_{IH}	MCLR input high level voltage	0.75 × V_{DD}		V_{DD} + 0.3	V
R_{PU}	MCLR pull-up equivalent resistor		210		kΩ
t_{Trig}	MCLR input pulse width – ensure trigger	250			ns

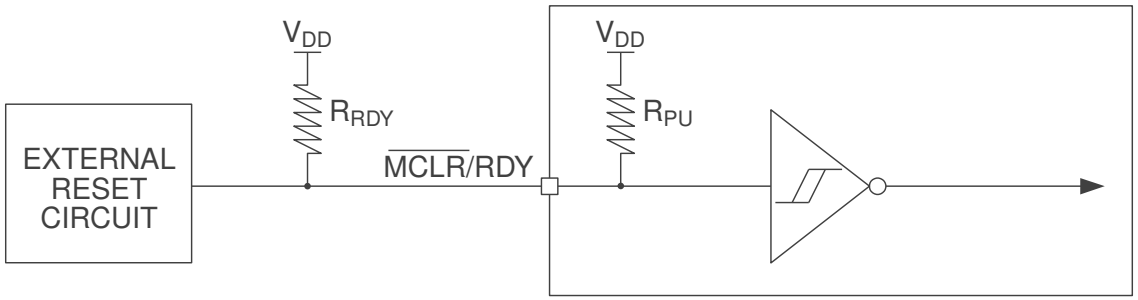


Figure 4.1: MCLR Pin Diagram

4.8 Digital I/O Characteristics

Table 4.8: Digital I/O Characteristics

Parameter		Test Conditions[i]	Min	Max	Unit
V_{OL}	Output low voltage of SDA and SCL pins	I_{OL} = 20 mA $V_{DD} > 2$ V		0.4	V
		I_{OL} = 20 mA $V_{DD} \leq 2$ V		0.2 V_{DD}	
	Output low voltage of SDA and SCL pins in GPIO output mode	I_{OL} = 10 mA		0.1 V_{DD}	
	Output low voltage of MCLR/RDY	I_{OL} = 5 mA			
	Output low voltage of any other GPIO pin	I_{OL} = 10 mA			
V_{OH}	Output high voltage	I_{OH} = −5 mA	0.9 V_{DD}		V
V_{IL}	Input low voltage		V_{SS} − 0.3	0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}	V_{DD} + 0.3	V
C_b	SDA and SCL bus capacitance			550	pF

[i] Standard operating conditions:
V_{DD}: 1.8 V to 3.6 V, unless otherwise stated.
Operating temperature: −20 °C to 80 °C.

4.9 I²C Characteristics

Table 4.9: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Set-up time for a repeated START condition	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data set-up time	50		ns
$t_{SU,STO}$	Set-up time for STOP condition	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

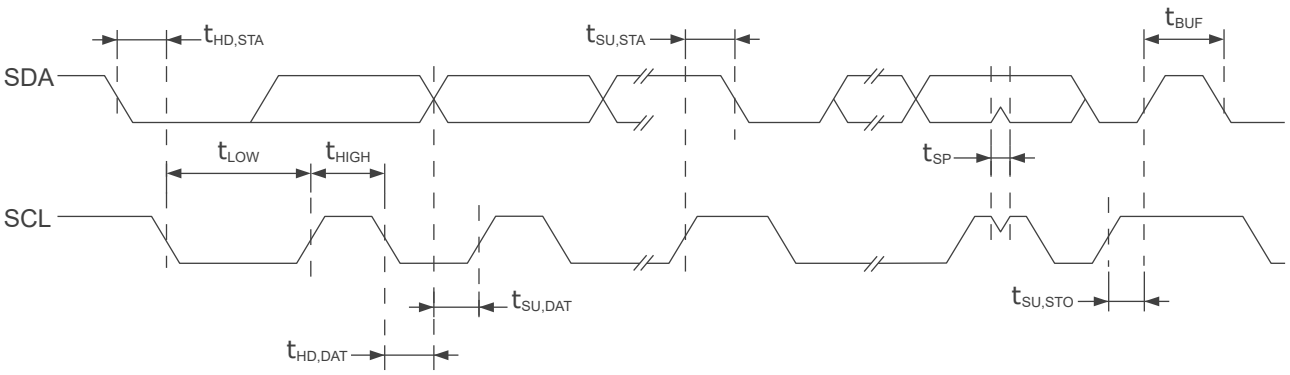


Figure 4.2: I²C Timing Diagram

4.10 H-Bridge Specifications

Table 4.10: H-Bridge Specifications

Symbol	Parameter	Min	Nominal	Max	Unit
R_L	Load resistance at V_{DD} = 3.3 V		18		Ω
I_L	Average DC load current		150	200	mA
f_{LRA}	LRA drive frequency	100		300	Hz

4.11 Current Consumption

The current consumption of the IQS396 is highly dependent on the specific parameters configured during initialisation, as well as on the frequency and duration of I²C communications. Therefore, the following tables serve as an illustration of the expected power consumption for similar configurations[i]. All measurements are taken with either *Event Mode* or *Standalone Mode* enabled, without any sensor

[i] These measurements are based on bench testing and have not been characterised over large volumes.

activations, and without any I²C communications. Momentary higher current consumption may be expected during activated states. The setup for the current measurement is shown in Table 4.11 and all other settings, unless stated otherwise, are kept default.

Table 4.11: IQS396 Inductive and Self-capacitive Current Measurement Setup

Parameters	Inductive	Self-capacitive
Number of Channels	Single I²C / Standalone channel	
ATI Target	4000	5000
ATI Base	4000	10000
HFosc	14 MHz	
Tx at HFosc	Enabled	Disabled
Invert Logic	Enabled	Disabled
Charge transfer frequency	1.75MHz	875kHz
Interface Selection	Event Mode / Standalone	

Table 4.12: IQS396 Inductive (I²C Event Mode)

Configuration	Sampling period [ms]	Sensing Mode	Typical Current [µA] 3.3V	
			NP	ULP
InputB to VSS	200	Inductive	8	4
InputB to VDD	43		26	6

Table 4.13: IQS396 Inductive (Standalone Mode)

Configuration	Sampling period [ms]	Sensing Mode	Typical Current [µA] 3.3V	
			NP	ULP
InputB to VSS	200	Inductive	8	4
InputB to VDD	43		26	6

Table 4.14: IQS396 Self-Capacitive (I²C Event Mode)

Configuration	Sampling period [ms]	Sensing Mode	Typical Current [µA] 3.3V	
			NP	ULP
InputB to VSS	200	Self-capacitive	13	4
InputB to VDD	43		45	12

Table 4.15: IQS396 Self-Capacitive (Standalone Mode)

Configuration	Sampling period [ms]	Sensing Mode	Typical Current [µA] 3.3V	
			NP	ULP
InputB to VSS	200	Self-capacitive	12	4
InputB to VDD	43		43	11

5 LRA Drive Theory

A Linear Resonant Actuator (LRA) is a spring mass system. The mass is magnetic. A driving coil creates a magnetic field to exert force on the magnetic mass.

The coil must be driven with an Alternating Current (AC) voltage to create the magnetic field. When the frequency of this AC voltage matches the resonant frequency of the spring mass system, the maximum vibration force is exerted.

In the ideal case, the AC voltage is a pure sinusoid. The IQS396 approximates a pure sinusoid drive with a Pulse Width Modulated (PWM) drive signal. When the duty cycle of the PWM drive is varied sinusoidally, the average drive voltage follows a pure sinusoid.

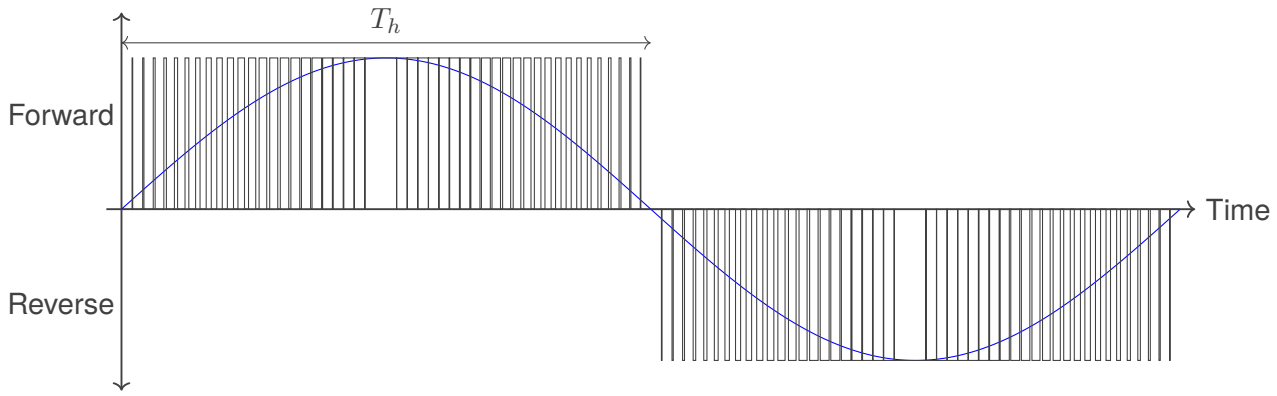


Figure 5.1: PWM Drive Approximation

Figure 5.1 shows the PWM output drive in relation to the ideal sinusoid drive. T_h is the width of a single half cycle. For a 200 Hz motor, this would be $\frac{1}{2\times200} = 2.5\,\mathrm{ms}$. The motor is driven in the forward direction for one half cycle and then in the reverse direction for one half cycle. This is repeated for the duration of the haptic pulse. The strength of vibration depends on the amplitude of the average sinusoidal drive. Since the amplitude of the average drive signal is directly related to the maximum duty cycle of the PWM drive, the vibration strength can be varied by changing the maximum duty cycle of the PWM drive signal.

It is difficult to vary the duty cycle of the PWM according to a pure sinusoid. For this reason, the IQS396 applies a further approximation to the PWM drive signal. Each half cycle of the sinusoidal modulation is approximated as three linearly interpolated segments. The first segment is linearly increasing, the second constant, and the third linearly decreasing. The IQS396 provides fine control over these segments. A detailed description of the configuration of these segments is given in Section 9.

6 Autoresonance

6.1 Operation

The autoresonance algorithm matches the drive frequency to the resonant frequency of the driven LRA. The driver operates by monitoring the back-EMF of the motor at the end of every half cycle. By detecting the zero-cross of the back-EMF, the driver is able to track changes in the resonant frequency of the LRA. This provides consistent vibration strength in changing conditions and across production variations. It is recommended to set the initial frequency slightly higher than the expected resonant frequency.

Autoresonance is enabled per pattern. For a complete understanding of how to enable it, see Section 9.1.

6.2 Backoff

Once a frequency lock has been achieved, it is crucial that the zero-cross occurs. If the zero-cross does not occur, the driver has no information about the back-EMF and cannot make an intelligent decision about the next half cycle's drive frequency. A zero-cross may not occur when the drive frequency is far from the resonant frequency of the motor. If the drive frequency is much lower than the resonant frequency, it can take many cycles to acquire a lock. If the drive frequency is much higher than the resonant frequency, an accurate lock may never be achieved.

When a zero-cross does not occur, the driver assumes that the drive frequency is too low. The driver increases the drive frequency by a fixed percentage. This is an attempt to re-establish a frequency lock. In most cases, a zero-cross will be seen within the next few half cycles, and the frequency lock will be restored.

This effect can be mitigated by slightly increasing the drive frequency such that it is more than the exact resonant frequency as measured by the zero cross. Unless conditions change significantly, this guarantees that a zero-cross will occur on the next half cycle.

The drive frequency should be increased by as little as possible to ensure it matches the resonant frequency. The exact amount depends on the motor being driven. To this end, the *Autoresonance Backoff* setting is included in the memory map.

When a zero-cross is detected, the drive frequency will be set to the resonant frequency of the motor and then increased by a percentage equal to one hundred divided by the value in the *Autoresonance Backoff* register.

$$\text{Percentage Increase} = \frac{100}{\text{Autoresonance Backoff}}$$

Setting *Autoresonance Backoff* to '0' will match the zero-cross frequency exactly.

In Figure 6.1, the current half-cycle drive is shown in red. Provided $T_{h(n)}$ is close to but less than the resonant half-cycle period, the back-EMF of the motor will lag the drive voltage. The driver detects the zero cross of the back-EMF and uses this to determine T_z. The frequency of the next half cycle is then increased from T_z in accordance with the *Autoresonance Backoff* setting to determine $T_{h(n+1)}$. This is the period of the next half cycle. Note that Figure 6.1 shows the average voltage for the driven half cycles and the instantaneous voltage for the back-EMF.

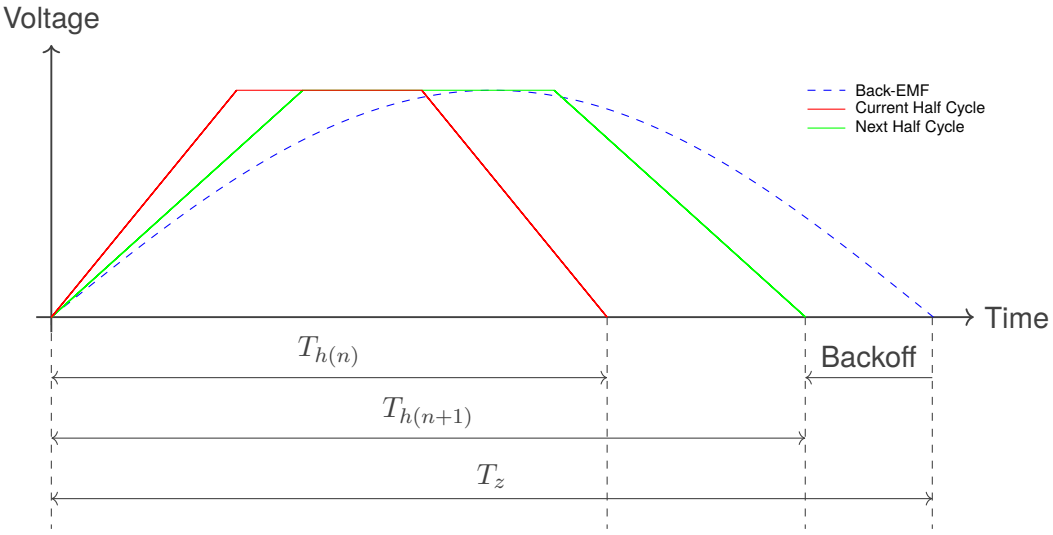


Figure 6.1: Autoresonance Backoff

6.3 Recommend Recalibrate

If the frequency at the start of a waveform differs by more than 25% from the frequency at the end of the waveform, the *Recommend Recalibrate* bit in register 0x1003 will be set. Typically, this will occur for one of three situations:

1. This is the first haptic pulse, and the starting frequency was far from the resonant frequency.
2. External conditions have changed significantly.
3. An error has occurred with the autoresonance algorithm.

The *Recommend Recalibrate* bit is cleared when the master adjust the LRA frequency by writing to the *LRA Frequency* register over I^2C.

For item 1, the master can simply read the *LRA Frequency* register and write the same value back. This is most likely to occur during a calibration sequence, where the master initiates several autoresonance-enabled waveforms to find the motor frequency. The calibration sequence is successful when the *Recommend Recalibrate* bit is not set for several consecutive trigger haptic commands.

Items 2 and 3 are error conditions. If the *Recommend Recalibrate* bit is set outside of a calibration sequence, it indicates that either item 1 or item 2 has occurred. The calibration sequence should be done again.

7 H-Bridge

7.1 Settings

7.1.1 Slew Rate

The internal H-bridge has a slew rate-limiting function. This limits the slew rate of the PWM drive. Limiting the slew rate can help to reduce electromagnetic interference caused by the fast switching H-bridge drive signals.

The *Slew Rate Control* bit in the *H-Bridge Setup* register enables the slew rate function. When enabled, the *Slew Rate* setting selects the slew rate limit.

7.1.2 Drive Strength

The internal H-bridge is comprised of several drive stages. The *Drive Strength* setting in the *H-Bridge Setup* register controls which of these stages are active. The higher the *Drive Strength*, the more stages are active. The values in Section 4.10 are specified for a drive strength of '5'.

A drive strength of at least '1' is required for the H-bridge to function. Generally, the *Drive Strength* should be set to '5'.

7.1.3 Ground Inactive

When the *Ground Inactive* bit in the *H-Bridge Setup* register is set, both M+ and M- will be pulled to ground when the motor is not being driven and the IQS396 is not in the ULP power state. In combination with inverted patterns, this can help to brake the motor and provide a crisper feel to the haptic pulse.

7.2 Protections

The internal H-bridge is equipped with several protection mechanisms. These are controlled by the H-bridge hardware. If enabled, they will automatically disable the H-bridge drive under the relevant error condition.

7.2.1 Over-Temperature Protection

Over-temperature protection is enabled by setting the *Over-Temperature Protection* bit in the *H-Bridge Setup* register. Over-temperature protection activates when the temperature of the device exceeds the temperature specified by the *Over-Temperature Threshold* in the *Over-Temperature Settings* register.

The *Hysteresis* bit enables one-way hysteresis for over-temperature detection. This ensures that the over-temperature protection activates cleanly when an over-temperature condition occurs. It is recommended to always have hysteresis enabled when using the over-temperature protection functionality.

7.2.2 Shoot-Through Protection

Shoot-through protection is enabled by setting the *Shoot-through Protection* bit in the *H-Bridge Setup* register. Shoot-through protection prevents direct shorting of VDD to GND when the H-bridge transistors are switching. It is recommended to always have shoot-through protection enabled.

8 Haptic Control and Monitoring

The IQS396 allows up to three unique waveforms to be stored in memory. The active waveform is chosen using the *Waveform Selection* field in the *Haptic Control* register.

8.1 Trigger Haptics Command

The currently configured waveform is played when a trigger haptics command is given. A trigger haptics command can be given through I^2C.

A trigger haptics command issued while haptics is active will be ignored.

Note: If the "Trigger haptics" command is issued while the device is in ULP mode, the haptic output will be queued and only execute when the device has finished its full sequence of ULP auto conversions at the instant of doing a "Normal power" loop again.

8.2 I^2C Control

In I^2C, a trigger haptics command is given by setting the *Trigger Haptics* bit in the *Haptic Control* register. The *Trigger Haptics* bit is cleared at the start of every waveform, regardless of how the waveform was triggered.

Since the *Waveform Selection* field and the *Trigger Haptics* bit are in the same register, only the address bytes plus a single data byte need to be written to both play and select a waveform.

The waveform can be stopped by disabling the *Enable Haptics* bit in the *Haptic Control* register immediately after the haptics event is reported. The waveform will be halted immediately. If the *Disable Haptics* bit is set when the haptics is already running, that is, waiting for a long period after the haptics event is reported, then it will have no effect and haptics will run until completion.

8.3 LRA Drive Frequency

The *LRA Frequency* register is used to set the frequency in Hertz (Hz) at which the duty cycle of the PWM output drive changes. It is also used to report the frequency measured by the autoresonance algorithm.

8.4 PWM Frequency

The *PWM Frequency* register sets the frequency in Hertz (Hz) of the output PWM drive. Internally, this has an effect on the time domain resolution with which the duty cycle of the drive updates.

It is recommended to always set the *PWM Frequency* register to ‘20000’.

9 Haptic Effect Configuration

The IQS396 defines the following concepts:

Segment	A PWM pulse with a duty cycle that is either increasing, decreasing or constant.
Pattern	A series of up to three consecutive segments.
LRA Drive Period	The time it takes for one full LRA drive cycle.
Half Cycle	A pattern lasting one half of an LRA drive period.
Stage	A pattern played for a number of half cycles, where the drive direction alternates every half cycle.
Haptic Pulse	Up to five stages, played sequentially.
Waveform	Any number of haptic pulses.
Repeat Count	The number of haptic pulses per waveform.
Repeat Time	The time between haptic pulses.

Figure 9.1 shows the basic components of a single drive cycle. The segments are denoted S_0, S_1, and S_2 and make up an approximately sinusoidal pattern. Each half cycle, denoted H_0 and H_1, consists of a single pattern. Every two-half cycles makes one LRA drive period. Every alternate half cycle is driven in the opposite direction to its predecessor.

Different haptic effects can be composed by creating combinations of these settings. For example, Figure 9.2 shows a two-stage waveform. The first stage consists of an approximately sinusoidal pattern lasting two half cycles. The second is a single half cycle driving a triangular pattern.

9.1 Pattern Definition

Each pattern can have up to three segments. A pattern is fully defined if the first N segments have valid settings when the *Segments* setting in a pattern's configuration registers is set to 'N'. Only the first N segments form part of the pattern. All other segments are ignored.

Each segment has a *Start Duty Cycle* and an *End Duty Cycle*. For every segment, the IQS396 will linearly interpolate the drive duty cycle from the *Start Duty Cycle* to the *End Duty Cycle*, and then progress to the next segment or half cycle.

The segment *Duration* parameter defines how long it will take to perform the interpolation. The *Duration* is specified as a percentage of the half cycle width, where 255 is 99%. For example, a register value of '85' will result in the segment lasting one third of every half cycle. For any given pattern, the values of all enabled segment *Duration* registers must sum to 255. For example, if two segments are used and the first segment's *Duration* register is '100', the second segment's *Duration* register must be set to '155'.

The *Invert* bit in a pattern's *Pattern Setup* register selects the drive direction for each half cycle. When the *Invert* bit is clear, even half cycles are driven in the forward direction and odd half cycles are driven in the reverse direction. Setting the *Invert* bit flips this behaviour. This allows braking patterns to be defined. The indexing begins at the start of the stages. In other words, the first half cycle of a stage is always considered even.

The *Autoresonance* bit in a pattern's *Pattern Setup* register enables autoresonance for the pattern. Any stage executing a pattern whose *Autoresonance* bit is set will perform autoresonance only for the duration of that stage. Pattern-specific autoresonance allows for easy configuration of braking and pseudo overdrive patterns. A full description of autoresonance is in Section 6.

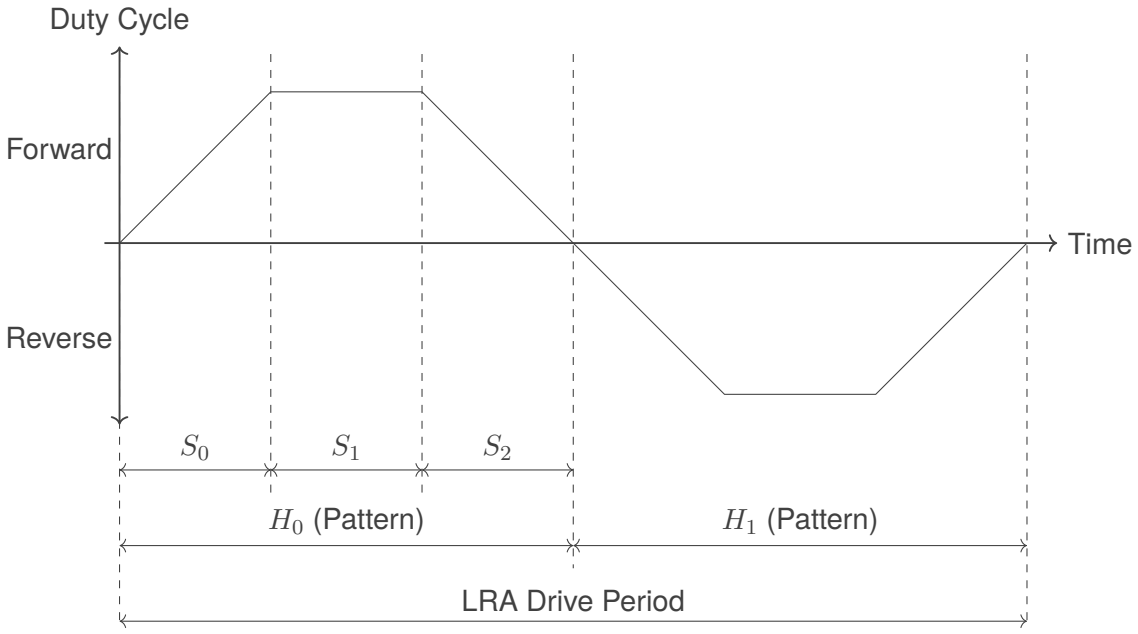


Figure 9.1: Anatomy of One Full Drive Cycle

9.2 Stages

Every waveform pulse consists of up to five stages. Patterns are packed into stages in a waveform's *Pattern Selection* register.

The 16-bit pattern select setting is laid out in groups of three-bit wide bitfields. Each bitfield corresponds to a stage. Since there are five stages, the most significant bit is ignored. If a pattern select bitfield is set to '0b000', no pattern is selected and the stage is disabled. Otherwise, it selects one of the seven definable patterns.

Every waveform has a block of five 8-bit wide half-cycle count settings. This array sets the number of half cycles to execute in each stage. Each half-cycle count corresponds to a stage. For example, the half cycle counts for waveform zero begin at memory map address 0x1102. The value loaded at address 0x1102 sets the number of half cycles for the first stage. The value loaded at address 0x1103 sets the number of half cycles for the second stage and so on.

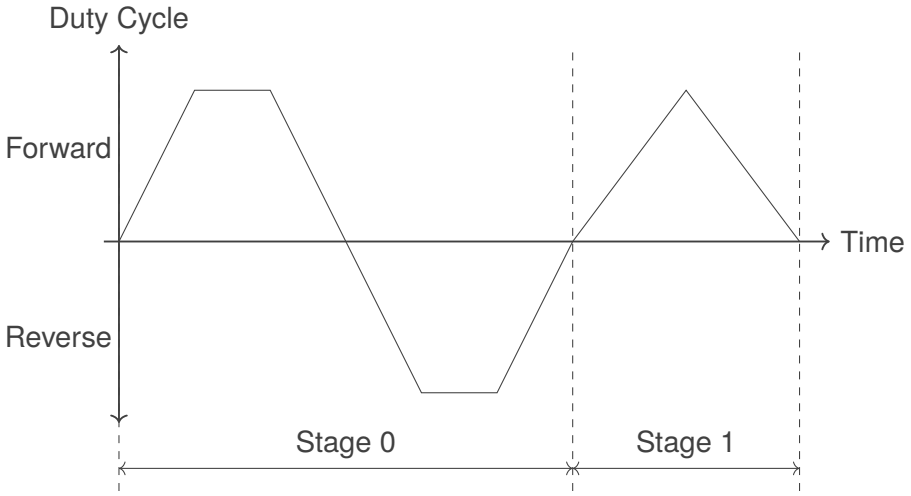


Figure 9.2: A Two Stage Waveform

10 ProxFusion® Channel

The IQS396 features a ProxFusion® sensing channel that uses Azoteq's patented on-chip ProxFusion® module to measure and process relative changes in either capacitive or inductive sensors.

10.1 Sensing Modes

The ProxFusion® channel supports one of the following sensing modes:

- Self-capacitive sensing
- Resonated inductive sensing

The sensing mode can be modified in the *ProxFusion Settings 1* registers.

Please refer to the following application notes for more information:

- AZD004: Overview of Azoteq's ProxFusion® Sensing
- AZD115: Design Guidelines for Inductive Sensing
- AZD125: Design Guidelines for Capacitive Touch Sensing

10.2 Counts

The ProxFusion® module reports a capacitance or inductance measurement as a relative, unit-less value referred to as "Raw Counts". These raw counts are related to the number of charge transfer cycles necessary to charge an internal sampling capacitor, and are typically inversely proportional to the signal measured on the external sensor.

10.2.1 Counts Linearisation

The IQS396 does not directly use the "Raw Counts" obtained from the sensing module, but uses "Linearised Counts", which is calculated as

$$\text{Linearised Counts} = \frac{3276750}{\text{Raw Counts}}. \tag{1}$$

All references to "Counts" in this datasheet, and in the I^2C memory map, use these Linearised Counts values.

After linearisation, counts are filtered using a low-pass IIR filter to reduce the high-frequency noise in the measurement. The response of the filter can be adjusted with the *Counts Filter Beta* value in the *Filter Betas* registers. Higher beta values result in a slower filter response, with less noise on the channel.

10.3 Button Event Detection

Button Events attempt to emulate the behaviour of a typical button, which stays in activation for a configurable period of time as it is pressed. A *Button Proximity Event* occurs when the configurable *Proximity Threshold* has been reached and this happens when a target comes into close proximity with the sensing electrode. A *Button Touch Event* occurs when the configurable *Touch Threshold* has been reached.

10.3.1 Long-Term Average

Button events are detected by comparing the filtered counts value to a reference value, known as the Long-Term Average (LTA). While the channel is not in activation, the LTA is slowly updated to track changes in the environment using a low-pass filter.

The difference between the filtered counts and the LTA is stored as the *Delta* value.

$$\text{Delta} = \text{LTA} - \text{Counts} \tag{2}$$

The delta is used to detect user interaction by comparing it to the *Touch Threshold*. The channel enters the active state when the delta exceeds the threshold, and the *Touch Active* bit in the *Button Events* register will be set.

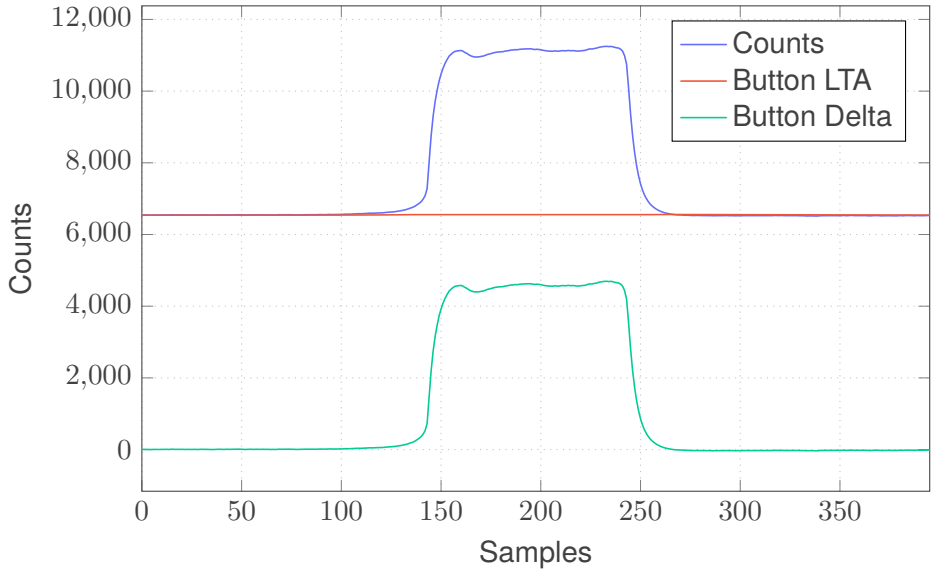


Figure 10.1: Button UI Activation

The LTA is then halted (kept constant) while the Button event is active, or while the delta exceeds the *LTA Halt Threshold*, as shown in Figure 10.1. The LTA Halt Threshold can typically be made smaller than the Button Threshold. This may help increase the sensitivity of the event detection during slower activations, preventing the LTA from drifting during user interaction.

The response of the LTA filter is controlled by the various *LTA Beta* values. The *LTA Beta* value sets the response of the filter during High-Accuracy and Normal power modes, whereas the *Low Power LTA Beta* is used during Low and Ultra-Low power modes. The Low Power Beta value should be set to a *larger* value than the Normal Beta value, to maintain adequate sensitivity at lower sampling rates.

10.3.2 Direction

Negative delta values are typically ignored, as they typically indicate an unexpected decrease in signal. If a negative delta value exceeds the *Fast LTA Bound* threshold, the LTA will be updated using the *Fast LTA Beta* filter. This behaviour can be disabled by setting the *Bi-Directional* bit, or the sign of the delta can be inverted by setting the *Inverse* bit in the *ProxFusion Settings 0* register.

10.3.3 LTA Reseeding

The reseed function of the device will replace the filtered counts and the long-term average value of the channel with the latest sampled counts value to reset the environmental reference of the channel. This may be necessary in certain instances when the Button event gets incorrectly stuck in an activation. Detection of stuck states is controlled by the *Touch Timeout* and *Proximity Timeout* parameters. If any of the Button events remain active for the timeout duration, the LTA is reseeded automatically. This behaviour can be disabled by setting the timeout parameter to 0.

A *Reseed* command can also be given manually by setting the corresponding bit in *System Commands*.

10.4 Automatic Tuning Implementation

The ATI is a sophisticated technology implemented in ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode designs, without modification to external components.

The ATI functions by using the *Base* and *Target* parameters to calculate appropriate *Divider* and *Compensation* values to achieve an LTA approximately equal to the ATI target value. Note that the base and target values are specified in terms of Linearised Counts, and the base value should always be larger than the target. Typical base and target values for inductive and capacitive sensing modes are shown in Table 10.1.

Table 10.1: Base and Target Range

Sensing Mode	Base		Target	
	Min	Max	Min	Max
Inductive Sensing	3500	8000	3500	8000
Capacitive Sensing	10000	30000	4500	10000

The sensitivity of the touch channel can be adjusted by configuring the *ATI Base* and *ATI Target* registers. The ATI parameters' relationship to sensitivity is generally described as:

$$\text{Sensitivity} \propto \frac{\text{ATI Base}}{\text{ATI Target}}.$$

To increase the sensitivity of the touch sensor, the Target value can be decreased. To reduce the sensitivity, the Base value can be decreased.

If the ATI algorithm cannot achieve a counts value within the ATI Band, the IQS396 will set the channel's ATI Error flag.

The Coarse Gain parameter in the *ProxFusion Dividers* register can be tuned in the GUI. The ATI will then adjust the Fine Divider parameter until the counts reach the base value. The Coarse Gain should be manually adjusted at design time until the Fine Divider reaches a value between '4' and '14' after ATI. It can then be fixed across production.

10.4.1 Automatic Re-ATI

One of the most important features of the automatic Re-ATI functionality of the IQS396 is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. It is always recommended to have the automatic Re-ATI functionality enabled. When a Re-ATI is performed on the IQS396, the *ATI Event* status bit will be set momentarily to indicate that this has occurred.

An automatic Re-ATI operation is performed when the reference of a channel drifts outside the acceptable range around the ATI Target, which is defined by the *ATI Band* parameter. Automatic Re-ATI is also triggered on ATI Error states.

10.5 Debouncing and Hysteresis

Each of the Button event provides two mechanisms to prevent jitter: debouncing and hysteresis.

Debouncing occurs when the Button delta initially crosses the threshold. It forces the IQS396 to perform a number of quick measurements (at Normal Power report rate), checking that all measurements exceed the threshold. The event's *Debouncing* flag is set as long as debouncing is active. Once debouncing is complete, the event's *Active* flag is set.

The number of high-frequency measurements to execute can be configured independently for entering or exiting the event's active state in the *Debounce* register. Setting the debounce values to '0' or '1' will disable debouncing.

Hysteresis allows the channel to use different enter and exit thresholds for an event. Once the event has entered the active state by exceeding the normal threshold value, the exit threshold is calculated as

$$\text{Exit Threshold} = \text{Threshold} \times \left(1 - \frac{\text{Hysteresis Value}}{256}\right) \tag{3}$$

For example, with a Button threshold of 100 counts, and a hysteresis value of 50, the Button event will enter the Active state when the delta exceeds 100 counts, and will exit the Active state when the delta drops down to $100 \times (1 - 50/256) = 80$ counts.

10.6 Power Mode Timeout

In order to optimise the power consumption and the performance, the power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time, known as the "power mode timeout".

10.7 Sensor Setup

10.7.1 Channel Setup

The channel sensitivity and report rate can be adjusted using two input pins on the IQS396. For more information see Section 11.1.

10.7.2 Channel Default Settings

The default settings for the channel sensitivity, report rate, proximity and touch event timeout are shown below.

Table 10.2: Default Channel Settings

Order Codes	Prox Timeout [s]	Touch Timeout [s]	Sampling Period [ms]		Sensitivity	
			Slow	Fast	Low	High
IQS396-0xx IQS396-1xx	20	20	200	43	Base: 5000 Target: 5000	Base: 4000 Target: 4000
IQS396-2xx					Base: 10000 Target: 6000	Base: 10000 Target: 5000

10.7.3 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) is set to a default of 14 MHz for the IQS396-0xx and IQS396-1xx order codes, and 875 kHz for the IQS396-2xx order code unless otherwise indicated. F_{OSC} can be used as the Tx frequency by setting the *F_{OSC} Tx Frequency* bit in the *Sensor Setup* register.

10.8 Watchdog Timer

The IQS396 implements a hardware watchdog timer. The watchdog timer is set to expire after the default 1023 ms if not reset and it will trigger a software reset upon expiration. The watchdog timer period is configurable in the *ULP And Watchdog Settings* register.

During I^2C communication the watchdog timer will reset whenever a read or write occurs. If the master initiates communication by sending an I^2C START condition and does not complete the I^2C transaction within 1023 ms, the IQS396 device will reset.

The I^2C transaction is completed either when an I^2C STOP notification is sent by the master or when the master ends the communication as described in Section 12.9.

10.9 Hardware Reset

The MCLR pin (active low) can be used to hard reset the device. For more details see Section 4.7.

11 Basic Standalone Functionality

11.1 Input Pin Functionality

The IQS396 offers two input pins that can be used to adjust the sensitivity and report rate. Table 11.1 shows the different input pin configurations.

Table 11.1: IQS396 input pin description

Input pin[i]	VDD[ii]	VSS[iii]
InputA	High sensitivity	Low sensitivity
InputB[iv]	High report rate / I^2C Address 0x48	Low report rate / I^2C Address 0x56

Note: In standalone mode, debugging is not possible when InputA is shorted to VSS. Both InputA and Output must have pull-up resistors connected.

11.2 Output Pin Functionality

The Output pin is used to indicate when a touch event has occurred. This pin is configured as a push-pull active low pin and is set to VSS when a touch enter / touch release is detected. When a touch enter is detected, the Output pin is set to VSS for a configurable period (t_{out}), which is dependent on the report rate. After the time period t_{out}, the pin is set to VDD and will remain set to VDD while the touch state is active. When a touch release is detected, the pin is set to VSS again for a duration of t_{out}.

In summary, t_{out} can be set to either 43ms (high report rate) or 200ms (low report rate). A touch event will trigger two pulses on the Output pin, one pulse for the touch enter event and another pulse for the touch release event. Haptics is also triggered whenever a touch enter and touch release event occur.

The period (t_{out}), can be longer than the report rate period if Haptics pattern to output is longer than the report rate period (e.g. fast sampling and more half cycles to execute). The two output pulses can be joined when the report rate period is longer than the touch persistence (e.g. touched and released within the report rate period). The IQS396 power-on state description is shown in Table 11.2.

Table 11.2: IQS396 power-on state description

IC sensing option	POR state of the Output pin	Output pin state description
Inductive	High	Not in touch
Self-capacitive	High	Not in touch

11.3 Standalone Power On Sequence of the IQS396

On startup, the output of the IQS396 will follow the sequence shown in Figures 11.1 and 11.2. As shown in the figures below, the time interval t_{start_up}, is typically less than 500 ms and the time interval for checking the states of the input pins is typically less than 12 ms. After power-on-reset (POR), the input pin states are checked and the necessary settings are selected based on the strap options

[i] InputA and InputB must not be left floating.
[ii] Pins are shorted to VDD.
[iii] Pins are shorted to VSS.
[iv] Only the IQS396-002 order code allows InputB to be used for I^2C address selection.

shown in Table 11.1. The I²C debug window is then made available with the ability to transition the device interface from standalone to I²C mode.

Note: If no interface transition occur then the device proceed into a complete standalone mode where the input pins are no longer read and no system settings can be changed. A POR is required in order to correctly configure the device whenever the state of any input pin has changed and/or whenever the system settings must be adjusted through the I²C debug window.

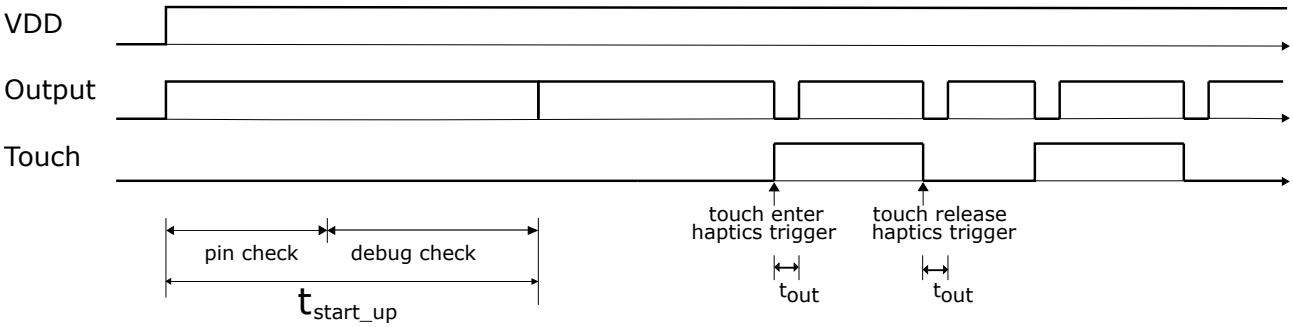


Figure 11.1: IQS396 output timing diagram (no touch at POR)

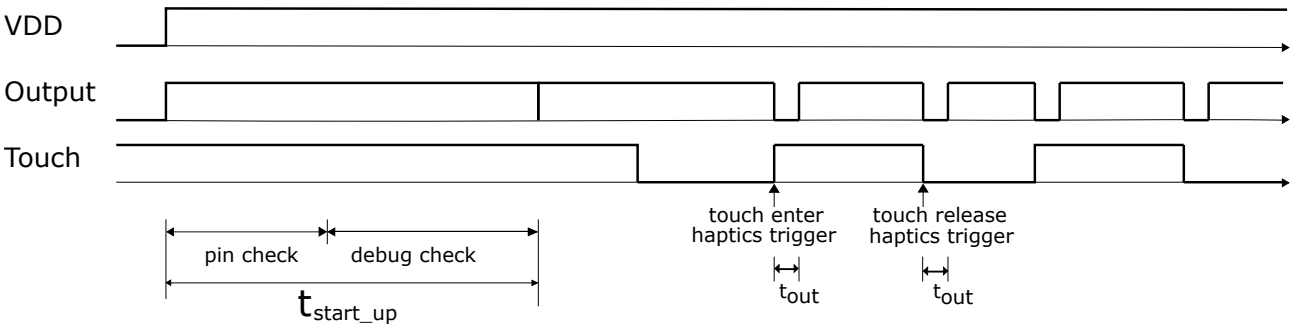


Figure 11.2: IQS396 output timing diagram (touch at POR)

12 I²C Interface

12.1 I²C Module Specification

The device features a standard two-wire I²C interface, complemented by a RDY (ready interrupt) line, supporting a maximum bit rate of up to 1 Mbit/s. The memory structures accessible over the I²C interface are byte-addressable with 16-bit address values. 16-bit or 32-bit values are packed with little-endian byte order and are stored in word-aligned addresses.

- Standard two-wire interface with RDY interrupt line
- *Fast-Mode Plus* I²C with up to 1 Mbit/s bit rate
- 7-bit device address
- 16-bit little-endian register addressing
- One data byte stored per register address

12.2 I²C Address

The IQS396 has a supports two I²C addresses, that is, 0x48 (0b1001000) and 0x56 (0b1010110).

The full address byte of address 0x48 is 0x90 (write) or 0x91 (read), and the full address byte of 0x56 is 0xAC (write) or 0xAD (read).

12.2.1 Reserved I²C Address

When communicating with the IQS396, it will acknowledge (ACK) communication attempts made to an additional address derived from its slave address. This derived address is obtained by flipping the least significant bit of the slave address.

For example, with the default slave address of 0x56, the derived address would be 0x57 (0b1010111), obtained by changing the LSB from ‘0’ to ‘1’. This derived address is reserved for internal use and should not be used. Even though the device will acknowledge communication attempts to this address, it will not function as normal, and should therefore be avoided.

12.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

12.4 Memory Map Addressing

All memory locations are 16-bit addressable in little-endian byte order.

12.5 Memory Map Data

Each 16-bit memory map address stores a single byte (8 bits), making the memory map byte-addressable. Since the data is packed in a little-endian sequence, a 16-bit value starting at, for example, address 0x1014 will have its least significant byte at address 0x1014 and its most significant byte at address 0x1015.

12.6 RDY/IRQ

The IQS396 has an open-drain active low RDY signal to inform the master that updated data is available. The IQS396 will pull the RDY line low to indicate that it has opened a communications window, or “RDY window”, for the master to read the new updated data. While the master can communicate with the device at any time according to the *Force Comms Method*, it is recommended to use the RDY signal for optimal power consumption. Integrating the RDY signal as an interrupt input allows the master MCU to read and write data efficiently.

The device provides both streaming and event modes. In streaming mode, the RDY line toggles continuously, with each sensing cycle, whereas in event mode the RDY toggles only when specific events occurs. The types of events that trigger the RDY window are configurable in the *Event Mask* register.

12.7 Read and Write Operations

12.7.1 I²C Read From Specific Address

A typical read operation is displayed in Figure 12.1. The master device waits for the RDY line of the IQS396 to go low, indicating the availability of new data and an available communication window. Once the RDY interrupt is triggered, the master initiates communication by sending a start condition followed by the device address and a write command. The IQS396 responds with an acknowledgement, after which the master device will transmit two bytes defining the register address. The master then sends a repeated start condition, followed by the device address with a read command. The IQS396 transmits data from the requested address and will continue to do so while the master acknowledges each byte. The read operation is ended when the master does not acknowledge the last byte received and produces a stop condition.

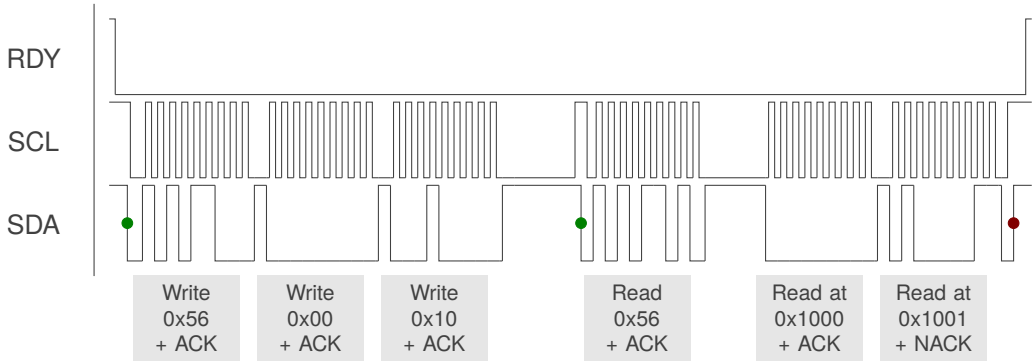


Figure 12.1: I²C Read Example — Read System Control Registers 0x1000 and 0x1001

12.7.2 I²C Write To Specific Address

The write operation is displayed in Figure 12.2. Similar to the read transaction, when the RDY interrupt is triggered, the master initiates communication by sending a start condition followed by the device address and a write command. The IQS396 responds with an acknowledgement, after which the master device transmits two bytes defining the register address. The slave acknowledges the register address bytes. The master may then write a series of bytes to the register address and the addresses that follow, with each byte being acknowledged by the slave. The write operation is ended when the master produces a stop condition.

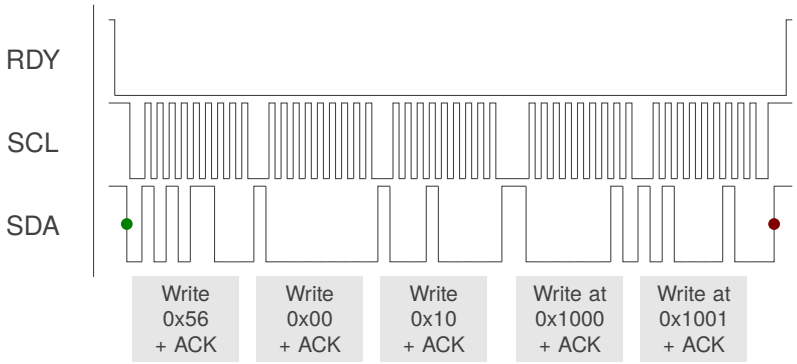


Figure 12.2: I²C Write Example — Write Two Bytes to System Control Registers 0x1000 and 0x1001

12.7.3 Modifying Bits Over I²C

When modifying individual bits in a register, it is recommended to read the register first, make the necessary modifications, and then write the updated value back to the IQS396 register to prevent unintentional bit changes.

For example, setting the *Ack Reset* bit and *Power Mode* setting would involve:

- Read the *System Control* Registers (0x1000 and 0x1001) as illustrated in Figure 12.1.
- Set the *Ack Reset* bit using the bitwise OR operator. For example:

  READ_VALUE OR 0x01

- Set the *Power Mode* setting by clearing the bit field using a bitwise AND operation, then setting the bit field value with an OR operation. For example, to set the *Power Mode* to 'Auto':

  (READ_VALUE AND 0xF8) OR 0x02

- Write the new values back over I²C, as shown in Figure 12.2.

Read-modify-write transactions should be done in a single communication window, using I²C restart conditions. Please refer to Section 12.9 for more information regarding multiple I²C transactions in a single communication window.

12.8 I²C Timeout

If the communication window is not serviced within the *I²C Timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be lost, so this should be avoided. The default I²C timeout period is set to 250 ms.

12.9 Terminate Communication

With the *Terminate Comms Window* setting enabled in the *Power Settings* register, a standard I²C STOP ends the current communication window. If multiple I²C transactions need to be done, then they should be strung together using repeated-start conditions instead of giving a STOP. Allowing an I²C STOP to terminate the communication window is the recommended method, as illustrated in Figures 12.1 and 12.2.

This behaviour can be temporarily disabled by clearing the *Terminate Comms Window* setting. In this case, an I²C STOP will NOT terminate the communication window. Instead, the communication window can be closed manually, as desired, by setting the *Terminate Comms Window* bit as the final I²C transaction, followed by a STOP.

12.10 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside a communication window (while RDY is high).

12.11 Event Mode Communication

The device can be set up to bypass the communication window when no activity is sensed by setting the *Event Mode* bit in the *Power Settings* register. This is usually enabled since the master does not need to be interrupted unnecessarily during every cycle if no activity occurs. The communication will resume (RDY will indicate available data) if an enabled event occurs. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

Event mode can only be entered if the following requirements are met:

- Events must be serviced by reading from the *Event Flags* register to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every cycle, similar to streaming mode.
- The *Show Reset* bit in the *Device Status* register has been cleared by setting the *Ack Reset* bit in *System Commands*.

12.11.1 Events

Numerous events can be individually enabled in the *Event Mask* register to trigger communication in Event Mode:

- Power mode changes
- ATI events
- Touch events
- Proximity events
- Haptics events

12.11.2 Force Communication

In streaming mode, the IQS396 I²C will provide RDY windows at regular intervals specified by the relevant power mode report rate. This will provide the master with regular opportunities to perform I²C communication as necessary.

If the device is placed in Event Mode or Halt Mode, the IQS396 will not open RDY windows unless certain conditions are met. A new RDY window can be requested by writing 0xFF over I²C, followed by a stop condition. After a short delay, the IQS396 will pull the RDY line low and open a new communication window. This is shown in Figure 12.3.

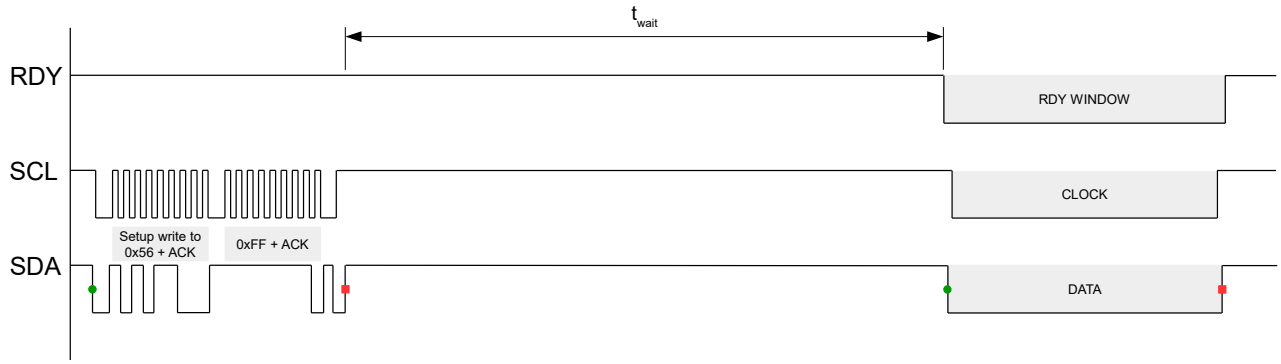


Figure 12.3: Force Comms Diagram

After a short delay, a new communication window will be made available, indicated by the RDY signal. The delay between the communication request and the opening of a RDY window (t_{wait}) is application specific, but will typically be under 2 milliseconds.

13 I²C Memory Map

Table 13.1: I²C Memory Map

Address	Length	Description	Default	Notes
Read-Only	**No. Bytes**	**Version Info**		
0x00 - 0x09	10	Version Details		Section A.1
Read-Write	**No. Bytes**	**System Control Settings**		
0x1000	1	System Commands		Section A.2
0x1001	1	Power Settings		Section A.3
0x1002	1	Event Masks		Section A.4
0x1003	1	ULP, Autoresonance and Watchdog Settings		Section A.5
0x1004	2	AutoProx Threshold	200	[csi^{i}]
0x1005				
0x1006	2	NP Low Report Rate	200	0 – 3000 [ms]
0x1007				
0x1008	2	ULP Low Report Rate	200	0 – 3000 [ms]
0x1009				
0x100A	2	NP High Report Rate	43	0 – 3000 [ms]
0x100B				
0x100C	2	ULP High Report Rate	43	0 – 3000 [ms]
0x100D				
0x100E	2	Power Mode Timeout	5000	[ms]
0x100F				
0x1010	2	I²C Timeout	250	[ms]
0x1011				
Read-Write	**No. Bytes**	**ProxFusion® Settings**		
0x1012	1	ProxFusion Settings 0		Section A.6
0x1013	1	ProxFusion Settings 1		Section A.7
0x1014	2	Proximity Timeout	20000	[ms]
0x1015				
0x1016	2	Touch Timeout	20000	[ms]
0x1017				
0x1018	2	ATI Delay	2000	[ms]
0x1019				
0x101A	1	Low Report Rate Counts Filter Beta	1	0 – 15
0x101B	1	Low Report Rate LTA Filter Beta	8	0 – 15
0x101C	1	Low Report Rate Fast LTA Filter Beta	1	0 – 15
0x101D	1	Low Report Rate ULP LTA Filter Beta	5	0 – 15
0x101E	2	Low Report Rate Fast LTA Filter Bound	5	0 – 8000
0x101F				
0x1020	1	High Report Rate Counts Filter Beta	1	0 – 15
0x1021	1	High Report Rate LTA Filter Beta	8	0 – 15
0x1022	1	High Report Rate Fast LTA Filter Beta	1	0 – 15
0x1023	1	High Report Rate ULP LTA Filter Beta	5	0 – 15
0x1024	2	High Report Rate Fast LTA Filter Bound	5	0 – 8000
0x1025				

Continued on next page...

Table 13.1: I²C Memory Map (Continued)

0x1026 0x1027	2	Proximity Threshold	500	[csi]
0x1028	1	Proximity Debounce	0x22	Section A.8
0x1029	1	Proximity Hysteresis	0	
0x102A 0x102B	2	Touch Threshold	1200	[csi]
0x102C	1	Touch Debounce	0x11	Section A.9
0x102D	1	Touch Hysteresis	50	
0x102E	1	ProxFusion ATI Band	15	[%]
0x102F	1	Reserved		
0x1030 0x1031	2	LTA Halt Threshold	500	[csi]
Read-Write	**No. Bytes**	**ProxFusion® ATI Settings**		
0x1032 0x1033	2	High Sensitivity ATI Base	4000	[csi]
0x1034 0x1035	2	High Sensitivity ATI Target	4000	[csi]
0x1036 0x1037	2	Low Sensitivity ATI Base	5000	[csi]
0x1038 0x1039	2	Low Sensitivity ATI Target	5000	[csi]
0x103A 0x103B	2	ProxFusion Dividers		Section A.10
0x103C 0x103D	2	ProxFusion Compensation		Section A.11
Read-Write	**No. Bytes**	**Haptic Configuration**		
0x103E	1	Haptic Control		Section A.12
0x103F	1	Over Temperature Settings		Section A.13
0x1040 0x1041	2	H-Bridge Setup	0x353E	Section A.14
0x1042	1	Pattern 1 Segments	3	Range 0-3
0x1043	1	Pattern 1 Segment 0 Start Duty Cycle	0	Range 0-99
0x1044	1	Pattern 1 Segment 0 End Duty Cycle	99	Range 0-99
0x1045	1	Pattern 1 Segment 0 Duration	85	
0x1046	1	Pattern 1 Segment 1 Start Duty Cycle	99	Range 0-99
0x1047	1	Pattern 1 Segment 1 End Duty Cycle	99	Range 0-99
0x1048	1	Pattern 1 Segment 1 Duration	85	
0x1049	1	Pattern 1 Segment 2 Start Duty Cycle	99	Range 0-99
0x104A	1	Pattern 1 Segment 2 End Duty Cycle	0	Range 0-99
0x104B	1	Pattern 1 Segment 2 Duration	85	
0x104C	1	Pattern 1 Setup	0x00	Section A.15
0x104D	1	Pattern 2 Segments	0	Range 0-3
0x104E	1	Pattern 2 Segment 0 Start Duty Cycle	0	Range 0-99
0x104F	1	Pattern 2 Segment 0 End Duty Cycle	0	Range 0-99
0x1050	1	Pattern 2 Segment 0 Duration	0	
0x1051	1	Pattern 2 Segment 1 Start Duty Cycle	0	Range 0-99

Continued on next page...

Table 13.1: I²C Memory Map (Continued)

0x1052	1	Pattern 2 Segment 1 End Duty Cycle	0	Range 0-99
0x1053	1	Pattern 2 Segment 1 Duration	0	
0x1054	1	Pattern 2 Segment 2 Start Duty Cycle	0	Range 0-99
0x1055	1	Pattern 2 Segment 2 End Duty Cycle	0	Range 0-99
0x1056	1	Pattern 2 Segment 2 Duration	0	
0x1057	1	Pattern 2 Setup	0x00	Section A.15
0x1058	1	Pattern 3 Segments	0	Range 0-3
0x1059	1	Pattern 3 Segment 0 Start Duty Cycle	0	Range 0-99
0x105A	1	Pattern 3 Segment 0 End Duty Cycle	0	Range 0-99
0x105B	1	Pattern 3 Segment 0 Duration	0	
0x105C	1	Pattern 3 Segment 1 Start Duty Cycle	0	Range 0-99
0x105D	1	Pattern 3 Segment 1 End Duty Cycle	0	Range 0-99
0x105E	1	Pattern 3 Segment 1 Duration	0	
0x105F	1	Pattern 3 Segment 2 Start Duty Cycle	0	Range 0-99
0x1060	1	Pattern 3 Segment 2 End Duty Cycle	0	Range 0-99
0x1061	1	Pattern 3 Segment 2 Duration	0	
0x1062	1	Pattern 3 Setup	0x00	Section A.15
⋮	33	⋮	⋮	⋮
0x1084	1	Pattern 7 Segments	0	Range 0-3
0x1085	1	Pattern 7 Segment 0 Start Duty Cycle	0	Range 0-99
0x1086	1	Pattern 7 Segment 0 End Duty Cycle	0	Range 0-99
0x1087	1	Pattern 7 Segment 0 Duration	0	
0x1088	1	Pattern 7 Segment 1 Start Duty Cycle	0	Range 0-99
0x1089	1	Pattern 7 Segment 1 End Duty Cycle	0	Range 0-99
0x108A	1	Pattern 7 Segment 1 Duration	0	
0x108B	1	Pattern 7 Segment 2 Start Duty Cycle	0	Range 0-99
0x108C	1	Pattern 7 Segment 2 End Duty Cycle	0	Range 0-99
0x108D	1	Pattern 7 Segment 2 Duration	0	
0x108E	1	Pattern 7 Setup	0x00	Section A.15
0x108F	1	Reserved		
0x1090 0x1091	2	Waveform 0 Pattern Selection	0x0001	Section A.16
0x1092	1	Waveform 0 Stage 1 Half Cycles	0x00	
0x1093	1	Waveform 0 Stage 2 Half Cycles	0x00	
0x1094	1	Waveform 0 Stage 3 Half Cycles	0x00	
0x1095	1	Waveform 0 Stage 4 Half Cycles	0x00	
0x1096	1	Reserved		
0x1097 0x1098	2	Waveform 1 Pattern Selection	0x0000	Section A.16
0x1099	1	Waveform 1 Stage 1 Half Cycles	0x00	
0x109A	1	Waveform 1 Stage 2 Half Cycles	0x00	
0x109B	1	Waveform 1 Stage 3 Half Cycles	0x00	
0x109C	1	Waveform 1 Stage 4 Half Cycles	0x00	
0x109D	1	Reserved		

Continued on next page...

Table 13.1: I²C Memory Map (Continued)

0x109E 0x109F	2	Waveform 2 Pattern Selection	0x0000	Section A.16
0x1100	1	Waveform 2 Stage 1 Half Cycles	0x00	
0x1101	1	Waveform 2 Stage 2 Half Cycles	0x00	
0x1102	1	Waveform 2 Stage 3 Half Cycles	0x00	
0x1103	1	Waveform 2 Stage 4 Half Cycles	0x00	
0x1104	1	Reserved		
0x1105 0x1106	2	PWM Frequency	20000	Range 15000-20000
0x1107 0x1108	2	LRA Frequency	170	Range 100-300
0x1109	1	Autoresonance Backoff	40	Range 0-100
0x110A	1	Reserved	0x00	Set to ’0x00’
Read-Only	**No. Bytes**	**System Flags**		
0x2000	1	Power Mode Flags		Section A.17
0x2001	1	Device Status		Section A.18
0x2002	1	System Event Flags		Section A.19
0x2003	1	ProxFusion® States		Section A.20
0x2004	1	Info Flags		Section A.21
0x2005	1	Button Event Flags		Section A.22
Read-Only	**No. Bytes**	**ProxFusion®Counts**		
0x2006 0x2007	2	Raw Counts		
0x2008 0x2009	2	Inverted Counts		[csi]
0x200A 0x200B	2	Filtered Counts		[csi]
0x200C 0x200D	2	Reserved		
0x200E 0x200F	2	Filtered LTA		[csi]
0x2010 0x2011	2	Reserved		
0x2012 0x2013	2	Delta		[Signed csi]
0x2014 0x2015 0x2016 0x2017	4	Reserved		

[i] Linearised Counts (csi) - see Section 10.2.1

14 Ordering Information

14.1 Ordering Code

Table 14.1: Order Code Description

IQS396 zzz ppb

IC NAME				IQS396
CONFIGURATION	zzz	=	001	I²C proximity/touch button with haptics feedback
			002	I²C proximity/touch button with haptics feedback. Includes address select input pin and optimized trigger reporting
			100	Standalone inductive proximity/touch button with haptics feedback
			200	Standalone capacitive proximity/touch button with an integrated noise filtering algorithm
PACKAGE TYPE	pp	=	QF	QFN-20 Package
BULK PACKAGING	b	=	R	QFN-20 Reel (2000 pcs/reel)

Other order codes for standalone operation are available on special request – please contact Azoteq.

14.2 Top Marking

"IQS396" = Product Name

"ppp" = Product Code

"xx" = Batch Code

Figure 14.1: IQS396-QFN20 Package Top Marking

"IQS3hd" = Product Name

"ppp" = Product Code

"xx" = Batch Code

Figure 14.2: QFN20 Generic Package Top Marking

15 Package Information

15.1 QFN20 Package Outline

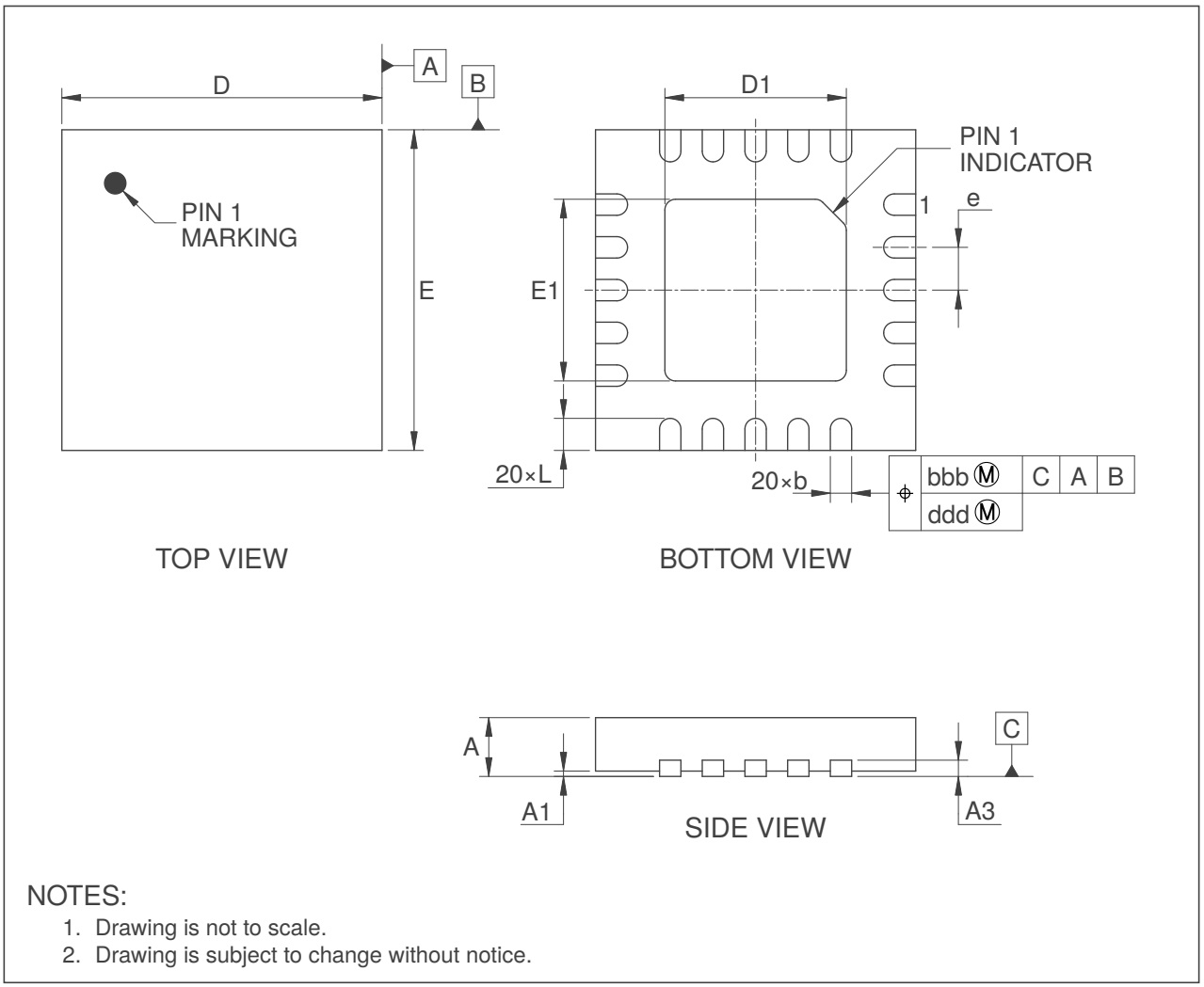


Figure 15.1: QFN20 Package Outline

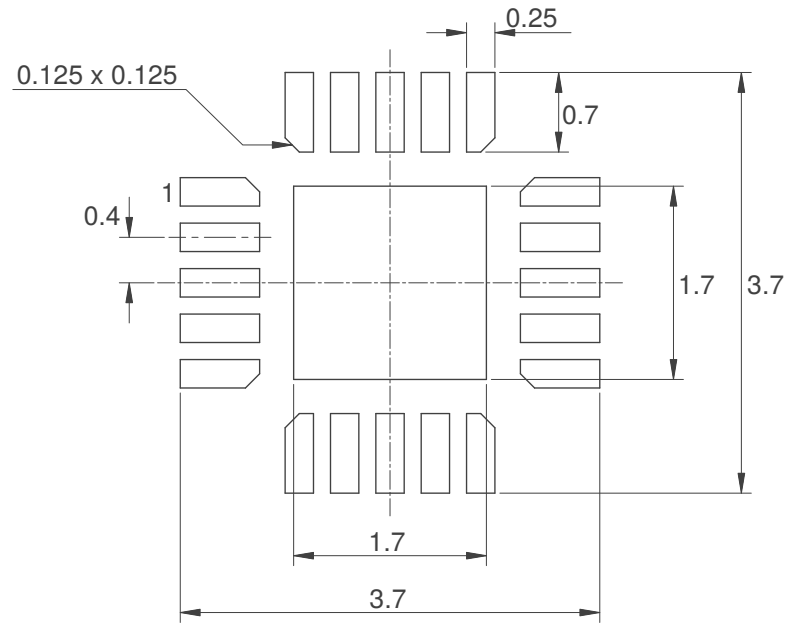
Table 15.1: QFN20 Package Dimensions [mm]

Dimension	Millimeters		
	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

Table 15.2: QFN20 Package Tolerances [mm]

Tolerance	Millimeters
bbb	0.07
ddd	0.05

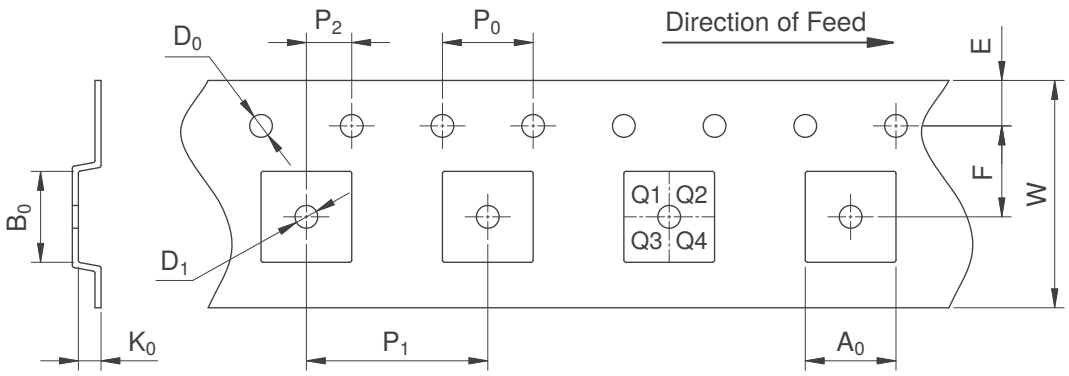
15.2 QFN20 Recommended Footprint



NOTES:
1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 15.2: QFN20 Recommended Footprint

15.3 Tape and Reel Specifications

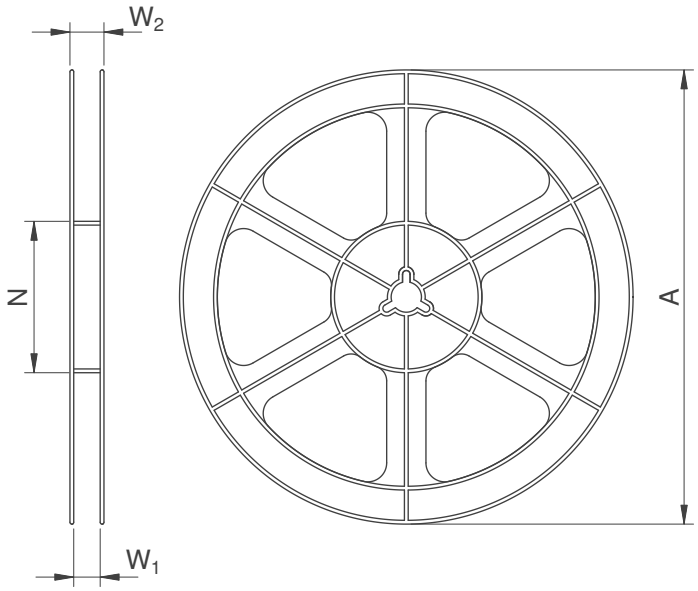


NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 15.3: Carrier Tape Specification

Table 15.3: Carrier Tape Dimensions [mm]

Dimension	Package
	QFN20
A_0	3.30
B_0	3.30
K_0	0.75
D_0	1.50
D_1	1.55
E	1.75
F	5.50
P_0	4.00
P_1	8.00
P_2	2.00
W	12.00
Pin 1 Quadrant	Q2



NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 15.4: Reel Specification

Table 15.4: Reel Dimensions [mm]

Dimension	Package
	QFN20
A	178
N	60
W_1	12.4
W_2 (Max)	18.4

A Memory Map Descriptions

A.1 Version Information (0x00 – 0x09)

Address	Category	Name	IQS396-xxx			
			001	002	100	200
0x00	Version Information	Product Number	2470	2470	3677	3691
0x01		Major Version	1	1	1	1
0x02		Minor Version	0	1	0	0
0x03		Reserved				
0x04						
0x05 - 0x09		Reserved				

A.2 System Commands (0x1000)

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Reseed	Reserved	ATI	Soft Reset	Ack Reset

- Bit 4: **Reseed ProxFusion Channel**
  - 0: No action
  - 1: Reseed the ProxFusion channel LTA
  - Bit automatically cleared
- Bit 2: **ATI ProxFusion Channel**
  - 0: No action
  - 1: Perform ATI calibration of the ProxFusion channel
  - Bit automatically cleared
- Bit 1: **Soft Reset**
  - 0: No action
  - 1: Soft reset the device
  - Bit automatically cleared
- Bit 0: **Ack Reset**
  - 0: No action
  - 1: Acknowledge a device reset
  - Bit automatically cleared

A.3 Power Settings (0x1001)

Bit	7	6	5	4	3	2	1	0
Description	Terminate Comms	Interface Select		Reserved		Power Mode Setting		

- Bit 7: **Terminate Comms on Stop**
  - 0: Keep I^2C communications window open on I^2C stop condition
  - 1: Close I^2C communications window on I^2C stop condition
- Bit 5-6: **Interface select**
  - 0: Streaming mode enabled. An I^2C communications window is opened every cycle.
  - 1: Event mode enabled. An I^2C communications window is opened only if an enabled event occurs.
  - 2: Reserved
  - 3: Standalone mode. I^2C is disabled.
- Bit 0-2: **Power Mode Setting**
  - 0: Normal Power
  - 1: Ultra Low Power
  - 2: Auto

A.4 Event Masks (0x1002)

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Over-Temperature Event	Haptics Event	Touch Event	Proximity Event	ATI Event	Power Mode Event

- Bit 5: **Over-Temperature Event**
  - 0: Disabled
  - 1: Open an I^2C communications window on over-temperature events
- Bit 4: **Haptics Event**
  - 0: Disabled
  - 1: Open an I^2C communications window on haptics events
- Bit 3: **Touch Event**
  - 0: Disabled
  - 1: Open an I^2C communications window on touch events
- Bit 2: **Proximity Event**
  - 0: Disabled
  - 1: Open an I^2C communications window on proximity events
- Bit 1: **ATI Event**
  - 0: Disabled
  - 1: Open an I^2C communications window on ATI events
- Bit 0: **Power Mode Event**
  - 0: Disabled
  - 1: Open an I^2C communications window on power mode changes

A.5 ULP, Autoresonance and Watchdog Settings (0x1003)

Bit	7	6	5	4	3	2	1	0
Description	Recommend Recalibrate	Disable Read-Only Check	Watchdog Period			AutoProx Enable	AutoProx Conversion Setting	

- Bit 7: **Recommend Recalibrate**
  - 0: Disabled
  - 1: Enabled
- Bit 6: **Disable Read-Only Check**
  - 0: Disabled
  - 1: Enabled
- Bit 3-5: **Watchdog Period**
  - 3: 33 ms
  - 4: 65 ms
  - 5: 257 ms
  - 6: 511 ms
  - 7: 1023 ms
- Bit 2: **AutoProx Enable**
  - 0: AutoProx disabled
  - 1: AutoProx enabled
- Bit 0-1: **AutoProx Conversion Setting**
  - 0: Update all channels and UIs after 4 AutoProx conversions
  - 1: Update all channels and UIs after 8 AutoProx conversions
  - 2: Update all channels and UIs after 16 AutoProx conversions
  - 3: Update all channels and UIs after 32 AutoProx conversions

A.6 ProxFusion Settings 0 (0x1012)

Bit	7	6	5	4	3	2	1	0
Description	ATI Mode		Dual Threshold	Inverse	Reserved			

- Bit 6-7: **ATI Mode**
  - 0: Disabled
  - 1: Divider Only
  - 2: Compensation Only
  - 3: Divider And Compensation
- Bit 5: **Dual Threshold**
  - Allow button events to trigger for both positive and negative delta values
  - 0: Disabled
  - 1: Enabled
- Bit 4: **Inverse**
  - Set button events to trigger for negative deltas. May be necessary for inductive sensing.
  - 0: Disabled
  - 1: Enabled

A.7 ProxFusion Settings 1 (0x1013)

Bit	7	6	5	4	3	2	1	0
Description	Enable FOsc Tx	Noise Algorithm	Sensing Mode		Conversion Frequency			

- Bit 7: **F_{OSC} Tx**
  - 0: Disabled
  - 1: Run sensor with TX at F_{OSC} frequency. Recommended only for inductive sensing.
- Bit 6: **Noise Algorithm**
  - 0: Disabled
  - 1: Enabled. Recommended only for capacitive sensing.
- Bit 4-5: **Sensing Mode**
  - 0: Disabled
  - 1: Self-Capacitance
  - 2: Inductance
- Bit 0-3: **Conversion Frequency**

  The following are recommended example values:
  - 3: 1.750 MHz
  - 7: 0.875 MHz
  - 15: 0.4375 MHz

  Note: The maximum recommended conversion frequency for capacitive sensing is 1 MHz.

A.8 Proximity Debounce (0x1028)

Bit	7	6	5	4	3	2	1	0
Description	Debounce Exit				Debounce Enter			

- Bit 4-7: **Debounce Exit**
  - 4-bit value
  - Number of high-frequency samples while exiting proximity state
- Bit 0-3: **Debounce Enter**
  - 4-bit value
  - Number of high-frequency samples while entering proximity state

A.9 Touch Debounce (0x102C)

Bit	7	6	5	4	3	2	1	0
Description	Debounce Exit				Debounce Enter			

- Bit 4-7: **Debounce Exit**
  - 4-bit value
  - Number of high-frequency samples while exiting touch state
- Bit 0-3: **Debounce Enter**
  - 4-bit value
  - Number of high-frequency samples while entering touch state

A.10 ProxFusion Dividers (0x103A)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Fine Divider					Coarse Gain

Bit	7	6	5	4	3	2	1	0
Description	Coarse Gain							

- Bit 9-13: **Fine Divider**
  - 5-bit value
- Bit 0-8: **Coarse Gain**
  - 9-bit value

A.11 ProxFusion Compensation (0x103C)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	Compensation Divider					Compensation Selection	

Bit	7	6	5	4	3	2	1	0
Description	Compensation Selection							

- Bit 10-14: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation**
  - 10-bit value

A.12 Haptics Control (0x103E)

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Enable Haptics	Reserved	Waveform Selection			Trigger Haptics

- Bit 5: **Enable Haptics**
  - 0: Haptics Output Enabled
  - 1: Haptics Output Disabled
- Bit 1-3: **Waveform Selection**
  - 0: WAV0
  - 1: WAV1
  - 2: WAV2

- Bit 0: **Trigger Haptics**
  - 0: Haptics not triggered
  - 1: Haptics triggered
  - Bit automatically cleared

A.13 Over-Temperature Settings (0x103F)

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Enable Hysteresis	Trip Temperature			

- Bit 4: **Enable Hysteresis**
  - 0: Over-temperature hysteresis filter disabled
  - 1: Over-temperature hysteresis filter enabled
- Bit 0-3: **Trip Temperature**
  - 0: 29°C
  - 1: 36°C
  - 2: 44°C
  - 3: 49°C
  - 4: 56°C
  - 5: 64°C
  - 6: 71°C
  - 7: 81°C
  - 8: 89°C
  - 9: 99°C
  - 10: 106°C
  - 11: 116°C
  - 12: 126°C
  - 13: 136°C
  - 14: 146°C
  - 15: 159°C

A.14 H-Bridge Setup (0x1040)

Bit	15	14	13	12	11	10	9	8
Description	Reserved			Ground Inactive Pins	Reserved	Drive strength Select		

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Slew Rate		Slew Rate Protection	Shoot-through protection	Over-Temperature Protection	Reserved

- Bit 12: **Ground Inactive Pins**
  - 0: Do not ground inactive pins
  - 1: Ground inactive pins
- Bit 8-10: **Drive Strength**
  - 0: DRV_{OFF}
  - 1: DRV_{1}
  - 2: DRV_{2A}
  - 3: DRV_{2B}
  - 4: DRV_{3}
  - 5: DRV_{5}
- Bit 4-5: **Slew Rate Selection**
  - 0: 20V/us
  - 1: 40V/us

- 2: 80V/us
- 3: 160V/us

- Bit 3: **Slew Rate Protection**
  - 0: Slew Rate Protection Disabled
  - 1: Slew Rate Protection Enabled
- Bit 2: **Shoot-Through Protection**
  - 0: Shoot-Through Protection Disabled
  - 1: Shoot-Through Protection Enabled
- Bit 1: **Over-Temperature Protection**
  - 0: Over-Temperature Protection Disabled
  - 1: Over-Temperature Protection Enabled

A.15 Pattern Setup (0x104C, 0x1057, 0x1062, ..., 0x108E)

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Auto-resonance	Invert

- Bit 1: **Autoresonance**
  - 0: Disable autoresonance
  - 1: Enable autoresonance
- Bit 0: **Invert**
  - 0: Do not invert pattern
  - 1: Invert pattern

A.16 Waveform Pattern Selection (0x1090, 0x1097, 0x109E)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	Stage 4			Stage 3			Stage2

Bit	7	6	5	4	3	2	1	0
Description	Stage 2		Stage 1			Stage 0		

- Bit 12-14: **Stage 4**
  - 0: None
  - 1: Pattern 1
  - 2: Pattern 2
  - 3: Pattern 3
  - 4: Pattern 4
  - 5: Pattern 5
  - 6: Pattern 6
  - 7: Pattern 7
- Bit 9-11: **Stage 3**
  - 0: None
  - 1: Pattern 1
  - 2: Pattern 2
  - 3: Pattern 3
  - 4: Pattern 4
  - 5: Pattern 5
  - 6: Pattern 6
  - 7: Pattern 7
- Bit 6-8: **Stage 2**
  - 0: None
  - 1: Pattern 1
  - 2: Pattern 2
  - 3: Pattern 3

- 4: Pattern 4
- 5: Pattern 5
- 6: Pattern 6
- 7: Pattern 7

- Bit 3-5: **Stage 1**
  - 0: None
  - 1: Pattern 1
  - 2: Pattern 2
  - 3: Pattern 3
  - 4: Pattern 4
  - 5: Pattern 5
  - 6: Pattern 6
  - 7: Pattern 7
- Bit 0-2: **Stage 0**
  - 0: None
  - 1: Pattern 1
  - 2: Pattern 2
  - 3: Pattern 3
  - 4: Pattern 4
  - 5: Pattern 5
  - 6: Pattern 6
  - 7: Pattern 7

A.17 Power Mode Flags (0x2000)

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Power Mode	

- Bit 0-1: **Power Mode**
  - 0: Normal Power
  - 1: Ultra Low Power

A.18 Device Status (0x2001)

Bit	7	6	5	4	3	2	1	0
Description	Reserved						AutoProx Error	Show Reset

- Bit 1: **AutoProx Error**
  - 0: Disabled
  - 1: An error occurred with the AutoProx limits. The device will perform regular measurements rather than Auto-Prox conversions in Ultra Low power mode.
- Bit 0: **Show Reset**
  - 0: Disabled
  - 1: System reset event occurred

A.19 System Event Flags (0x2002)

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Haptics Event	Touch Event	Proximity Event	ATI Event	Power Mode Event

- Bit 5: **Over-Temperature Event**
  - 0: No event
  - 1: Over-Temperature event occurred
  - Cleared on read
- Bit 4: **Haptics Event**
  - 0: No event
  - 1: Haptics event occurred
  - Cleared on read
- Bit 3: **Touch Event**
  - 0: No event
  - 1: Touch event occurred
  - Cleared on read
- Bit 2: **Proximity Event**
  - 0: No event
  - 1: Proximity event occurred
  - Cleared on read
- Bit 1: **ATI Event**
  - 0: No event
  - 1: ATI event occurred
  - Cleared on read
- Bit 0: **Power Mode Event**
  - 0: No event
  - 1: Power mode change occurred
  - Cleared on read

A.20 ProxFusion States (0x2003)

Bit	7	6	5	4	3	2	1	0
Description	Reserved						ATI Error	Reserved

- Bit 1: **ATI Error**
  - 0: No error
  - 1: ProxFusion channel failed to calibrate correctly

A.21 Info Flags (0x2004)

Bit	7	6	5	4	3	2	1	0
Description	Reserved				Report Rate	Sensitivity	Debounce	Output State

- Bit 3: **Report Rate**
  - 0: Slow sampling
  - 1: Fast Sampling.
- Bit 2: **Sensitivity**
  - 0: Low sensitivity
  - 1: High sensitivity.
- Bit 1: **Debounce**
  - 0: Button UI not currently debouncing
  - 1: Button UI currently debouncing by sampling at normal power report rate.
- Bit 0: **Output State**
  - 0: Button UI delta currently below threshold
  - 1: Button UI delta currently above threshold. Button is considered “pressed”.

A.22 Button Event Flags (0x2005)

Bit	7	6	5	4	3	2	1	0
Description	Current Power Mode	Report Rate	Sensitivity	Touch Event	Proximity Event	LTA Halt	Debounce	Output State

- Bit 2: **Touch Event**
  - 0: No event
  - 1: Touch event. *Output State* transitioned from ‘0’ to ‘1’.
- Bit 1: **Proximity Event**
  - 0: No event
  - 1: Proximity event.
- Bit 0: **LTA Halt**
  - 0: LTA is filtering normally
  - 1: LTA filter is halted to improve channel sensitivity.

B Revision History

Release	Date	Changes
v 1.0	December 2024	Initial release
v 1.1	February 2025	Added Usage Disclaimer section
v 1.2	June 2025	IQS396-0xx, IQS396-1xx, and IQS396-2xx order codes added.
v1.4	June 2026	Minor update to block diagram. Removed 1 nF capacitor on RDY pin in reference schematics. Removed 1 nF capacitor on MCLR pin in MCLR Pin Diagram. Updated tape and reel dimensions. Corrected Digital IO Electrical Specifications. Updated ESD level for QFN20 package to 4000 V.

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