IQS377 DATASHEET

1 Multi-level trigger channel with 1 additional sensing channel. The device features an I²C communications interface, custom output pin status assignment, low power options and AC noise compensation for reliable analogue detection.

1 Device Overview

The IQS377 ProxFusion® IC is a sensor fusion device for multi-level analogue sensing. An additional channel can be used in tandem to increase the reliability and accuracy of the multi-level trigger solution. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 3 external sensor pad connections
- Configure multiple channels on external pins (Self/Mutual/Inductive)
- External sensor options:
  - Self-capacitive sensor
  - Mutual-capacitive sensor
  - Multi-level inductive sensor
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Debounce and Hysteresis
  - Dual direction trigger indication
- Built-in Signal processing options:
  - Filter halt / Activation output
  - Scalable Level Output
  - Rapid Trigger
  - Proximity UI
- Design simplicity
  - PC Software for debugging and optimal setup for performance
- Automated system power modes for optimal response vs consumption
  - Distributed ultra low power (ULP) mode
- I²C communication interface with IRQ/RDY (up to fast plus 1 MHz)
- Hardware selectable I²C Address (0x44 / 0x46).
- Event and streaming modes with dedicated Output pin assignment
- Supply Voltage 1.71 V to 3.6 V
- Package options
  - QFN20 (3 × 3 × 0.55 mm) – 0.4 mm pitch
  - WLCSP11 (1.48 x 1.08 x 0.345 mm) - interleaved 0.35 mm x 0.35 mm ball pitch

WLCSP11 Package

QFN20 Package

1.2 Applications

- Analogue Trigger
- Buttons with Multiple actuation points

1.3 Block Diagram

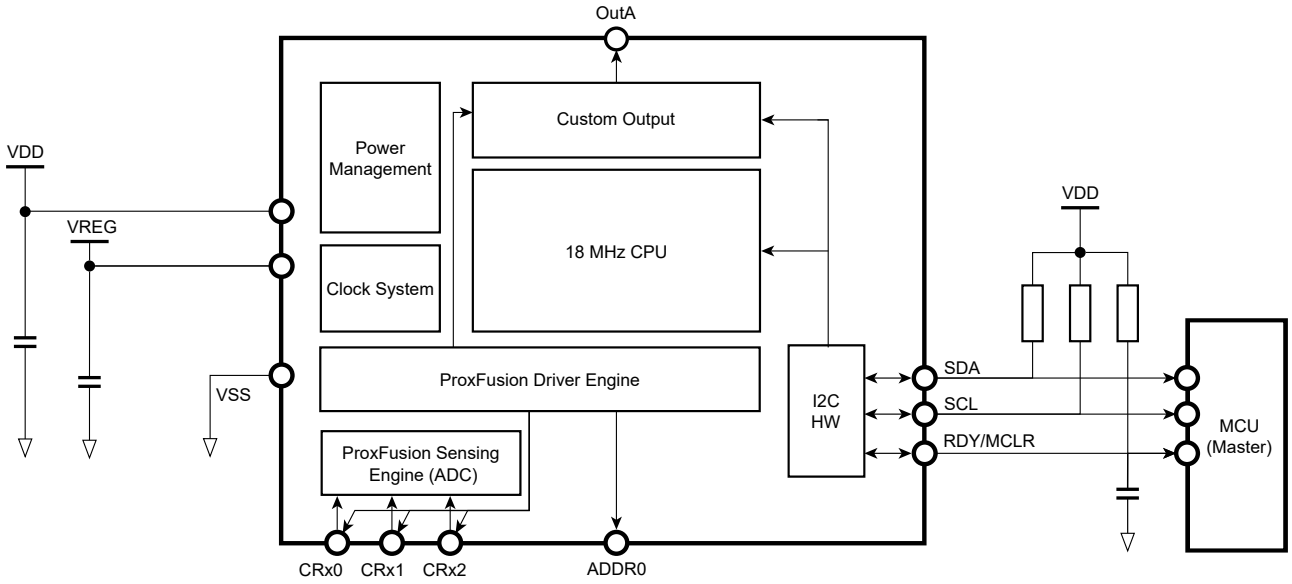
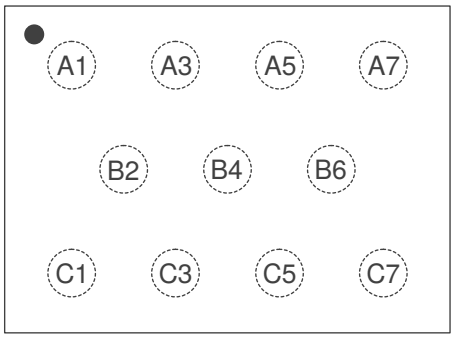


Figure 1.3: Functional Block Diagram

Contents

2 Hardware Connection

2.1 WLCSP11 Pin Diagram

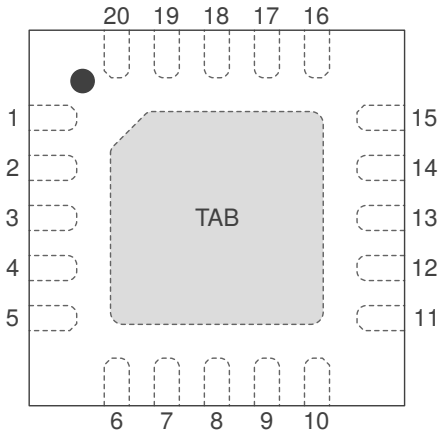


Top View

Table 2.1: 11-pin WLCSP Package

Pin no.	Signal
A1	CRx1/CTx1
A3	VREG
A5	SDA
A7	VSS
B2	CRx0/CTx0
B4	OutA
B6	ADDR0
C1	CRx2/CTx2/Bias
C3	SCL
C5	VDD
C7	RDY/MCLR

2.2 QFN20 Pin Diagram



Top View

Table 2.2: 20-pin QFN Package (Top View)

Pin no.	Signal	Pin no.	Signal
1	CRx2/CTx2/Bias	11	NC
2	CRx0/CTx0	12	NC
3	CRx1/CTx1	13	NC
4	NC	14	NC
5	NC	15	NC
6	VREG	16	NC
7	OutA	17	RDY/MCLR
8	VDD	18	ADDR0
9	VSS	19	SDA
10	NC	20	SCL

Area name	Signal
TAB[i]	Thermal pad (floating)

[i] It is recommended to connect the thermal pad (TAB) to VSS.

2.3 Signal Descriptions

Table 2.3: Signal Descriptions

Function	Signal Name	Signal Type	Pin Type[ii]	Description
ProxFusion®	CRx0/CTx0	Analog	IO	ProxFusion® channel
	CRx1/CTx1	Analog	IO	
	CRx2/CTx2/Bias	Analog	IO	
	ADDR0	Digital	O	ADDR0 pad
	OutA	Digital	O	OutA pad
GPIO	RDY/MCLR	Digital	IO	Active pull-up, 200k resistor to VDD. Pulled low during POR, and MCLR function enabled by default. VPP input for OTP
I^2C	SDA	Digital	IO	I^2C Data
	SCL	Digital	IO	I^2C Clock
Power	VDD	Power	P	Power supply input voltage
	VREG	Power	P	Internal regulated supply output
	VSS	Power	P	Analog/Digital Ground

[ii] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.4 Reference Schematic

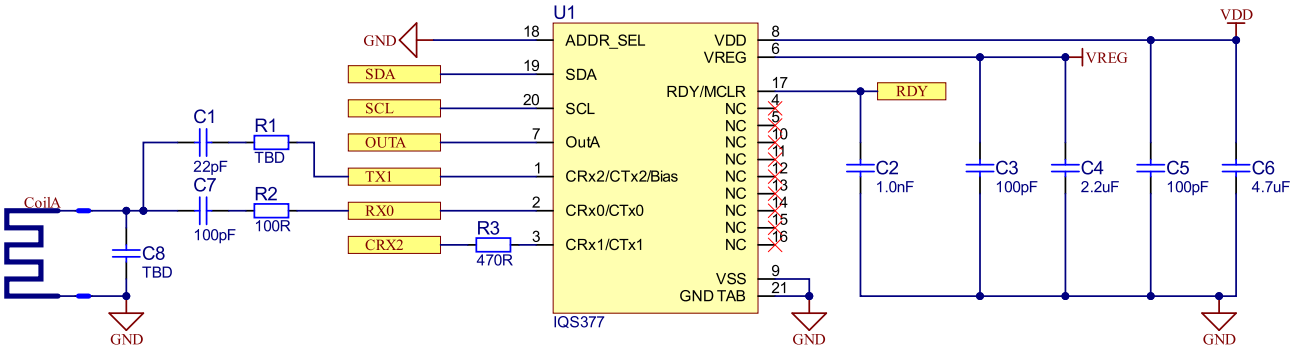


Figure 2.1: Inductive Trigger and Self Capacitance Button Reference Schematic

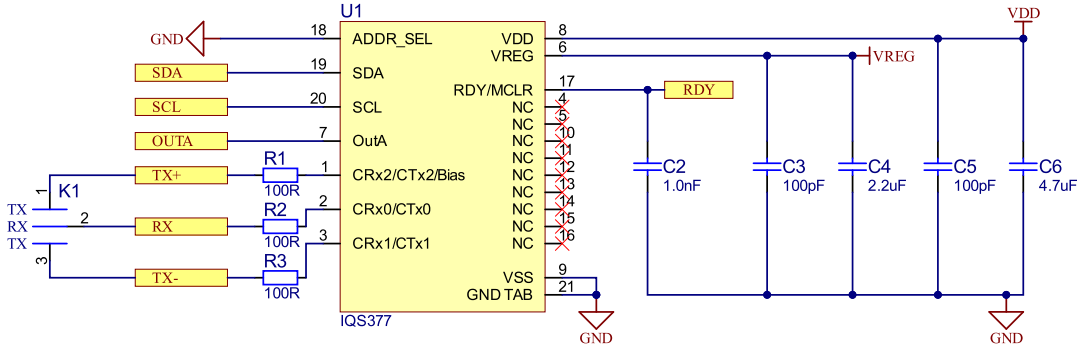


Figure 2.2: Differential Capacitance Trigger Reference Schematic

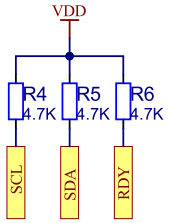


Figure 2.3: I2C communication pull-ups

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	-40	85	°C

3.2 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.6	V
VREG	Internal regulated supply output for analog domain		1.53		V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREG}$	$3\times C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR$\leq$ 200 mΩ	2[i]	4.7	13	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and external electrodes (self-capacitance mode)			400[ii]	pF
$Cm_{Tx–Rx}$	Capacitance between receiving and transmitting electrodes (mutual-capacitance mode)	0.2		9	pF
$Cp_{Rx–VSS}$	Maximum capacitance between ground and external electrodes (mutual-capacitance mode at f_{xfer} = 1 MHz)			100[ii]	pF
$\frac{Cx_{RX–VSS}}{Cm_{TX–RX}}$	Capacitance ratio for optimal SNR in mutual capacitance mode	10		20	n/a
$RCx_{Rx/Tx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[iii]	0.47	10[iv]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self-capacitance pins in self-capacitance mode	0[iii]	0.47	10[iv]	kΩ

3.3 ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[v]	± 2000	V

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to the AZD004 application note for more information regarding capacitor derating.

[ii] RCx = 0 Ω.

[iii] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

[iv] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6\times F_{xfer})}$ where C is the pin capacitance to VSS.

[v] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

3.4 Current Consumption

F_{OSC}: 14MHz
Inductive Mode Setup: ATI Target = 256, f_{xfer} = 7Mhz
Capacitive Mode Setup: ATI Target = 256, f_{xfer} = 2Mhz
Interface Selection: Event mode, Auto-Prox Cycles = 16
ULP: Auto-Prox Cycles = 16

Power mode	Active channels	Report rate [ms]	Typical Current [µA]
Normal Power	Inductive (1 coil)	0.25	1400
	Capacitive (2 channels)	0.30	1600
	Inductive (1 coil)	1	320
	Capacitive (2 channels)	1	460
Low Power	Inductive (1 coil)	10	64
	Capacitive (2 channels)	10	80
	Inductive (1 coil)	100	9
	Capacitive (2 channels)	100	12
Ultra Low Power	Inductive (1 coil)	100	9
	Capacitive (2 channels)	100	6

F_{OSC}: 18MHz
Inductive Mode Setup: ATI Target = 256, f_{xfer} = 9Mhz
Capacitive Mode Setup: ATI Target = 256, f_{xfer} = 2Mhz
Interface Selection: Event mode, Auto-Prox Cycles = 16
ULP: Auto-Prox Cycles = 16

Power mode	Active channels	Report rate [ms]	Typical Current [µA]
Normal Power	Inductive (1 coil)	0.25	1950
	Capacitive (2 channels)	0.25	2300
	Inductive (1 coil)	1	360
	Capacitive (2 channels)	1	560
Low Power	Inductive (1 coil)	10	110
	Capacitive (2 channels)	10	145
	Inductive (1 coil)	100	9
	Capacitive (2 channels)	100	12
Ultra Low Power	Inductive (1 coil)	100	9
	Capacitive (2 channels)	100	6

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

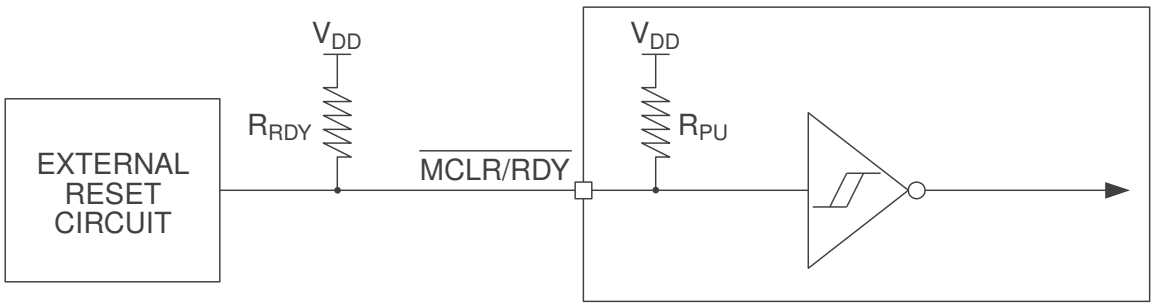


Figure 4.1: MCLR Pin Diagram

4.3 Miscellaneous Timings

Table 4.3: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	55	500-1500	7000	kHz
f_{OSC}	Master CLK frequency tolerance 14 MHz	13.23	14	14.77	MHz

4.4 Digital I/O Characteristics

Table 4.4: Digital I/O Characteristics

Parameter		Test Conditions[i]	Min	Max	Unit
V_{OL}	Output low voltage of SDA and SCL pins	I_{OL} = 20 mA $V_{DD} > 2$ V		0.4	V
		I_{OL} = 20 mA $V_{DD} \leq 2$ V		0.2 V_{DD}	
	Output low voltage of SDA and SCL pins in GPIO output mode	I_{OL} = 10 mA		0.1 V_{DD}	
	Output low voltage of RDY/MCLR	I_{OL} = 5 mA			
	Output low voltage of any other GPIO pin	I_{OL} = 10 mA			
V_{OH}	Output high voltage	I_{OH} = −5 mA	0.9 V_{DD}		V
V_{IL}	Input low voltage		V_{SS} − 0.3	0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}	V_{DD} + 0.3	V
C_b	SDA and SCL bus capacitance			550	pF

[i] Standard operating conditions:
V_{DD}: 1.8 V to 3.6 V, unless otherwise stated.
Operating temperature: −20 °C to 80 °C.

4.5 I²C Characteristics

Table 4.5: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	50		ns
$t_{SU,STO}$	Setup time for STOP	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

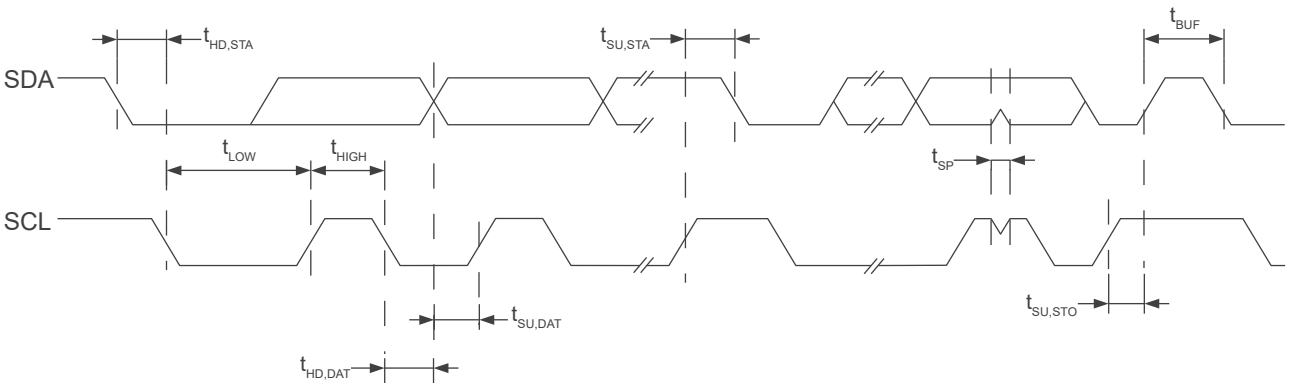


Figure 4.2: I²C Mode Timing Diagram

5 ProxFusion® Module

The IQS377 contains a single ProxFusion® module that uses patented technology to measure and process the sensor data.

5.1 Channel Options

Self-capacitive, mutual-capacitive, differential-capacitance and inductive designs are possible with the IQS377.

The below application notes provide background and information on applications where the IQS377 would be a suitable choice:

- AZD004: Azoteq Sensing Technologies
- AZD125: Capacitive Sensing Design Guide
- AZD115: Inductive Design Layout Guide
- AZD150: Mouse Button Trigger With Haptics (contact Azoteq)

5.2 Low Power Options

The IQS377 offers 3 power modes:

- Normal power mode (NP)
- Low power mode (LP)
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimized firmware setup
  - Intended for rapid wake-up from deep sleep on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are sampled at a slower rate in order to optimize power consumption

The NP, LP and ULP power modes are described in the AZD004 application note.

The currently active power mode is reported in the *System Status* register.

5.3 Power Mode Selection

The power mode is selected by writing the appropriate value to the *Power Mode* field in the *System Control* register.

In order to optimize power consumption, power modes are stepped when the power mode is set to ‘Automatic’. This moves the device to more power efficient modes when no interaction has been detected for a certain configurable time specified by the *Power Mode Timeout* register. Setting the power mode timeout to ‘0x00’ will prevent the chip from lowering the power mode.

While the power mode switching is set to either ‘Automatic’, the IQS377 will return to normal power mode regardless of the current power mode if any events are triggered. Thereafter, the automatic power mode switching will take effect.

5.4 Count Value

The sensing measurement returns a counts value for each channel. The counts value is the raw measured signal for a channel. Count values are inversely proportional to capacitance and inductance, and all other outputs are derived from this.

Counts are reported in the *Filtered Counts* registers.

5.4.1 Linearise Counts

If the *Linearise Counts* bit in the *System Configuration* register is set, the IQS377 linearises the counts before reporting them. If this option is set, the counts are inverted and the *Invert* bit must be appropriately set to ensure correct channel logic.

5.4.2 Max Counts

Each channel is limited to having a count value smaller than some limit. The limit is set by the *Max Counts* setting in the *System Configuration* register. If the ATI settings or hardware causes measured count values higher than the limit, the conversion will be stopped, and the maximum value will be read. Limiting the counts prevents the IQS377 from getting stuck under error conditions. The smallest maximum count setting that is above the expected maximum counts under normal operating conditions should be selected.

If the *Linearise Counts* bit in the *System Configuration* register is set, it is possible that a counts value greater than the maximum counts will be reported. This is because linearisation of the counts occurs after the maximum counts setting is enforced.

5.5 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value called the Long Term Average (LTA). The LTA of a sensor is slowly updated to track changes in the environment. During a Activation or Filter-Halt event, the LTA is frozen.

Channel LTA's are reported in the *Channel X LTA* registers.

5.5.1 Reseed

It is possible that there are situations which would call for a manual reseed of the LTA. A reseed takes the latest measured counts, and seeds the LTA with this value. This updates the LTA to match the latest conditions in the external environment.

A reseed command is given by setting the *Reseed* bit in the *System Control* register. The *Reseed* bit is automatically cleared once the reseed has been completed.

5.6 Filter Betas

An Infinite Impulse Response(IIR) filter is applied to the digitized raw input for both the counts value and the LTA. For more detail on IIR filtering, refer to AZD004.

Damping options for the counts and LTA filters are defined in the *Counts Filter Betas*, *LTA Filter Betas* and *LTA Fast Filter Betas* registers.

$$\text{Damping factor} = \frac{\text{Beta}}{256}$$

The NP filter betas are used when the *Current Power Mode* in the *System Status* register is 'Normal Power'. When the *Current Power Mode* is 'Low Power' or 'Ultra Low Power', the LP filter betas are used.

The *Fast Filter Band* determines when the fast beta filters are used. Fast filtering is applied to the LTA if the channel counts drift away from the LTA in the opposite direction to the sensing direction by more than the *Fast Filter Band*. Once the difference between the counts and LTA is less than the fast filter band the normal filters are used again.

5.7 Filter Halt and Activation Thresholds

Each channel has its own independently settable filter halt and Activation thresholds. These thresholds, along with the channel's counts and LTA, determine whether a channel is in a filter halt or Activation state. Once a channel enters a filter halt or Activation state, the relevant *CHx Filter Halt* or *CHx Activation* bits will be set in the *System Status* register, and will remain set until the channel leaves its filter halt or Activation state.

With non-inverted channel logic and dual direction sensing disabled, a channel will enter the filter halt state if

$$(\text{LTA} - \text{Counts}) > \text{Filter Halt Threshold}$$

for more than the number of consecutive samples specified by the *Filter Halt Debounce Enter* field in the *Filter Halt Settings* register. The channel will exit the filter halt state if the above condition is not met for more than the number of consecutive samples specified by the *Filter Halt Debounce Exit* field. The *Filter Halt Threshold* is set in the *Filter Halt Settings* register.

A channel will enter the Activation state if

$$(\text{LTA} - \text{Counts}) > \text{Activation Threshold}$$

and exit the Activation state if

$$(\text{LTA} - \text{Counts}) < (\text{Activation Threshold} - \text{Activation Hysteresis})$$

The *Activation Threshold* and *Activation Hysteresis* are set in the *Activation Settings* register.

Setting a channel's *Invert* bit in the *Sensor Setup* register will invert the logic above. This setting is required because counts increase with user interaction when sensing mutual capacitance and inductance, and decrease when sensing self capacitance.

If the *Dual Direction* bit in the *Sensor Setup* register is set, the filter halt and Activation thresholds will be applied in both directions, meaning that a channel will be in a filter halt or Activation state if

$$\text{Counts} > (\text{LTA} + \text{Threshold}) \text{ or } \text{Counts} < (\text{LTA} - \text{Threshold})$$

5.8 Power Mode Timeout

In order to optimize power consumption and performance, power modes are "stepped" when the power mode switching is set to 'Automatic'. This moves the device to more power efficient modes when no interaction has been detected for a certain (configurable) time known as the *Power Mode Timeout*. The value for the power mode to never timeout (i.e the current power mode will never progress to a lower power mode), is 0x00.

When the IQS377 *Report Rate* is set to 0 (maximum achieved rate) the device will not be able to lower the power mode automatically. Manual power mode switching will therefore be required.

5.9 Channel Timeouts

A channel will be reseeded and therefore exit a *Filter Halt* or *Activation* state if it has been in *Filter Halt* or *Activation* for longer than the relevant time specified by the *Filter Halt and Activation Event Timeouts*.

When the IQS377 *Report Rate* is set to 0 (maximum achieved rate) the *Filter Halt* or *Activation* will not trigger. Changing the Report Rate value to any other value will enable the timeouts.

5.10 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in ProxFusion® devices to provide optimal performance over a wide range of sensing electrode capacitances and inductance, without modification of external components.

The choice of ATI parameters has a significant impact on channel performance. The ATI algorithm is responsible for selecting each channel's dividers and multipliers as a gain index lookup value for the base and compensation for the target.

When *ATI Disable* in the *Sensor Setup* register is not set, the *Gain Index* register are set by the ATI algorithm using the value in the *ATI Base* register as an input to the algorithm. Generally, a lower base value will increase sensitivity.

Each channel's *Compensation Value* and *Compensation Divider* in the channel's *Compensation* register are set by the ATI algorithm using the *ATI Target*. A higher target will generally increase sensitivity.

When an ATI is triggered, the algorithm will first adjust the gain index so that the counts are as close to the *ATI Base* as possible. The *Compensation Value* and *Compensation Divider* are then adjusted until the counts are as close as possible to the ATI Target.

In certain cases it is desirable to fix the gain index at design time. For these cases, the *ATI Mode* can be set to 'ATI Target Only'.

For measurements where the conversion frequency is greater than 2MHz, the *Compensation Value* should be minimised and the *Compensation Divider* should be maximised, or both the *Compensation Value* and the *Compensation Divider* should be set to '0'. This is achieved by setting the *ATI Base* and *ATI Target* to the same value with ATI enabled, or disabling ATI and setting both the *Compensation Value* and *Compensation Divider* to '0'.

It is recommended to set the *ATI Mode* to 'Full' and to allow the ATI algorithm to select the best gain index for the desired base.

The ATI algorithm executes in a short time, and therefore goes unnoticed by the user.

5.11 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if the following is true for any channel after the ATI has completed:

- Counts are outside the **ATI Boundary** upon completion of the ATI algorithm

If this condition is met, the *ATI Error* flag will be set. The flag status is only updated again when a new ATI algorithm is performed.

A Re-ATI will not be automatically triggered if an ATI Error occurs. If an ATI Error occurs the master should manually trigger a Re-ATI using the Re-ATI bit in the *System Control* register.

5.12 Sensor Setup

To perform a measurement the IQS377, each sensor needs to be in the correct sensing mode. The IQS377 can be configured for inductive sensing, self-capacitance, mutual-capacitance and differential-capacitance. The setting to configure each sensor into the required sensing mode can be found in the *Sensor Setup* register.

6 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Only certain parameters are described below. The other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.

6.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}), also known as the conversion frequency, is set using the *Conversion Frequency Fraction* and *Conversion Frequency Period* fields in the *Conversion Frequency* register. For high resistance sensors, it might be needed to decrease f_{xfer}.

It is recommended to always set the *Conversion Frequency Fraction* to '127' and to select the conversion frequency with the *Conversion Frequency Period*.

The *Dead Time Enable* option in the *Sensor Setup* register must be considered when setting the conversion frequency. Dead time should always be enabled for capacitance measurements, and disabled for inductive measurements.

6.2 Reset

6.2.1 Reset Indication

After a reset, the *Reset Event* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *ACK Reset*. If it becomes set again, the master will know a reset has occurred, and can react appropriately.

While *Reset* bit remains set:

- The device will not be able to enter into I²C Event mode operation (i.e. streaming communication behavior will be maintained until the Reset bit is cleared)
- During the period of ATI execution, the device will provide communication windows continuously during the ATI process, resulting in a much longer time to finish the ATI routine.

6.2.2 Software Reset

The IQS377 can be reset by means of an I²C command *Soft Reset*.

6.2.3 Hardware Reset

The MCLR/RDY pin (active LOW) can be used to hard reset the device when outside an I²C communication window. For more details see Section 4.2.

7 Additional Features

7.1 OutA Functionality

OutA is freely configurable by the user *OutA Select* setting.

7.2 Multi-Level UI

The Multi-Level UI is activated once the trigger channel has passed its halt threshold. The number of levels is set with the *Number of Levels* setting.

The *Max Delta* setting needs to be set to allow the Multi-Level UI to work correctly. This can either be done by writing directly to the *Max Delta* setting or by setting the *Save Max Delta* bit in the system control register.

The *Zero Delta* setting can be set to create a starting point for the Multi-Level UI. This is useful if the sensor calibration has an unexpected offset and the default sensor delta is not equal to zero.

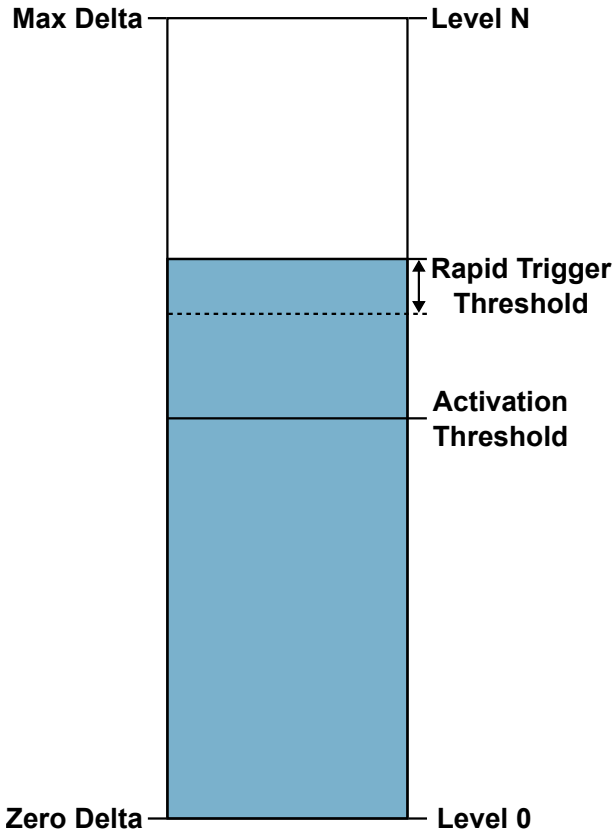


Figure 7.1: Multi-Level UI

7.3 TriggerMax™

The TriggerMax™ dynamic actuation algorithm commonly known as *Rapid Trigger* will track changes in the *Trigger Delta* value of the trigger channel when *Rapid Trigger* is enabled. The *Trigger Movement* value deduced is used to track changes in the *Trigger Level* value of a channel by following the *Trigger Delta* value of the trigger channel in a given direction depending on the state of the trigger activation bit (Section A.2: bit 12).

The *Rapid Trigger Threshold* parameter defines the difference that must occur between the *Trigger Delta* and *Trigger Movement* value of the trigger channel before the *Trigger Activation* flag may be cleared when already set or vice versa, set when already cleared. The behaviour of the algorithm is displayed in Figure 7.2.

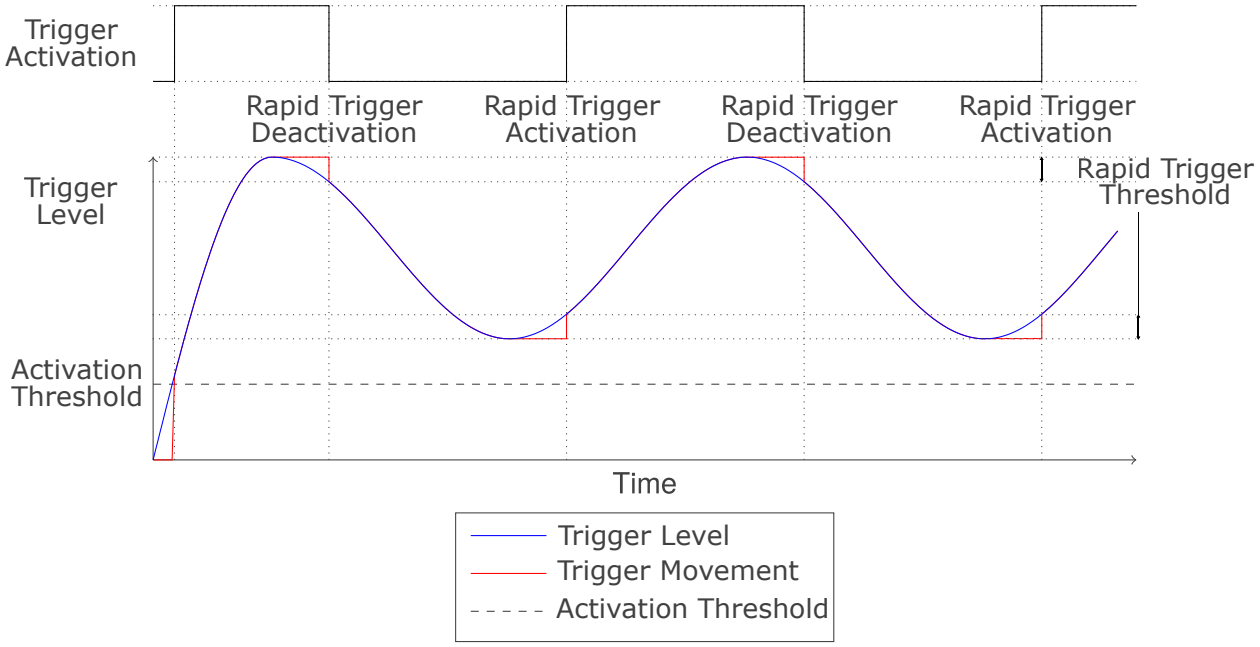


Figure 7.2: Movement Tracking Behaviour

The *Trigger Movement* is asserted based on the threshold level value defined in the *Rapid Trigger Threshold* register.

The TriggerMax™ dynamic actuation algorithm commonly known as *Rapid Trigger* may be disabled on the Trigger channel by clearing the *Enable Rapid Trigger* bit in the Section A.5 System Configuration register.

7.4 Watchdog Timer

The IQS377 implements a hardware watchdog timer. The watchdog timer is set to expire after 255 ms if not kicked and will trigger a software reset upon expiration.

During I^2C communication the watchdog timer is reset whenever a read or write occurs. Therefore, if the master initiates communication by sending an I^2C START condition and does not complete the I^2C transaction the IQS377 will reset after 255 ms.

The I^2C transaction is completed either when an I^2C STOP notification is sent by the master or when the master ends the communication as described in Section 8.10.

8 I²C Interface

8.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The RDY line is an open-drain active low implementation and indicates a communication window. The RDY pin also serves as a Master Clear (MCLR) and can be used to hard reset the device (Section 6.2.3). Byte level clock stretching is allowed. The communications interface of the IQS377 supports the following:

- *Fast-mode-plus* standard I²C up to 1 MHz.
- Streaming data as well as event mode.

The IQS377 implements 8-bit addressing with 2 bytes at each address.

8.2 Address Selection

Each order code allows for selection between two different I2C addresses. The available addresses are listed in Section 10.1.

The ADDR_SEL pin is used to select the address. Address 1 is selected when ADDR_SEL is pulled to ground. Address 2 is selected when ADDR_SEL is pulled to VDD. An external pullup or pulldown resistor is not required on the ADDR_SEL pin.

8.3 Reserved Address

The IQS377 will acknowledge an additional address derived from its selected slave address. This derived address is obtained by flipping the least significant bit of the slave address.

For every order code, the IQS377 will also acknowledge an additional debug I²C address. The debug address is for debugging purposes only and should not be used during normal operation. The debug address is the primary address with the least significant bit inverted. For example, the primary address for IQS377-001 is 0x44, and its debug address is 0x45.

8.4 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

8.5 Communication During ATI

If an ATI event is triggered then I²C communications are disabled for the duration of the ATI process.

8.6 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words meaning that two bytes are stored at each address. For example, address 0x10 will provide two bytes. The next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

8.7 RDY/IRQ

The communication has an open-drain active-LOW RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and initiate I²C reads accordingly.

The RDY line allows the master MCU to be woken from low-power/sleep when user presence is detected by the touch device. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

On the IQS377 the RDY line also serves as an MCLR pin. MCLR functionality is described in Section 6.2.3.

8.8 Communications Window

When the device has data for the master, it will pull the RDY line LOW. This indicates that the device has opened its *communications window* and is expecting the master to address it. When the communication window is closed the RDY line is released. For information on when the communications window is closed see Section 8.10.

Transfer of data between the master and slave must occur during the communications window (RDY is LOW). If the master wishes to initiate communication, a *Force Communications Request* must be made, after which the master should wait for the slave to pull RDY LOW before attempting to read or write. Section 8.13.2 describes the *Force Communications Request* sequence.

8.9 I²C Transaction Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH) and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be missed/lost. The default I²C timeout period is set to 200 ms. The I²C transaction timeout should be set between 2 ms and 230 ms. The *I²C transaction timeout* is measured from the start of the communications window (RDY goes LOW).

Once communication between the master and the IQS377 has begun (START condition on I²C lines), the I²C transaction timeout is disabled leaving the watchdog timer in control. For more information on the behaviour of the device under these conditions see Section 7.4.

8.10 Terminate Communication

A standard I²C STOP will close the current communication window.

If the *Stop Bit Disable* bit in the *System Config* register is set, the device will not respond to a standard I²C STOP. This bit takes effect immediately, meaning the communication window in which the bit is set needs to be closed with the end communications command. The communication window must be terminated using the end communications command (0xFF) shown in Figure 8.1.

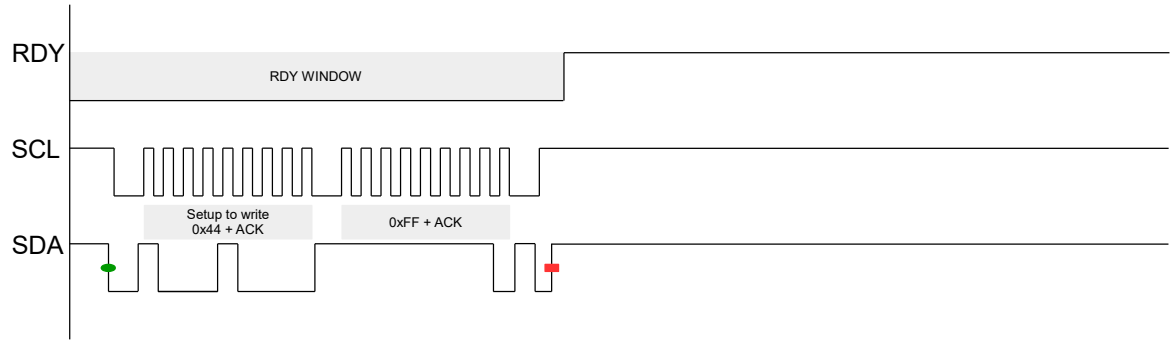


Figure 8.1: Force Stop Communication Sequence

8.11 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high).

8.12 I²C Interface

The IQS377 has 2 *Interface Types*, as described in the sections below.

8.12.1 I²C Streaming

In I²C Streaming mode data is constantly reported at the relevant power mode report rate specified in registers *0x21* (normal power report rate), *0x22* (low power report rate).

8.12.2 I²C Event Mode

In *Event Mode* the RDY line will only go LOW when one or more of the enabled events are triggered or if the device resets. This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred.

8.13 Event Mode Communication

For event mode to function correctly the following requirements must be met:

- A device reset, as indicated by the *Reset Event* flag, must be acknowledged by setting the *ACK Reset* bit. Setting the *ACK RESET* bit will clear the *RESET Event* flag in the *System Status* register.
- Enabled events must be serviced by reading from the *System Status* register (0x10) to ensure all event flags are cleared. If these flags are not cleared continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode.

8.13.1 Events

Events can be individually enabled to trigger communication. Bit definitions can be found in *System Events*.

Using the *Events Enable* register the events in *System Events*.

8.13.2 Force Communication

In streaming mode, the IQS377 I²C will provide Ready (RDY) windows at intervals specified by the relevant power mode report rate. Ideally, communication with the IQS377 should only be initiated in a RDY window. A communication request described in the figure below will force a RDY window to open. In event mode RDY windows are only provided when an event is reported. A RDY window must be requested to write or read settings outside of this provided window. The minimum and maximum time between the communication request and the opening of a RDY window (t_{wait}) is application specific. The average values of t_{wait} are 0.1 ms $\leq t_{wait} \leq$ 45 ms[i].

The communication request sequence is shown in Figure 8.2.

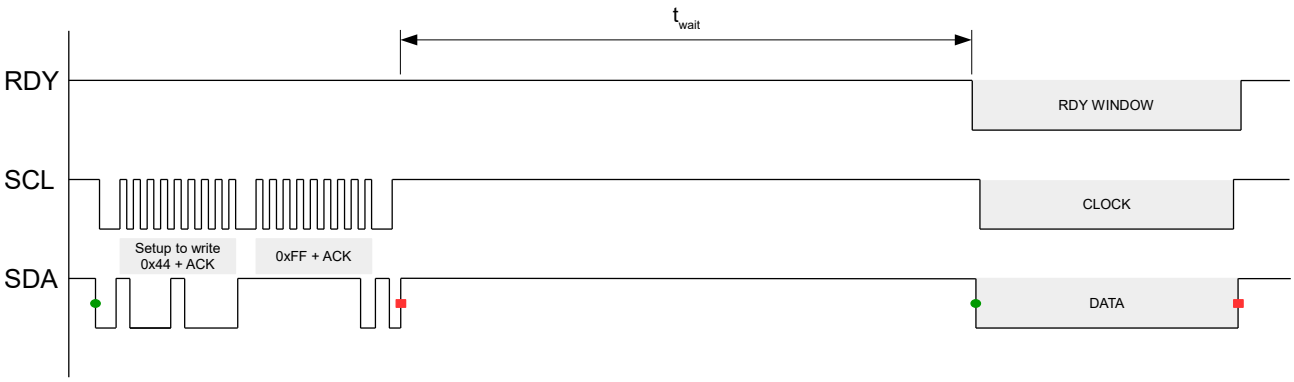


Figure 8.2: Force Communication Sequence

[i] Please contact Azoteq for an application specific value of t_{wait}

9 Memory Map Register Descriptions

Address	Data (16bit)	Notes
0x00 - 0x09	Version details	Section A.1
Read Only	**System Information**	
0x10	Systems Status	Section A.2
0x11	Events	Section A.3
0x12	Trigger Level	uint16
0x13	Trigger Movement	uint16
0x14	Trigger Delta	int16
0x15	CH0 Counts	uint16
0x16	CH1 Counts	uint16
0x17	CH0 LTA	uint16
0x18	CH1 LTA	uint16
0x19	CH0 Delta	int16
0x1A	CH1 Delta	int16
Read/Write	**System Settings**	
0x20	System Control	Section A.4
0x21	System Configuration	Section A.5
0x22	Normal Power Mode Report Rate	uint16
0x23	Low Power Mode Report Rate	uint16
0x24	Transaction Timeout	uint16
0x25	Power Mode Timeout	Section A.6
0x26	Filter Betas	Section A.7
0x27	Enabled Events	Section A.9
0x28	OutA Allocation	Section A.10
Read/Write	**Sensor 0 Setup**	
0x30	Sensor Setup	Section A.11
0x31	Input Selection 0	Section A.12
0x32	Input Selection 1	Section A.13
0x33	Conversion Frequency	Section A.14
0x34	ATI Base	uint16
0x35	ATI Base	uint16
0x36	Gain Index	Section A.15
0x37	Compensation	Section A.16
Read/Write	**Sensor 1 Setup**	
0x40	Sensor Setup	Section A.11
0x41	Input Selection 0	Section A.12
0x42	Input Selection 1	Section A.13
0x43	Conversion Frequency	Section A.14
0x44	ATI Base	uint16
0x45	ATI Target	uint16
0x46	Gain	Section A.15
0x47	Compensation	Section A.16
Read/Write	**Channel 0 Setup**	
0x50	Setup	Section A.17
0x51	Event Timeouts	Section A.18
0x52	Filter Halt Settings	Section A.19
0x53	Activation Settings	Section A.20
Read/Write	**Channel 1 Setup**	
0x60	Setup	Section A.17

0x61	Event Timeouts	Section A.18
0x62	Filter Halt Settings	Section A.19
0x63	Activation Settings	Section A.20
Read/Write	**Trigger Settings**	
0x70	Settings	Section A.21
0x71	Threshold	uint16
0x72	Hysteresis	uint16
0x73	Rapid Trigger Threshold	uint16
0x74	Total Levels	uint16
0x75	Max Delta	uint16
0x76	Zero Delta	int16

10 Ordering Information

10.1 Ordering Code

IQS377 zzz ppb

Table 10.1: Order Code Description

IC NAME			IQS377
DEFAULT CONFIGURATION	zzz	= 001	I2C Address 1 = 0x44 (0x45[i]) I2C Address 2 = 0x46 (0x47i)
PACKAGE TYPE	pp	= CS QF	WLCSP11 package QFN20 package
BULK PACKAGING	b	= R	WLCSP11 Reel (3000 pcs/reel) QFN20 Reel (2000 pcs/reel)

Example : IQS377001QFR

10.2 Top Marking

10.2.1 WLCSP11 Package Marking

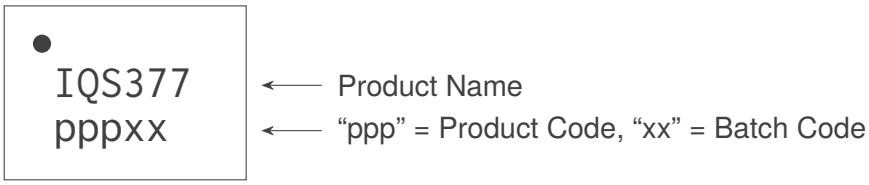


Figure 10.1: IQS377-WLCSP11 Package Top Marking

10.2.2 QFN20 Package Marking Options

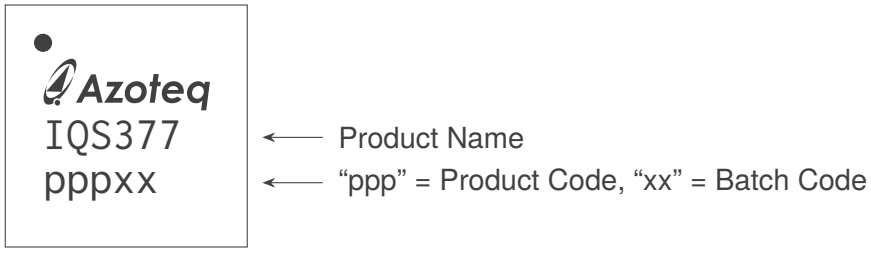


Figure 10.2: IQS377-QFN20 Package Top Marking

[i] Reserved secondary I²C address

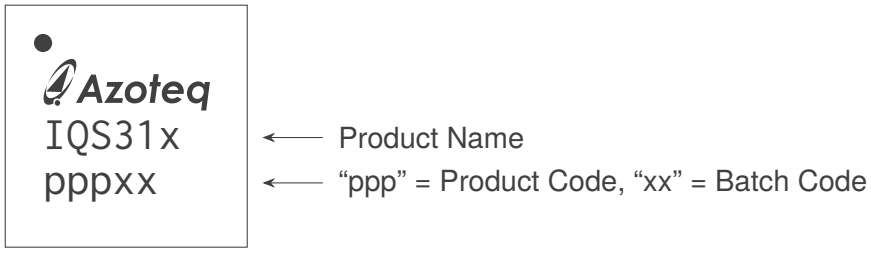


Figure 10.3: IQS31x-QFN20 Package Top Marking

11 Package Specification

11.1 Package Outline Description – WLCSP11

This package outline is specific to order codes ending in WLCSP.

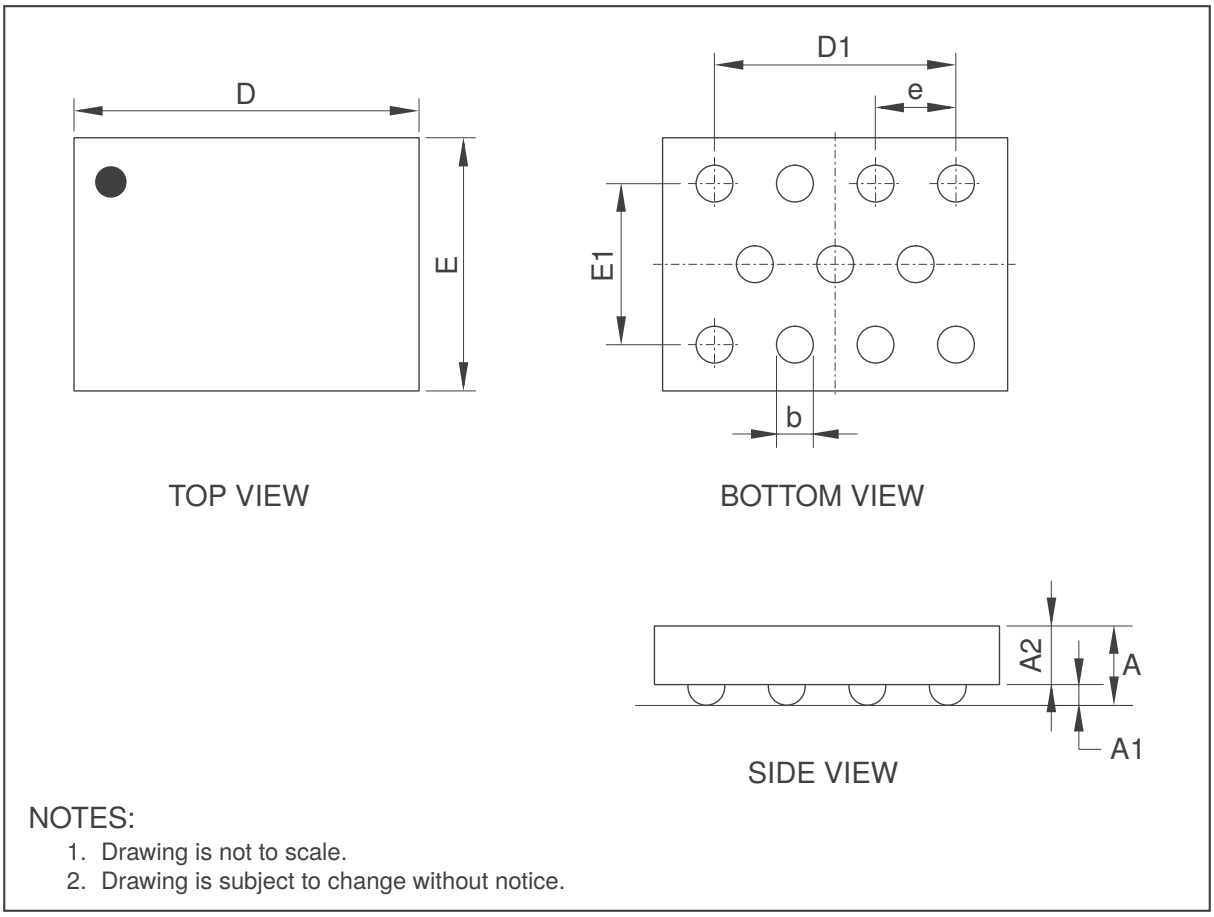
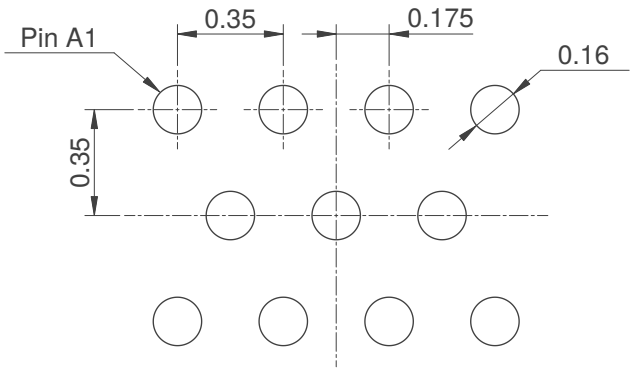


Figure 11.1: WLCSP11 (1.48x1.08) Package Outline Visual Description

Table 11.1: WLCSP11 (1.48x1.08) Package Outline Visual Description (mm)

Dimension	Min	Nom	Max
A	0.303	0.345	0.387
A1	0.076	0.090	0.104
A2	0.227	0.255	0.283
D	1.46	1.48	1.50
E	1.06	1.08	1.10
D1	1.05 BSC		
E1	0.700 BSC		
b	0.136	0.160	0.184
e	0.350 BSC		

11.2 Package Footprint Description – WLCSP11



NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 11.2: WLCSP11 Recommended Footprint

11.3 Package Outline Description – QFN20

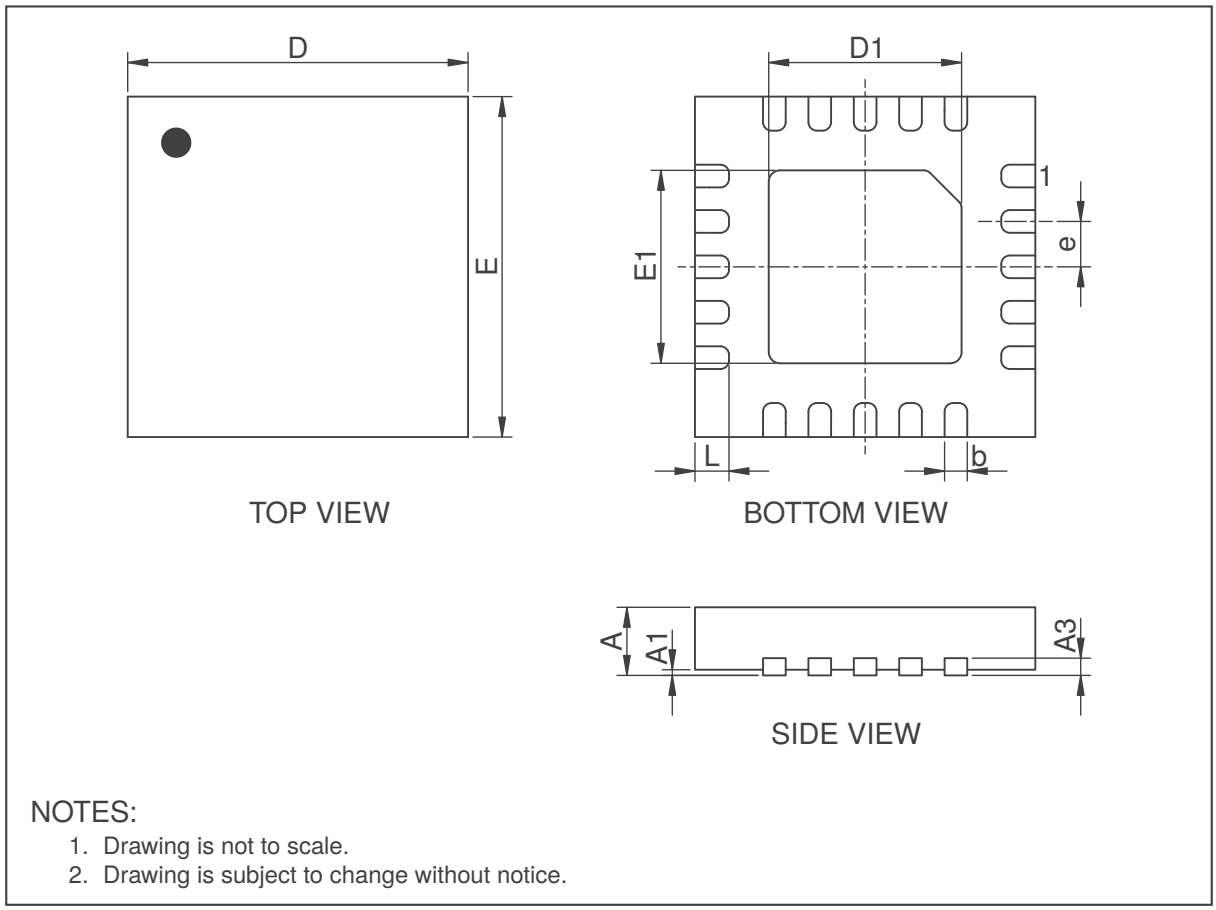
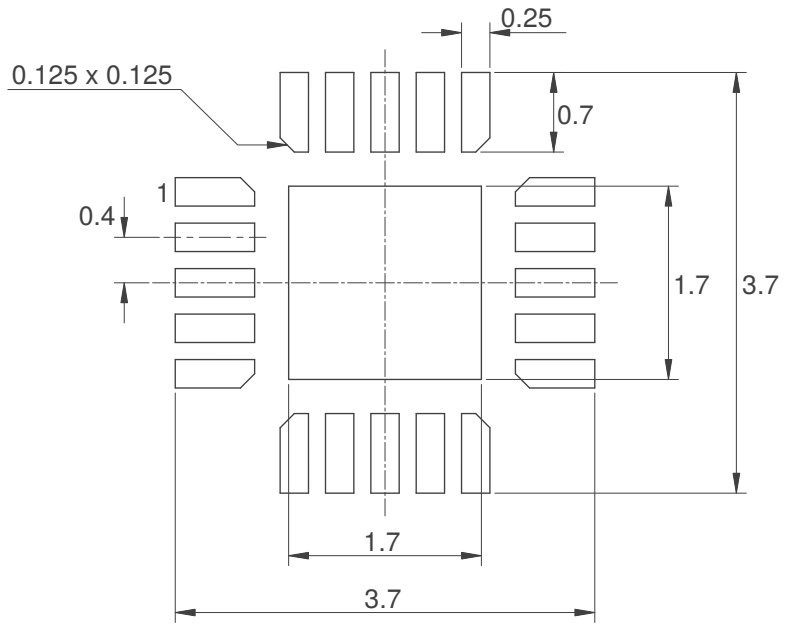


Figure 11.3: QFR (3x3)-20 Package Outline Visual Description

Table 11.2: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

11.4 Package Footprint Description – QFN20

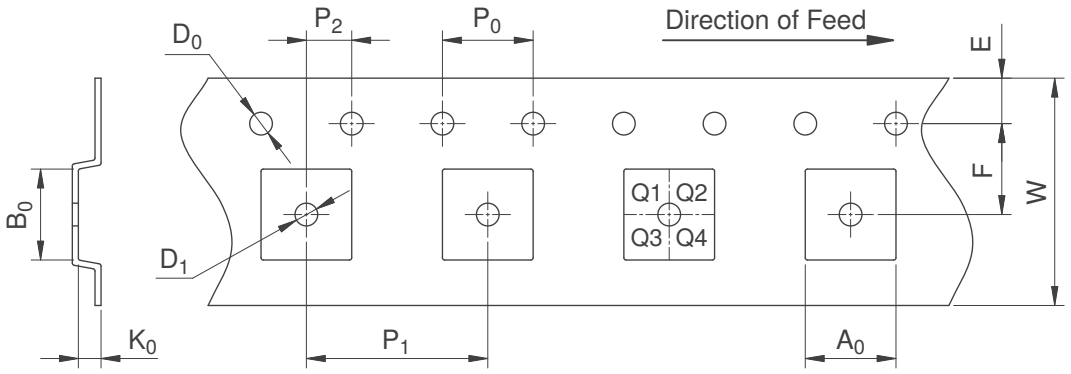


NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 11.4: QFN20 Recommended Footprint

11.5 Tape and Reel Specifications

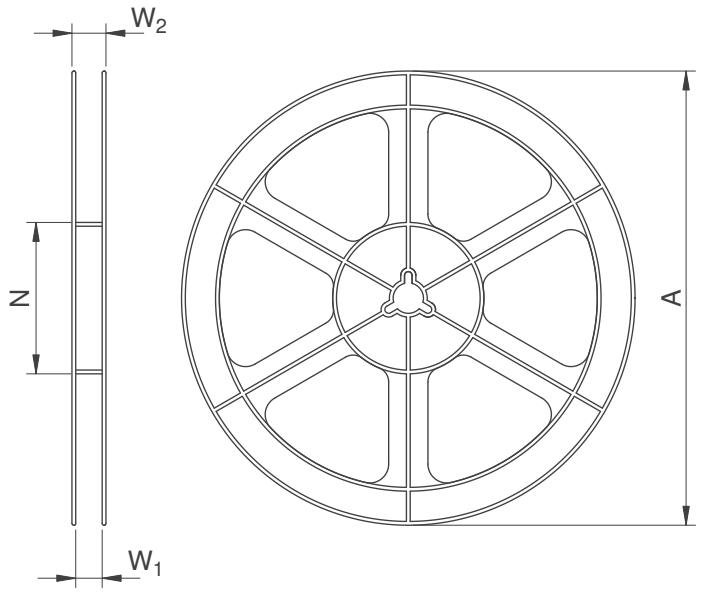


NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 11.5: Carrier Tape Specification

Table 11.3: Carrier Tape Dimensions [mm]

Dimension	Package	
	WLCSP11	QFN20
A_0	1.35	3.30
B_0	1.75	3.30
K_0	0.50	0.75
D_0	1.50	1.50
D_1	0.60	1.55
E	1.75	1.75
F	3.50	5.50
P_0	4.00	4.00
P_1	4.00	8.00
P_2	2.00	2.00
W	8.00	12.00
Pin 1 Quadrant	Q2	Q2



NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 11.6: Reel Specification

Table 11.4: Reel Dimensions [mm]

Dimension	Package	
	WLCSP11	QFN20
A	179	178
N	55	60
W_1	8.4	12.4
W_2 (Max)	14.4	18.4

A Memory Map Descriptions

A.1 Version Information (0x00 – 0x09)

Address	Category	Name	Value
0x00	Reserved	Product Number	3558
0x01		Major Version	TBC
0x02		Minor Version	TBC
0x03		Reserved	
0x04			
0x05 - 0x09			

A.2 System Flags (0x10)

Bit	15	14	13	12	11	10	9	8
Description	Reserved					Power Mode		

Bit	7	6	5	4	3	2	1	0
Description	Trigger Activation	Trigger Level	CH1 Activation	CH0 Activation	CH1 Filter-Halt	CH0 Filter-Halt	ATI Error	Show Reset

- Bit 10-8: **Current Power Mode**
  - 00: Normal Power
  - 01: Low Power
  - 10: Ultra Low Power
- Bit 7: **Trigger Active**
  - 0: Trigger is not Active
  - 1: Trigger is Active
- Bit 6: **Trigger Level**
  - 0: No Trigger level changed
  - 1: Trigger level changed
- Bit 5-2: **CHx Touch and Prox**

  For CHx Activation
  - 0: CHx not in Activation
  - 1: CHx in Activation

  For CHx Filter Halt
  - 0: CHx not in Filter Halt
  - 1: CHx in Filter Halt
- Bit 1: **ATI Error**
  - 0: No ATI Error occurred
  - 1: ATI Error occurred
- Bit 0: **Reset Event**
  - 0: No Reset Event occurred
  - 1: Reset Event occurred

A.3 Events (0x11)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Trigger	Activation	Filter Halt	Power	ATI

- Bit 4: **Trigger Event**
  - 0: No Touch Event occurred

- 1: Trigger Event occurred

- Bit 3: **Touch Event**
  - 0: No Activation Event occurred
  - 1: Activation Event occurred
- Bit 2: **Prox Event**
  - 0: No Filter Halt Event occurred
  - 1: Filter Halt Event occurred
- Bit 1: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 0: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred

A.4 System Control (0x20)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Save Zero Delta	Save Max Delta	Reseed	Re-ATI	Soft Reset	Ack Reset

- Bit 5: **Save Zero Delta**
  - 0b0: Bit cleared automatically after instruction
  - 0b1: Save Current Channel Delta as Zero for Trigger
- Bit 4: **Save Max Delta**
  - 0b0: Bit cleared automatically after instruction
  - 0b1: Save Current Channel Delta as Max for Trigger
- Bit 3: **Reseed**
  - 0b0: Bit cleared automatically after instruction
  - 0b1: Reseed all channels
- Bit 2: **Re-ATI**
  - 0b0: Bit cleared automatically after instruction
  - 0b1: Re-ATI all channels
- Bit 1: **Soft Reset**
  - 0b0: Bit cleared automatically after instruction
  - 0b1: Soft Reset
- Bit 0: **ACK Reset**
  - 0b0: Bit cleared automatically after instruction
  - 0b1: ACK Reset

A.5 System Configuration (0x21)

Bit	15	14	13	12	11	10	9	8
Description	Stop Bit Disable	S/H Bias Select		Scatter	GPIO Out	Linearise	Max Counts	

Bit	7	6	5	4	3	2	1	0
Description	Auto-Prox Allocation	I2C Mode	FOSC Select	Auto Prox Cycles		Power Mode		

- Bit 15: **Stop Bit Disable**
  - 1: I2C Stop Bit do not close RDY window.
  - 0: I2C Stop Bit closes RDY window.
- Bit 14-13: **S/H Bias Select**

- 00: 2 μA
- 01: 5 μA
- 10: 7 μA
- 11: 10 μA

- Bit 12: **Scatter Sampling**
  - 1: Scatter Sampling Enabled
  - 0: Scatter Sampling Disabled
- Bit 11: **GPIO Output Logic**
  - 1: Active High
  - 0: Active Low
- Bit 10: **Linearise Counts**
  - 1: Linearise channel counts
  - 0: Do not linearise channel Counts
- Bit 9-8: **Max Counts**
  - 0b00: 1023
  - 0b01: 2047
  - 0b10: 4095
  - 0b11: 16383
- Bit 7: **Auto-Prox Allocation**
  - 1: CH1
  - 0: CH0
- Bit 6: **I²C Mode**
  - 0: I²C Streaming
  - 1: I²C Event Mode
- Bit 5: **FOSC Select**
  - 0: FOSC = 14 MHz
  - 1: FOSC = 18 MHz
- Bit 4-3: **Auto Prox Cycles Select**
  - Number of conversions before each interrupt is generated in Auto Prox Mode
  - 0b00: 4
  - 0b01: 8
  - 0b10: 16
  - b011: 32
- Bit 2-0: **Power Mode**
  - 0b000: Automatic
  - 0b001: Normal Power Mode
  - 0b010: Low Power Mode
  - 0b100: Ultra Low Power Mode

A.6 Power Mode Timeouts (0x25)

Bit	15	14	13	12	11	10	9	8
Description	Low Power Mode Timeout							

Bit	7	6	5	4	3	2	1	0
Description	Normal Power Mode Timeout							

- Bit 15-8: **Low Power Mode Timeout**
  - Actual Timeout = Timeout * 265 ms
- Bit 7-0: **Normal Power Mode Timeout**
  - Actual Timeout = Timeout * 265 ms

A.7 Counts Filter Betas (0x26)

Bit	15	14	13	12	11	10	9	8
Description	Low Power Counts Filter							

Bit	7	6	5	4	3	2	1	0
Description	Normal Power Counts Filter							

- Bit 15-8: **Low Power Counts Filter**
  - 8-bit value
- Bit 7-0: **Normal Power Counts Filter**
  - 8-bit value

A.8 LTA Filter Betas (0x27)

Bit	15	14	13	12	11	10	9	8
Description	Low Power LTA Filter							

Bit	7	6	5	4	3	2	1	0
Description	Normal Power LTA Filter							

- Bit 15-8: **Low Power LTA Filter**
  - 8-bit value
- Bit 7-0: **Normal Power LTA Filter**
  - 8-bit value

A.9 Enabled Events (0x28)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Trigger Event	Touch Event	Prox Event	Power Event	ATI Event

- Bit 4: **Trigger Event Enabled**
  - 0: Trigger Event Disabled
  - 1: Trigger Event Enabled
- Bit 3: **Touch Event Enabled**
  - 0: Touch Event Disabled
  - 1: Touch Event Enabled
- Bit 2: **Prox Event Enabled**
  - 0: Prox Event Disabled
  - 1: Prox Event Enabled
- Bit 1: **Power Event Enabled**
  - 0: Power Event Disabled
  - 1: Power Event Enabled
- Bit 0: **ATI Event Enabled**
  - 0: ATI Event Disabled
  - 1: ATI Event Enabled

A.10 OutA Select (0x29)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Trigger Activation	Trigger Level	CH1 Touch	CH0 Touch	CH1 Prox	CH0 Prox	ATI Error	Reset

- Bit 7: **Trigger Activation Select**
  - 0: Not selected
  - 1: Trigger Activation Selected for OutA
- Bit 6: **Trigger Event Enabled**
  - 0: Not selected
  - 1: Trigger Level Selected for OutA
- Bit 5: **Touch Event Enabled**
  - 0: Not selected
  - 1: CH1 Touch Selected for OutA
- Bit 4: **Touch Event Enabled**
  - 0: Not selected
  - 1: CH0 Touch Selected for OutA
- Bit 3: **CH1 Prox Select**
  - 0: Not selected
  - 1: CH1 Prox Selected for OutA
- Bit 2: **CH0 Prox Select**
  - 0: Not selected
  - 1: CH0 Prox Selected for OutA
- Bit 1: **ATI Error**
  - 0: Not selected
  - 1: ATI Error Selected for OutA
- Bit 0: **Reset**
  - 0: Not selected
  - 1: Reset State Selected for OutA

A.11 Sensor Setup (0x30,0x40)

Bit	15	14	13	12	11	10	9	8
Description	Reserved					Deadtime Enable	ATI Mode	

Bit	7	6	5	4	3	2	1	0
Description	ATI Band	Cal-Cap			FOSC TX	Sensing Mode		

- Bit 9: **Deadtime**
  - 0: Deadtime Disable
  - 1: Deadtime Enable
- Bit 9-8: **ATI Mode**
  - 00: Disable
  - 01: Base Only
  - 10: Target Only
  - 11: Full ATI
- Bit 7: **ATI Band**
  - 0: Small ATI Band = ($\frac{1}{16}$ x ATI TARGET)
  - 1: Large ATI Band = ($\frac{1}{8}$ x ATI TARGET)
- Bit 6-4: **Cal Cap Size**
  - 000: 0pF
  - 001: 0.5pF

- 010: 1pF
- 011: 1.5pF
- 100: 2pF
- 101: 2.5pF
- 110: 3pF
- 111: 3.5pF

› Bit 3: **FOSC TX Frequency**
- 0: ATI Enable
- 1: ATI Disable

› Bit 2-0: **Sensing Mode**
- 000: Disabled
- 001: Self-Capacitance
- 010: Mutual-Capacitance
- 011: Inductive
- 100: Differential Capacitance

A.12 Input Selection 0 (0x31,0x41)

Bit	15	14	13	12	11	10	9	8
Description	0	0	Cal-Cap	0	0	CTX2	CTX1	CTX0

Bit	7	6	5	4	3	2	1	0
Description	0	0	0	0	Cal-Cap	CRX2	CRX1	CRX0

› Bit 15-8: **TX Selection**
- Bit 8: CTX0
- Bit 9: CTX1
- Bit 10: CTX2
- Bit 13: Cal-Cap

› Bit 7-0: **RX Selection**
- Bit 0: CRX0
- Bit 1: CRX1
- Bit 2: CRX2
- Bit 3: Cal-Cap

A.13 Input Selection 1 (0x32,0x42)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	0	0	Cal-Cap	0	0	CTX2	CTX1	CTX0

› Bit 7-0: **Diff TX Selection**
- Bit 0: CTX0
- Bit 1: CTX1
- Bit 2: CTX2
- Bit 5: Cal-Cap

A.14 Conversion Frequency (0x33,0x43)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	Conversion Frequency Period						

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Conversion Frequency Fraction						

- Bit 8-15: **Conversion Frequency Period**
  - The calculation of the charge transfer frequency (f_{xfer} is shown below. The relevant formula is determined by the value of the dead time enabled bit (refer to table A.11)
  - Dead time disabled: $f_{xfer} = \frac{f_clk}{2*period+2}$
  - Dead time enabled: $f_{xfer} = \frac{f_clk}{2*period+3}$
  - Range: 0 - 127
- Bit 0-7: **Conversion Frequency Fraction**
  - $256 * \frac{f_{conv}}{f_{clk}}$
  - Range: 0 - 127
- Note: if Conversion frequency fraction is fixed at 127 and dead time is enabled, the following values of the conversion period will result in the corresponding charge transfer frequencies:
  - 1: 3MHz
  - 7: 1MHz[i]
  - 16: 500kHz
  - 24: 350kHz
  - 34: 250kHz
  - 58: 150kHz

A.15 Gain Index (0x36,0x46)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Gain Index						

- Bit 6-0: **Gain Index**
  - 7-bit value

A.16 Compensation (0x37,0x47)

Bit	15	14	13	12	11	10	9	8
Description	Compensation Divider					Reserved	Compensation	

Bit	7	6	5	4	3	2	1	0
Description	Compensation							

- Bit 15-11: **Compensation Divider**
  - 5-bit value
- Bit 9-0: **Compensation Value**
  - 10-bit value

[i] Please note: The maximum charge transfer frequency for mutual capacitive mode (refer to table A.11) is 1MHz

A.17 Channel Setup (0x50,0x60)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Dual	Inverse

- Bit 1: **Dual Direction**
  - 0: Do not Trigger on Both Direction
  - 1: Trigger in Both Directions
- Bit 0: **Inverse Direction**
  - 0: Trigger in Default Direction
  - 1: Trigger in Inverse Direction

A.18 Event Timeouts (0x51,0x61)

Bit	15	14	13	12	11	10	9	8
Description	Activation Timeout							

Bit	7	6	5	4	3	2	1	0
Description	Filter Halt Timeout							

- Bit 15-8: **Filter Halt Timeout**
  - Range: 0 - 255
  - 255ms * value
- Bit 7-0: **Filter Halt Timeout**
  - Range: 0 - 255
  - 255ms * value

A.19 Filter Halt Settings (0x52,0x62)

Bit	15	14	13	12	11	10	9	8
Description	Exit				Enter			

Bit	7	6	5	4	3	2	1	0
Description	Threshold							

- Bit 15-12: **Filter Halt Debounce Exit**
  - 0000: Filter Halt Debounce Exit disabled
  - Number of debounce conversions on Filter Halt Exit (4-bit value)
- Bit 11-8: **Filter Halt Debounce Enter**
  - 0000: Filter Halt Debounce Enter disabled
  - Number of debounce conversions on Filter Halt Enter (4-bit value)
- Bit 7-0: **Filter Halt Threshold**
  - 8 bit value

A.20 Activation Settings (0x53,0x63)

Bit	15	14	13	12	11	10	9	8
Description	Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Threshold							

- Bit 15-8: **Touch Hysteresis**
  - $Touch\ Hysteresis = \frac{Touch\ Hysteresis}{256} \times Touch\ Threshold$
- Bit 7-0: **Touch Threshold**
  - $Touch\ Threshold = \frac{Threshold \times LTA}{256}$

A.21 Trigger Settings (0x70)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reserved				Trigger CH Allocation		Enable Rapid Trigger	Enable

- Bit 3-2: **Trigger Channel Allocation**
  - Channel Allocated As Trigger
  - 0b00: None
  - 0b01: CH0
  - 0b10: CH1
  - 0b11: Both
- Bit 1: **Enable Rapid Trigger**
  - 0b0: Rapid Trigger Disabled
  - 0b1: Rapid Trigger Enabled
- Bit 0: **Enable**
  - 0: Disable Trigger UI
  - 1: Enable Trigger UI

A.22 Trigger Threshold (0x71)

Bit	15	14	13	12	11	10	9	8
Description	Trigger Threshold							

Bit	7	6	5	4	3	2	1	0
Description	Trigger Threshold							

- Bit 15-0: **Trigger Threshold (trip level)**
  - 16 bit value
  - Range: 0 - Trigger Levels
  - Unit: levels
  - Trigger Activation occurs when Trigger Level > Trigger Threshold

A.23 Trigger Hysteresis (0x72)

Bit	15	14	13	12	11	10	9	8
Description	Trigger Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Trigger Hysteresis							

- Bit 15-0: **Trigger Hysteresis (amount of levels)**
  - Trigger Deactivation Level = Trigger Threshold - Trigger Hysteresis
  - Applicable when Rapid Trigger is disabled.

A.24 Rapid Trigger Threshold (0x73)

Bit	15	14	13	12	11	10	9	8
Description	Rapid Trigger Threshold							

Bit	7	6	5	4	3	2	1	0
Description	Rapid Trigger Threshold							

- Bit 15-0: **Rapid Trigger Threshold (level change)**
  - 16 bit value
  - Range: <Trigger Levels
  - Unit: levels
  - Trigger Activation occurs when Trigger Movement > Rapid Trigger Threshold
  - Trigger Deactivation occurs when Trigger Movement < (-1) * (Rapid Trigger Threshold)

A.25 Trigger Levels (0x74)

Bit	15	14	13	12	11	10	9	8
Description	Trigger Levels							

Bit	7	6	5	4	3	2	1	0
Description	Trigger Levels							

- Bit 15-0: **Trigger Levels**
  - 16 bit value
  - Division of (Max Delta - Zero Delta) range into discrete amount of desired trigger levels

A.26 Trigger Max Delta (0x75)

Bit	15	14	13	12	11	10	9	8
Description	Trigger Max Delta							

Bit	7	6	5	4	3	2	1	0
Description	Trigger Max Delta							

- Bit 15-0: **Trigger Max Delta**
  - 16 bit value
  - Maximum Channel Delta amount considered as final/full travel position

A.27 Trigger Zero Delta (0x76)

Bit	15	14	13	12	11	10	9	8
Description	Trigger Zero Delta							

Bit	7	6	5	4	3	2	1	0
Description	Trigger Zero Delta							

- Bit 15-0: **Trigger Zero Delta**
  - 16 bit value
  - Minimum Channel Delta amount considered as start/zero travel position

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