



## IQS320 DATASHEET

2 Channel Proximity Sensing / Single Channel Proximity Sensing with Reference Tracking Controller including Movement and SNR Boost User Interfaces. The device is specifically designed for SAR and other similar high performance proximity sensing requirements. The device features an I<sup>2</sup>C communications interface and the option to run the device in a standalone mode.

### 1 Device Overview

The IQS320 ProxFusion® IC is a self-capacitive sensing device optimised to work in SAR and similar applications that require the detection of very small capacitive changes in a high capacitive load environment. The sensor is fully I<sup>2</sup>C compatible with the ability to operate in a standalone mode. On-chip calculations allow the device to process small movements, and detect the smallest possible changes in capacitance. It is recommended to use the *SNR Boost UI* in conjunction with the *Reference UI* in applications with sensitive or critical proximity triggers and high capacitance load environments.

#### 1.1 Main Features

- > Dual channel self-capacitance Sensor
- > 2 External sensor pad connections
- > External sensor options:
  - 2 self-capacitance sensors
  - 1 self-capacitance sensor with a reference tracking sensor
- > Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Debounce & Hysteresis
  - High performance in high capacitive load conditions
- > Built-in Signal processing options:
  - Touch/Proximity output
  - Movement User Interface
  - Reference User Interface
  - Signal to Noise Ratio Boost User Interface by means of over-sampling (add Reference UI for optimal performance)
- > Design simplicity
  - PC Software for debugging & optimal setup for performance
- > I<sup>2</sup>C communication interface with IRQ/RDY(up to fast plus -1 MHz)
- > Event and streaming modes with I<sup>2</sup>C
- > Selectable I<sup>2</sup>C address
- > Standalone output mode
- > Supply Voltage 1.71 V to 3.5 V
- > Package options
  - WLCSP11 (1.48 x 1.08 x 0.345 mm) - interleaved 0.35 mm x 0.35 mm ball pitch
  - DFN12 (3 x 3 x 0.75 mm) - 0.5 mm pitch
  - QFN20 (3 x 3 x 0.55 mm) - 0.4 mm pitch



WLCSP11 Package



DFN12 Package



QFN20 Package

#### 1.2 Applications

- > SAR Safety Sensor
- > Keyboard back-lighting
- > Wireless charger wake-up



### 1.3 Block Diagram

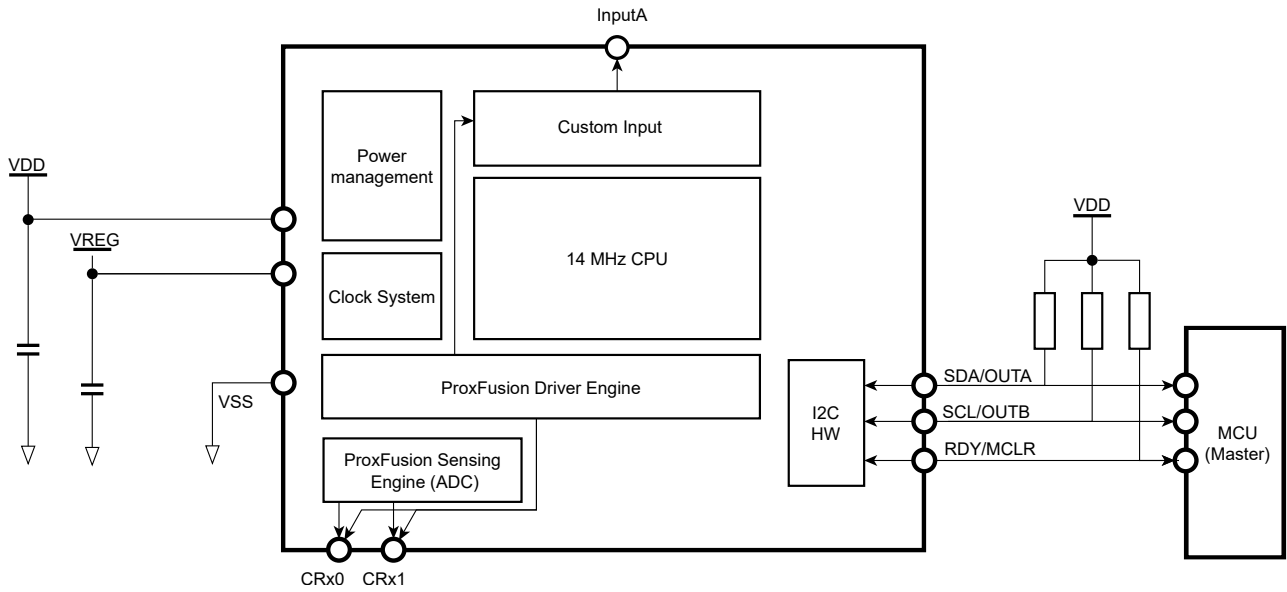


Figure 1.4: Functional Block Diagram



## Contents

|          |   |           |
|----------|---|-----------|
| <b>1</b> | <b>Device Overview</b>                            | <b>1</b>  |
| 1.1      | Main Features . . . . .                           | 1         |
| 1.2      | Applications . . . . .                            | 1         |
| 1.3      | Block Diagram . . . . .                           | 2         |
| <b>2</b> | <b>Hardware Connection</b>                        | <b>6</b>  |
| 2.1      | WLCSP11 Pin Diagram . . . . .                     | 6         |
| 2.2      | DFN12 Pin Diagram . . . . .                       | 6         |
| 2.3      | QFN20 Pin Diagram . . . . .                       | 7         |
| 2.4      | Signal Descriptions . . . . .                     | 7         |
| 2.5      | Reference Schematic . . . . .                     | 8         |
| <b>3</b> | <b>Electrical Characteristics</b>                 | <b>11</b> |
| 3.1      | Absolute Maximum Ratings . . . . .                | 11        |
| 3.2      | Recommended Operating Conditions . . . . .        | 11        |
| 3.3      | ESD Rating . . . . .                              | 11        |
| 3.4      | Current Consumption . . . . .                     | 12        |
| <b>4</b> | <b>Noise Performance</b>                          | <b>13</b> |
| <b>5</b> | <b>Timing and Switching Characteristics</b>       | <b>14</b> |
| 5.1      | Reset Levels . . . . .                            | 14        |
| 5.2      | MCLR Pin Levels and Characteristics . . . . .     | 14        |
| 5.3      | Miscellaneous Timings . . . . .                   | 14        |
| 5.4      | Digital I/O Characteristics . . . . .             | 15        |
| 5.5      | I <sup>2</sup> C Characteristics . . . . .        | 15        |
| <b>6</b> | <b>ProxFusion<sup>®</sup> Module</b>              | <b>16</b> |
| 6.1      | Channel Options . . . . .                         | 16        |
| 6.2      | Count Value . . . . .                             | 16        |
| 6.2.1    | Max Counts . . . . .                              | 16        |
| 6.2.2    | Linearise Counts . . . . .                        | 16        |
| 6.3      | Reference Value/Long-Term Average (LTA) . . . . . | 16        |
| 6.3.1    | Reseed . . . . .                                  | 17        |
| 6.4      | Prox and Touch Thresholds . . . . .               | 17        |
| 6.5      | Event Timeout . . . . .                           | 18        |
| 6.6      | Filter Betas . . . . .                            | 18        |
| 6.7      | Automatic Tuning Implementation (ATI) . . . . .   | 18        |
| 6.8      | Automatic Re-ATI . . . . .                        | 19        |
| 6.8.1    | Description . . . . .                             | 19        |
| 6.8.2    | Conditions for Re-ATI to Activate . . . . .       | 19        |
| 6.8.3    | ATI Error . . . . .                               | 20        |
| <b>7</b> | <b>Hardware Settings</b>                          | <b>21</b> |
| 7.1      | Charge Transfer Frequency . . . . .               | 21        |
| 7.2      | Reset . . . . .                                   | 21        |
| 7.2.1    | Reset Indication . . . . .                        | 21        |
| 7.2.2    | Software Reset . . . . .                          | 21        |
| 7.2.3    | Hardware Reset . . . . .                          | 21        |



|           |   |           |
|-----------|---|-----------|
| <b>8</b>  | <b>Additional Features</b>              | <b>22</b> |
| 8.1       | Reference UI                            | 22        |
| 8.2       | Movement UI                             | 22        |
| 8.2.1     | Movement Threshold                      | 23        |
| 8.3       | SNR Boost UI                            | 23        |
| 8.4       | Standalone Mode                         | 23        |
| 8.4.1     | ATI Indication                          | 24        |
| 8.5       | Watchdog Timer                          | 25        |
| <b>9</b>  | <b>I<sup>2</sup>C Interface</b>         | <b>26</b> |
| 9.1       | I <sup>2</sup> C Module Specification   | 26        |
| 9.2       | I <sup>2</sup> C Address                | 26        |
| 9.3       | I <sup>3</sup> C Compatibility          | 26        |
| 9.4       | Memory Map Addressing and Data          | 26        |
| 9.5       | Ready (RDY) Indicator                   | 26        |
| 9.6       | Communications Window                   | 27        |
| 9.7       | I <sup>2</sup> C Transaction Timeout    | 27        |
| 9.8       | Terminate Communication                 | 27        |
| 9.9       | Invalid Communications Return           | 27        |
| 9.10      | I <sup>2</sup> C Interface              | 28        |
| 9.10.1    | I <sup>2</sup> C Streaming              | 28        |
| 9.10.2    | I <sup>2</sup> C Event Mode             | 28        |
| 9.11      | Event Mode Communication                | 28        |
| 9.11.1    | Events                                  | 28        |
| 9.11.2    | Force Communication                     | 28        |
| 9.12      | Read/Write Check Disable                | 29        |
| 9.12.1    | Program Flow Diagram                    | 30        |
| <b>10</b> | <b>Memory Map Register Descriptions</b> | <b>31</b> |
| <b>11</b> | <b>Ordering Information</b>             | <b>33</b> |
| 11.1      | Ordering Code                           | 33        |
| 11.2      | Top Marking                             | 33        |
| 11.2.1    | WLCSP11 Package Marking                 | 33        |
| 11.2.2    | DFN12 Package Marking Options           | 33        |
| 11.2.3    | QFN20 Package Marking Options           | 34        |
| <b>12</b> | <b>Package Specification</b>            | <b>35</b> |
| 12.1      | Package Outline Description – WLCSP11   | 35        |
| 12.2      | Package Footprint Description – WLCSP11 | 36        |
| 12.3      | Package Outline Description – DFN12     | 37        |
| 12.4      | Package Footprint Description – DFN12   | 38        |
| 12.5      | Package Outline Description – QFN20     | 39        |
| 12.6      | Package Footprint Description – QFN20   | 40        |
| 12.7      | Tape and Reel Specifications            | 41        |
| <b>A</b>  | <b>Memory Map Descriptions</b>          | <b>43</b> |
| A.1       | Version Information (0x00 – 0x09)       | 43        |
| A.2       | System Status (0x10)                    | 43        |
| A.3       | Sensor Setup 0 (0x20, 0x30)             | 44        |
| A.4       | Conversion Frequency Setup (0x21, 0x31) | 44        |
| A.5       | Prox Control (0x22, 0x32)               | 45        |

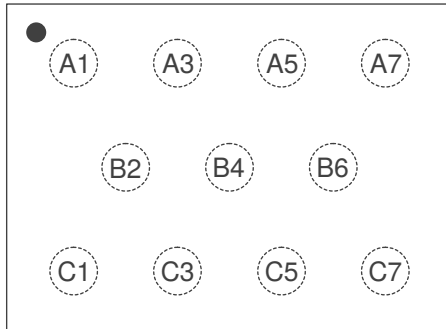


|          |   |           |
|----------|---|-----------|
| A.6      | Timing Generator Control & Prox Input (0x23, 0x33)          | 45        |
| A.7      | Inactive Rxs & Calibration Capacitor Selection (0x24, 0x34) | 46        |
| A.8      | ATI Setup (0x25, 0x35)                                      | 46        |
| A.9      | ATI Multipliers and Dividers (0x27, 0x37)                   | 46        |
| A.10     | Compensation (0x28, 0x38)                                   | 47        |
| A.11     | Prox Settings (0x40, 0x50)                                  | 47        |
| A.12     | Touch Settings (0x41, 0x51)                                 | 47        |
| A.13     | Movement Settings (0x42, 0x52)                              | 48        |
| A.14     | Counts Filter Beta & LTA Filter Beta (0x60)                 | 48        |
| A.15     | LTA Fast Filter Beta & Movement Beta (0x61)                 | 48        |
| A.16     | System Control (0x70)                                       | 48        |
| A.17     | Event Timeouts (0x73)                                       | 49        |
| A.18     | Events Enable & SNR Boost Factor (0x74)                     | 49        |
| A.19     | Reference Scaling (0x75)                                    | 50        |
| A.20     | I <sup>2</sup> C Settings (0x80)                            | 50        |
| <b>B</b> | <b>Revision History</b>                                     | <b>51</b> |
| <b>C</b> | <b>Known Issues</b>   | <b>52</b> |



## 2 Hardware Connection

### 2.1 WLCSP11 Pin Diagram

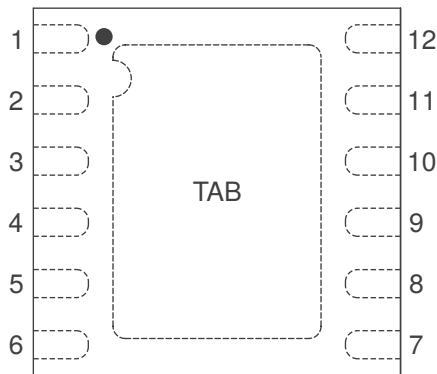


Top View

Table 2.1: 11-pin WLCSP Package

| Pin no. | Signal    |
|---------|-----------|
| A1      | CRx1/CTx1 |
| A3      | VREG      |
| A5      | SDA/OutA  |
| A7      | VSS       |
| B2      | CRx0/CTx0 |
| B4      | Unused    |
| B6      | InputA    |
| C1      | Unused    |
| C3      | SCL/OutB  |
| C5      | VDD       |
| C7      | RDY/MCLR  |

### 2.2 DFN12 Pin Diagram



Top View

Table 2.2: 12-pin DFN Package

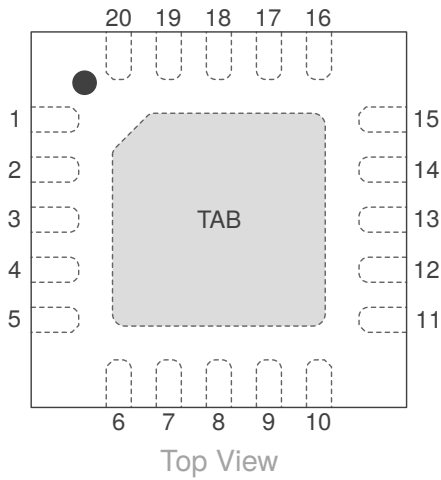
| Pin no. | Signal    |
|---------|-----------|
| 1       | InputA    |
| 2       | SDA/OutA  |
| 3       | VDD       |
| 4       | VREG      |
| 5       | SCL/OutB  |
| 6       | Unused    |
| 7       | CRx0/CTx0 |
| 8       | NC        |
| 9       | CRx1/CTx1 |
| 10      | Unused    |
| 11      | RDY/MCLR  |
| 12      | VSS       |

| Area name | Signal                 |
|-----------|------------------------|
| TAB       | Thermal pad (floating) |



## 2.3 QFN20 Pin Diagram

Table 2.3: 20-pin QFN Package (Top View)



| Pin no. | Signal    | Pin no. | Signal   |
|---------|-----------|---------|----------|
| 1       | Unused    | 11      | NC       |
| 2       | CRx0/CTx0 | 12      | NC       |
| 3       | CRx1/CTx1 | 13      | NC       |
| 4       | NC        | 14      | NC       |
| 5       | NC        | 15      | NC       |
| 6       | VREG      | 16      | NC       |
| 7       | Unused    | 17      | RDY/MCLR |
| 8       | VDD       | 18      | InputA   |
| 9       | VSS       | 19      | SDA/OutA |
| 10      | NC        | 20      | SCL/OutB |

| Area name        | Signal                 |
|------------------|------------------------|
| TAB <sup>i</sup> | Thermal pad (floating) |

## 2.4 Signal Descriptions

Table 2.4: Signal Descriptions

| Function                      | Signal Name | Signal Type | Pin Type <sup>ii</sup> | Description   |
|-------------------------------|-------------|-------------|------------------------|---|
| ProxFusion®                   | CRx0/CTx0   | Analog      | IO                     | ProxFusion® channel   |
|                               | CRx1/CTx1   | Analog      | IO                     |   |
|                               | Unused      | -           | IO                     |   |
|                               | InputA      | Digital     | O                      | InputA pad  |
|                               | Unused      | -           | O                      | Unused pad  |
| GPIO                          | RDY/MCLR    | Digital     | IO                     | Active pull-up, 200k resistor to VDD.<br>Pulled low during POR, and MCLR function enabled by default. VPP input for OTP |
| Digital Out/ I <sup>2</sup> C | SDA/OutA    | Digital     | IO                     | Digital Output / I <sup>2</sup> C Data (Debugging)  |
|                               | SCL/OutB    | Digital     | IO                     | Digital Output / I <sup>2</sup> C Clock (Debugging)   |
| Power                         | VDD         | Power       | P                      | Power supply input voltage  |
|                               | VREG        | Power       | P                      | Internal regulated supply output  |
|                               | VSS         | Power       | P                      | Analog/Digital Ground   |

<sup>i</sup> It is recommended to connect the thermal pad (TAB) to VSS.

<sup>ii</sup> Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power



## 2.5 Reference Schematic

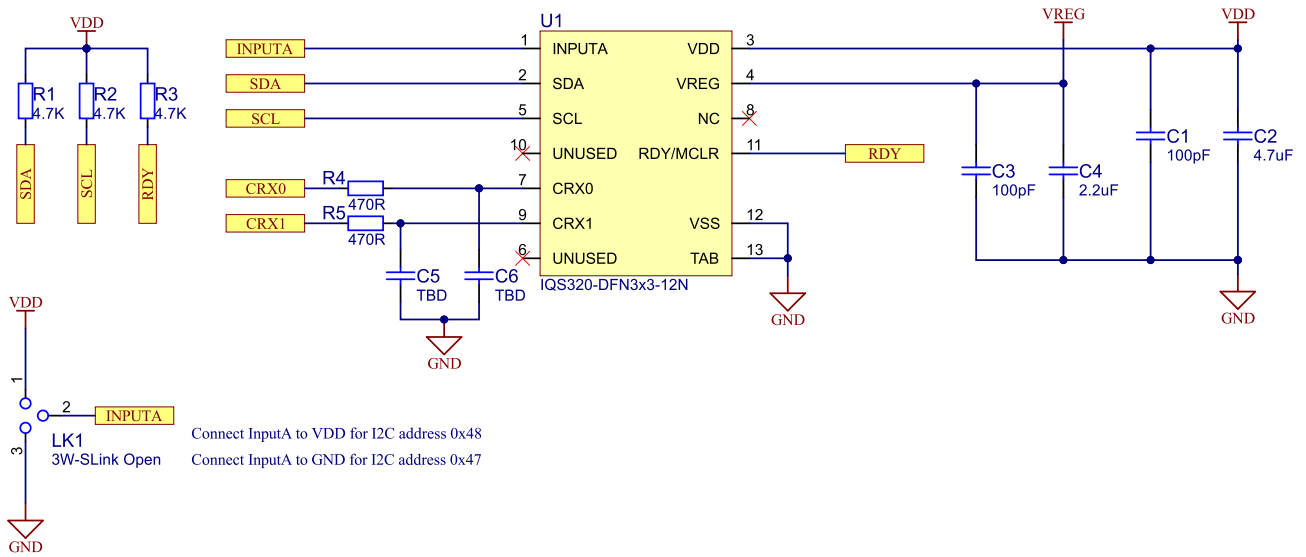


Figure 2.1: DFN12 I<sup>2</sup>C Reference Schematic

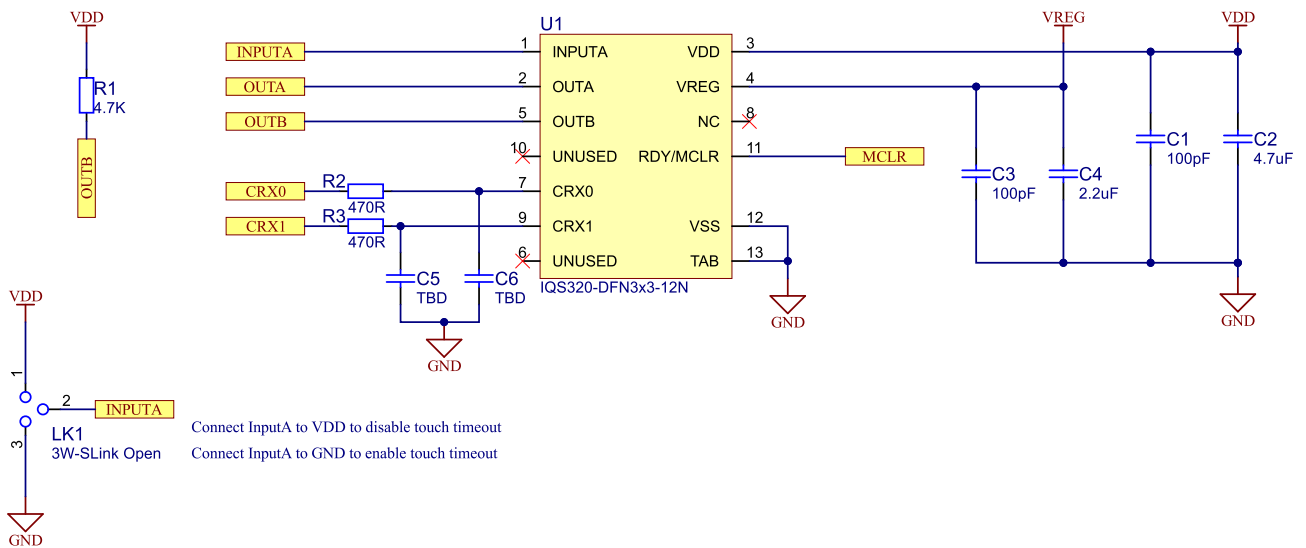


Figure 2.2: DFN12 Standalone Reference Schematic

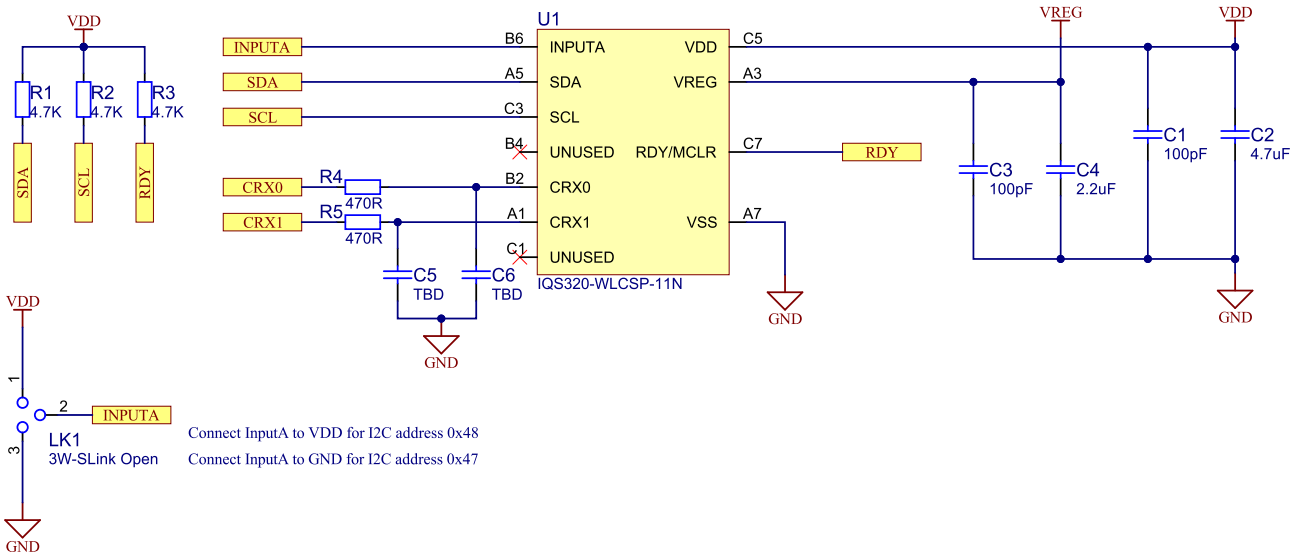


Figure 2.3: WLCSP11 I<sup>2</sup>C Reference Schematic

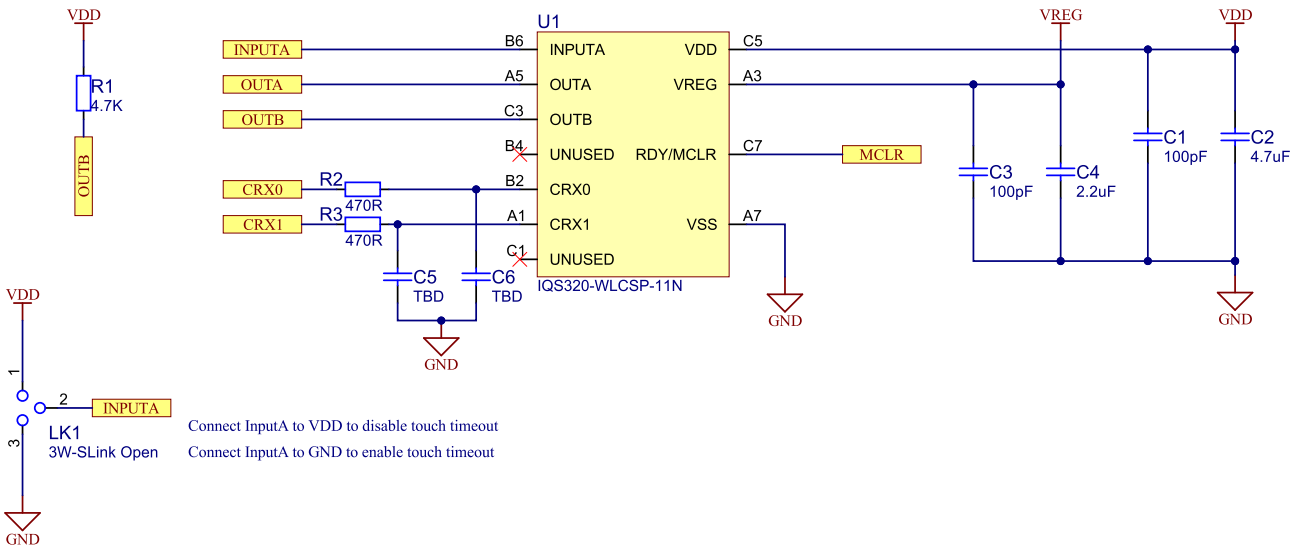


Figure 2.4: WLCSP11 Standalone Reference Schematic

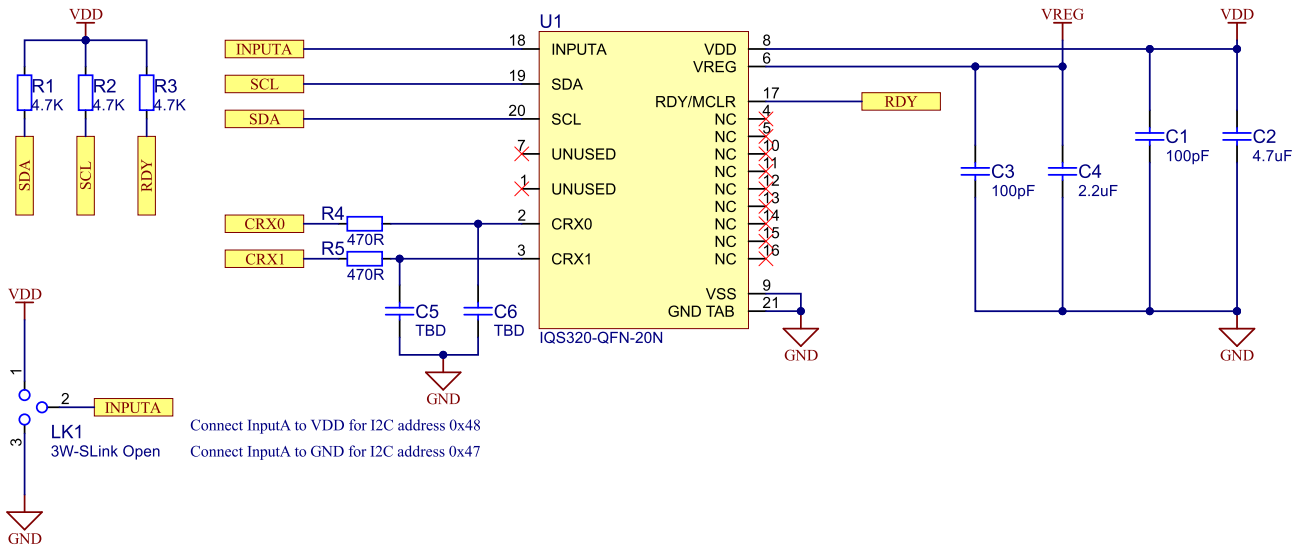


Figure 2.5: QFN20 I<sup>2</sup>C Reference Schematic

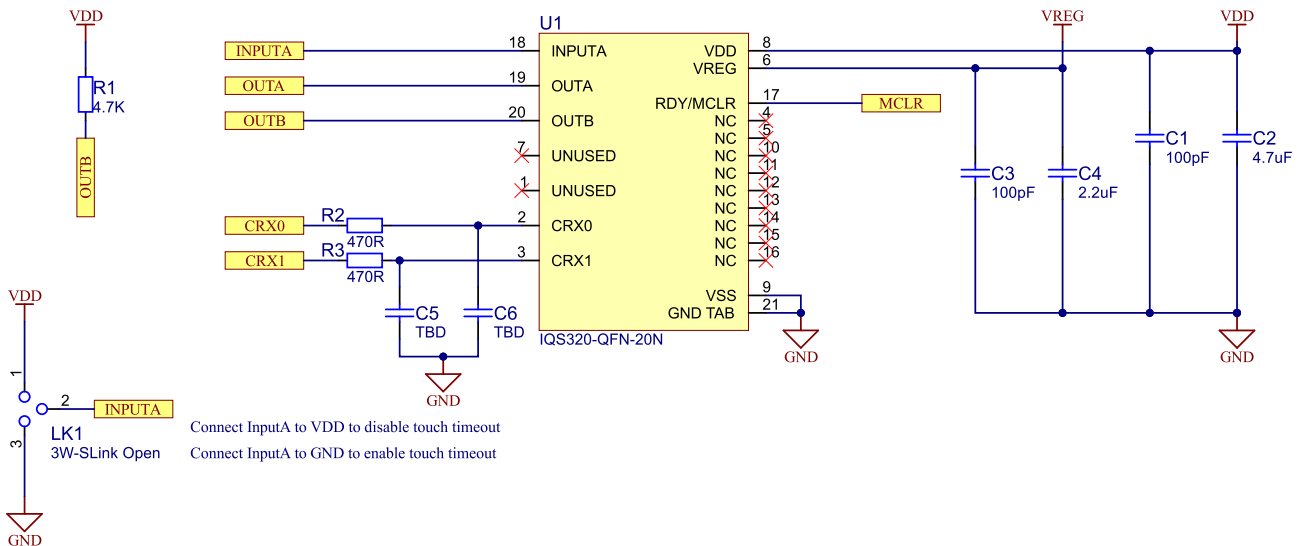


Figure 2.6: QFN20 Standalone Reference Schematic

<sup>i</sup> The TBD capacitors are used to balance the loads on CRx0/CTx0 and CRx1/CTx1. Please refer to Section 8.1 for more information.



### 3 Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

|  | Min  | Max                      | Unit |
|--|------|--------------------------|------|
| Voltage applied at VDD pin to VSS                    | 1.71 | 3.6                      | V    |
| Voltage applied to any ProxFusion® pin               | -0.3 | VREG                     | V    |
| Voltage applied to any other pin (referenced to VSS) | -0.3 | VDD + 0.3<br>(3.6 V max) | V    |
| Storage temperature, T <sub>stg</sub>                | -40  | 85                       | °C   |

#### 3.2 Recommended Operating Conditions

| Recommended operating conditions |  | Min                 | Nom                 | Max               | Unit |
|----------------------------------|--|---------------------|---------------------|-------------------|------|
| VDD                              | Supply voltage applied at VDD pin  | 1.71                |                     | 3.6               | V    |
| VREG                             | Internal regulated supply output for analog domain                                 |                     | 1.53                |                   | V    |
| VSS                              | Supply voltage applied at VSS pin  | 0                   | 0                   | 0                 | V    |
| T <sub>A</sub>                   | Operating free-air temperature   | -40                 | 25                  | 85                | °C   |
| C <sub>VDD</sub>                 | Recommended capacitor at VDD   | 2×C <sub>VREG</sub> | 3×C <sub>VREG</sub> |                   | μF   |
| C <sub>VREG</sub>                | Recommended external buffer capacitor at VREG, ESR ≤ 200 mΩ                        | 2 <sup>i</sup>      | 4.7                 | 13                | μF   |
| C <sub>XSELF-VSS</sub>           | Maximum capacitance between ground and external electrodes (self-capacitance mode) |                     |                     | 400 <sup>ii</sup> | pF   |
| RC <sub>XSELF</sub>              | Series (in-line) resistance of all self-capacitance pins in self-capacitance mode  | 0 <sup>iii</sup>    | 0.47                | 10 <sup>iv</sup>  | kΩ   |

#### 3.3 ESD Rating

|  | Value   | Unit        |
|--|---|-------------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>v</sup> | ± 2000<br>V |

<sup>i</sup> Absolute minimum allowed capacitance value is 1 μF, after taking derating, temperature, and worst-case tolerance into account. Please refer to the [AZD004](#) application note for more information regarding capacitor derating.

<sup>ii</sup> RC<sub>x</sub> = 0 Ω.

<sup>iii</sup> Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

<sup>iv</sup> Series resistance limit is a function of  $f_{xfer}$  and the circuit time constant, RC.  $R_{max} \times C_{max} = \frac{1}{(6 \times f_{xfer})}$  where C is the pin capacitance to VSS.

<sup>v</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.



### 3.4 Current Consumption

**Sensor Setup:** Channels = 2  
ATI Base = 80  
ATI Target = 2600  
 $F_{xfer} = 875 \text{ kHz}^i$

**Interface Selection:** Event mode

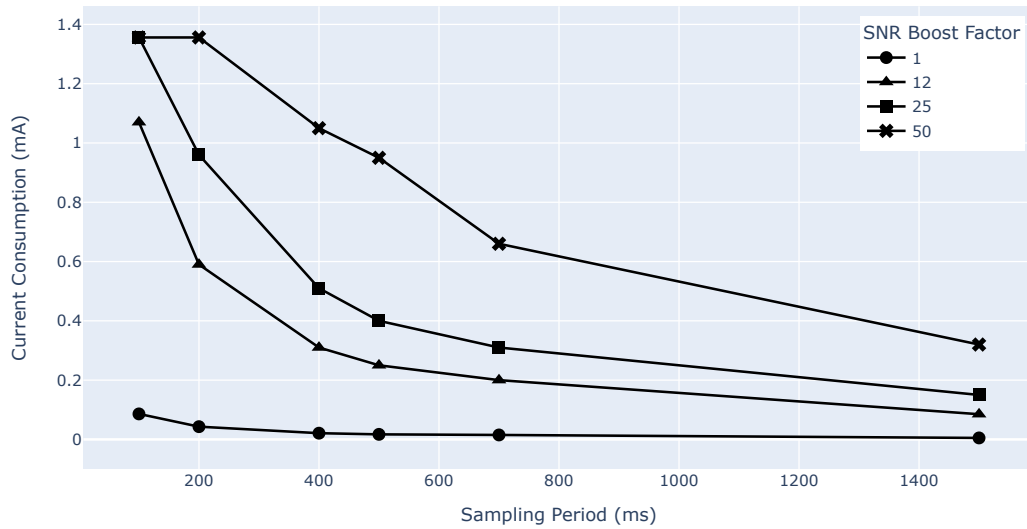


Figure 3.1: Sampling Period vs Current Consumption at different SNR Boost Factors

<sup>i</sup> The sampling period and current consumption will increase and decrease according to  $F_{xfer}$



## 4 Noise Performance

**Sensor Setup:** Reference tracking = enabled  
ATI Base = 80  
ATI Target = 2600  
 $F_{xfer} = 875$  kHz  
Signal = 25 fF

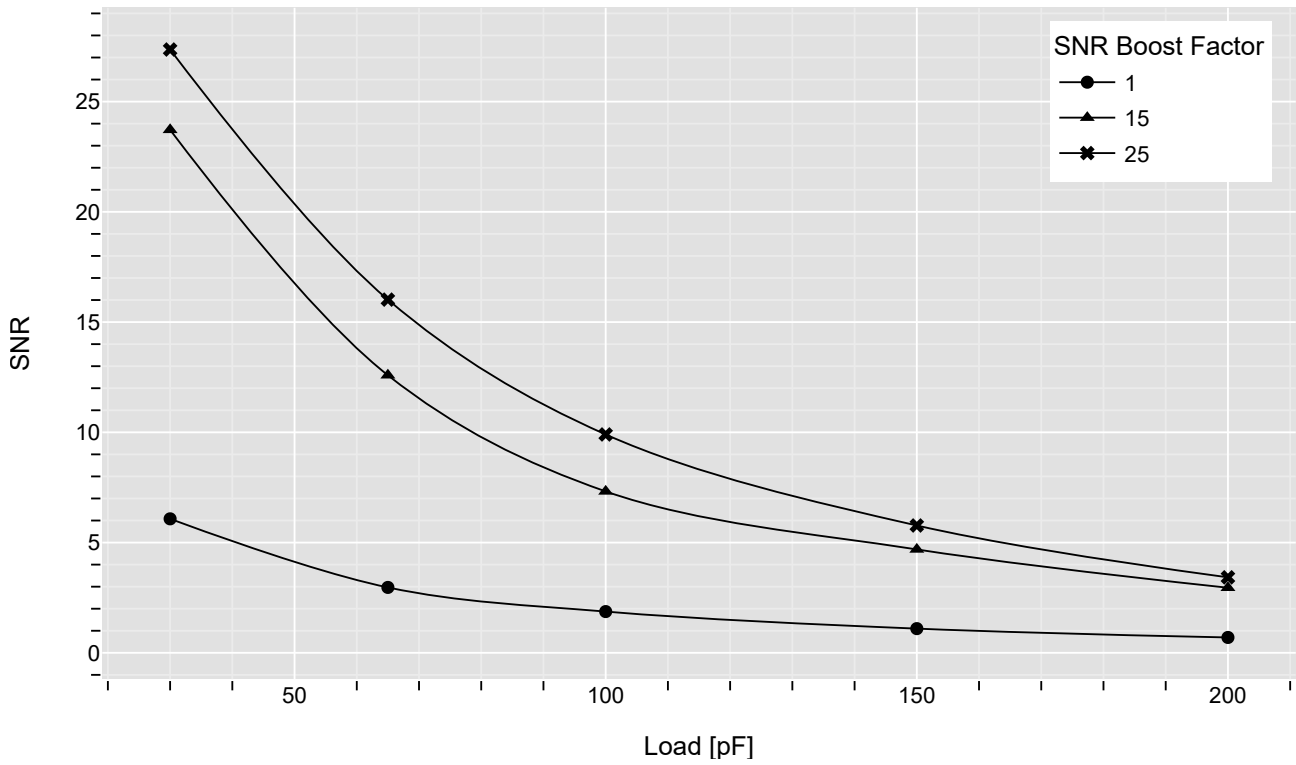


Figure 4.1: SNR vs Load Capacitance at various SNR Boost Factors and different Beta coefficients for a 25 fF signal<sup>i</sup>

<sup>i</sup> Using High SNR Boost Factors will cause a decrease in the dynamic resolution of the signal.

## 5 Timing and Switching Characteristics

### 5.1 Reset Levels

Table 5.1: Reset Levels

| Parameter        |   | Min | Max  | Unit |
|------------------|---|-----|------|------|
| V <sub>VDD</sub> | Power-up (Reset trigger) – slope > 100 V/s    |     | 1.65 | V    |
|                  | Power-down (Reset trigger) – slope < -100 V/s | 0.9 |      |      |

### 5.2 MCLR Pin Levels and Characteristics

Table 5.2: MCLR Pin Characteristics

| Parameter                |   | Conditions  | Min       | Typ | Max       | Unit |
|--------------------------|---|-------------|-----------|-----|-----------|------|
| V <sub>IL(MCLR)</sub>    | MCLR Input low level voltage            | VDD = 3.3 V | VSS - 0.3 | -   | 1.05      | V    |
|                          |   | VDD = 1.7 V |           |     | 0.75      |      |
| V <sub>IH(MCLR)</sub>    | MCLR Input high level voltage           | VDD = 3.3 V | 2.25      | -   | VDD + 0.3 | V    |
|                          |   | VDD = 1.7 V | 1.05      |     |           |      |
| R <sub>PU(MCLR)</sub>    | MCLR pull-up equivalent resistor        |             | 180       | 210 | 240       | kΩ   |
| t <sub>PULSE(MCLR)</sub> | MCLR input pulse width – no trigger     | VDD = 3.3 V | -         | -   | 15        | ns   |
|                          |   | VDD = 1.7 V |           |     | 10        |      |
| t <sub>TRIG(MCLR)</sub>  | MCLR input pulse width – ensure trigger |             | 250       | -   | -         | ns   |

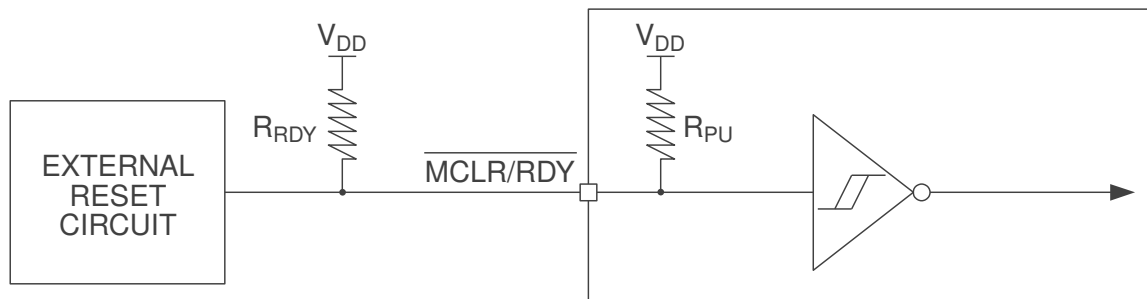


Figure 5.1: MCLR Pin Diagram

### 5.3 Miscellaneous Timings

Table 5.3: Miscellaneous Timings

| Parameter         |  | Min   | Typ      | Max   | Unit |
|-------------------|--|-------|----------|-------|------|
| f <sub>xfer</sub> | Charge transfer frequency (derived from f <sub>OSC</sub> ) | 55    | 500-1500 | 7000  | kHz  |
| f <sub>OSC</sub>  | Master CLK frequency tolerance 14 MHz                      | 13.23 | 14       | 14.77 | MHz  |



## 5.4 Digital I/O Characteristics

Table 5.4: Digital I/O Characteristics

| Parameter       | Test Conditions <sup>i</sup>                               | Min  | Max                   | Unit                  |    |
|-----------------|--|--|-----------------------|-----------------------|----|
| V <sub>OL</sub> | Output low voltage of SDA and SCL pins                     | I <sub>OL</sub> = 20 mA<br>V <sub>DD</sub> > 2 V |                       | 0.4                   | V  |
|                 |  | I <sub>OL</sub> = 20 mA<br>V <sub>DD</sub> ≤ 2 V |                       | 0.2 V <sub>DD</sub>   |    |
|                 | Output low voltage of SDA and SCL pins in GPIO output mode | I <sub>OL</sub> = 10 mA                          |                       | 0.1 V <sub>DD</sub>   |    |
|                 | Output low voltage of RDY/MCLR                             | I <sub>OL</sub> = 5 mA                           |                       |                       |    |
|                 | Output low voltage of any other GPIO pin                   | I <sub>OL</sub> = 10 mA                          |                       |                       |    |
| V <sub>OH</sub> | Output high voltage  | I <sub>OH</sub> = -5 mA                          | 0.9 V <sub>DD</sub>   | V                     |    |
| V <sub>IL</sub> | Input low voltage  |  | V <sub>SS</sub> - 0.3 | 0.3 V <sub>DD</sub>   | V  |
| V <sub>IH</sub> | Input high voltage   |  | 0.7 V <sub>DD</sub>   | V <sub>DD</sub> + 0.3 | V  |
| C <sub>b</sub>  | SDA and SCL bus capacitance                                |  |                       | 550                   | pF |

<sup>i</sup> Standard operating conditions:  
V<sub>DD</sub>: 1.8 V to 3.6 V, unless otherwise stated.  
Operating temperature: -20 °C to 80 °C.

## 5.5 I<sup>2</sup>C Characteristics

Table 5.5: I<sup>2</sup>C Characteristics

| Parameter           | Min   | Max  | Unit |    |
|---------------------|---|------|------|----|
| f <sub>SCL</sub>    | SCL clock frequency                                 | 1000 | kHz  |    |
| t <sub>HD,STA</sub> | Hold time (repeated) START                          | 0.26 | µs   |    |
| t <sub>SU,STA</sub> | Setup time for a repeated START                     | 0.26 | µs   |    |
| t <sub>HD,DAT</sub> | Data hold time                                      | 0    | ns   |    |
| t <sub>SU,DAT</sub> | Data setup time                                     | 50   | ns   |    |
| t <sub>SU,STO</sub> | Setup time for STOP                                 | 0.26 | µs   |    |
| t <sub>BUF</sub>    | Bus free time between a STOP and START condition    | 0.5  | µs   |    |
| t <sub>SP</sub>     | Pulse duration of spikes suppressed by input filter | 0    | 50   | ns |

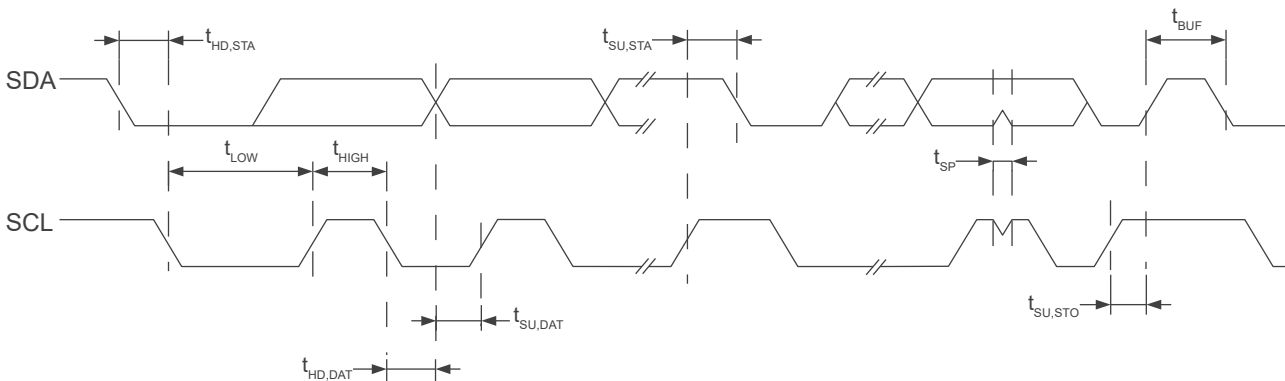


Figure 5.2: I<sup>2</sup>C Mode Timing Diagram



## 6 ProxFusion® Module

The IQS320 contains a single ProxFusion® module that uses patented technology to measure and process the sensor data.

### 6.1 Channel Options

The IQS320 is a dual channel self-capacitive sensor intended for SAR and similar proximity applications.

The below application notes provide background and information on applications where the IQS320 would be a suitable choice.

- > Azoteq Sensing Technologies: [AZD004](#)
- > Capacitive Sensing Design Guide: [AZD125](#)

### 6.2 Count Value

The sensing measurement returns a count value for each channel. Count values are inversely proportional to capacitance. The counts are filtered with the SNR Boost UI which oversamples the raw counts to improve the SNR, as such the counts do not reflect the target counts set by the user. The counts are shifted with a DC offset to a counts value of 16383 after an ATI occurs to ensure that measurements with large amounts of oversampling do not encounter numerical overflow.

Channel filtered counts are reported in the *Channel X Filtered Counts* registers.

#### 6.2.1 Max Counts

Each channel is limited to having a count value smaller than the configurable limit. The limit is set by the *Max Counts* setting in the *Prox Control* register. If the ATI setting or hardware causes measured count values higher than this, the conversion will be stopped, and the max value will be read for that relevant count value. This max value refers to a single raw measurement before oversampling has been applied.

#### 6.2.2 Linearise Counts

If the *Linearise Counts* bit in the *Sensor Setup 0* register is set, the IQS320 linearises the counts before reporting them. If this option is set the counts are inverted and the *Invert* bit in the *Sensor Setup 0* register must be set to invert the channel logic.

### 6.3 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value called the Long Term Average (LTA). The LTA of a sensor is slowly updated to track changes in the environment. During a touch or proximity event, the LTA is frozen.

Channel LTA's are reported in the *Channel X LTA* registers.



### 6.3.1 Reseed

Since the LTA for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the LTA with this value, therefore updating the value to the latest environment.

A reseed command can be given by setting the *Reseed* bit in the *System Control* register. The *Reseed* bit is automatically cleared once the reseed has been completed.

## 6.4 Prox and Touch Thresholds

Each channel has its own independently adjustable proximity and touch thresholds. If the difference between the channel's counts and LTA (also referred to as the *Delta* of the counts), exceeds the thresholds, an event will be triggered. Once a channel enters a proximity or touch state, the relevant *CHx Prox* or *CHx Touch* bits will be set in the *System Status* register, and will remain set until the channel leaves its proximity or touch state.

The *Prox Event* or *Touch Event* bits will be set in the *System Status* register when entering and exiting an the relevant state.

With non-inverted channel logic and dual direction sensing disabled, a channel will enter the proximity state if

$$\text{Delta} = \text{LTA} - \text{Counts}$$

$$\text{Delta} > \text{Prox Threshold}$$

for more than the number of consecutive samples specified by the *Prox Debounce Enter* field in the *Prox Settings* register. The channel will exit the proximity state if the above condition is not met for more than the number of consecutive samples specified by the *Prox Debounce Exit* field. The *Prox Threshold* is set in the *Prox Settings* register.

A channel will enter the touch state if

$$\text{Delta} > \text{Touch Threshold Counts}$$

and exit touch state if

$$\text{Delta} < \text{Touch Threshold Counts} - \text{Touch Hysteresis Counts}$$

Where the *Touch Hysteresis Counts* is

$$\text{Touch Hysteresis Counts} = \frac{\text{Touch Hysteresis}}{256} \times \text{Touch Threshold Counts}$$

and the *Touch Threshold Counts* is

$$\text{Let } k = \text{Post ATI Counts Snapshot} \times \text{SNR Boost Factor}$$



$$\text{Touch Threshold Counts} = \begin{cases} k \times \frac{\text{Touch Threshold}}{256} & \text{if } k < 16383 \\ 16383 \times \frac{\text{Touch Threshold}}{256} & \text{if } k \geq 16383 \end{cases}$$

The *Touch Threshold* and *Touch Hysteresis* are set in the *Touch Settings* register.

Setting a channel's *Invert* bit in the *Sensor Setup 0* register will invert the logic above. This setting is required because counts increase with user interaction when sensing mutual capacitance and inductance, and decrease when sensing self-capacitance.

If the *Dual Direction* bit in the *Sensor Setup 0* register is set, the proximity and touch thresholds will be applied in both directions, meaning that a channel will be in a proximity or touch state if

$$\text{Counts} > (\text{LTA} + \text{Threshold}) \text{ or } \text{Counts} < (\text{LTA} - \text{Threshold})$$

## 6.5 Event Timeout

A channel will be reseeded and therefore exit a proximity or touch state if it has been in a proximity or touch state for longer than the relevant time specified by the timeouts in the *Event Timeouts* register.

The times specified by the event timeouts apply to all channels.

## 6.6 Filter Betas

An Infinite Impulse Response(IIR) filter is applied to the digitized raw input for both the counts value and the LTA.

Damping options for the counts filters, LTA filters and movement filters are defined in the *Counts & LTA Filter Betas* and *LTA Fast Filter & Movement Beta* registers.

$$\text{Damping factor} = \frac{\text{Beta}}{256}$$

The *Fast Filter Band* determines when the fast beta filter is used. Fast filtering is applied to the LTA if the channel counts drift away from the LTA in the opposite direction to the sensing direction by more than the *Fast Filter Band*. Once the difference between the counts and LTA is less than the fast filter band the normal filter is used again.

## 6.7 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in ProxFusion® devices to provide optimal performance over a wide range of sensing electrode capacitances and inductance, without modification of external components.

The choice of ATI parameters has a significant impact on channel performance. The ATI algorithm is responsible for selecting each channel's dividers, multipliers and compensation.

When the *ATI Mode* in the *ATI Setup* register is set to 'Full', the *Coarse Fractional Divider*, *Fine Fractional Divider*, *Coarse Fractional Multiplier* and *Fine Fractional Multiplier* fields in the *ATI Multipliers and Dividers* register are set by the ATI algorithm using the value in the *ATI Base* register as an input



to the algorithm. The coarse parameters are set before the fine parameters. Generally, a lower base value will increase sensitivity.

Each channel's *Compensation Value* and *Compensation Divider* in the channel's *Compensation* register are set by the ATI algorithm using the *ATI Resolution Factor* in the *ATI Setup* register. A higher resolution factor will generally increase sensitivity.

When an ATI is triggered, the algorithm will first adjust the dividers and multipliers so that the counts are as close to the *ATI Base* as possible. The *Compensation Value* and *Compensation Divider* are then adjusted until the counts are as close as possible to the *ATI Target*, where:

$$\text{ATI Target} = (\text{Counts after dividers and multipliers have been set}) \times \left( \frac{\text{ATI Resolution Factor}}{16} \right)$$

In certain cases it is desirable to fix some or all of the dividers and multipliers at design time. For these cases, the *ATI Mode* can be set to 'ATI from Fine Fractional Divider', 'ATI from Compensation Divider' or 'Compensation Only'.

For inductive measurements, the *Compensation Value* should be minimised and the *Compensation Divider* should be maximised or disabled. This is achieved by setting the *ATI Resolution Factor* to '16' with ATI enabled, or disabling ATI and setting both the *Compensation Value* and *Compensation Divider* to '0'.

It is recommended to set the *ATI Mode* to 'Full' and to allow the ATI algorithm to select the dividers, multipliers and compensation.

## 6.8 Automatic Re-ATI

### 6.8.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled.

When a re-ATI occurs the *ATI Event* bit in the *System Status* register will be set. It is cleared when read by the master through I<sup>2</sup>C.

### 6.8.2 Conditions for Re-ATI to Activate

A re-ATI is executed when the LTA of a channel drifts outside of the *ATI Band*. The band is centered around the *ATI Target*. The *ATI Band* for all channels is configured in the *ATI Setup* register.

$$\text{Re-ATI Boundary} = \text{LTA snapshot} \pm \text{ATI Band}$$

Where the *ATI Band* is computed by

$$\text{Small ATI Band} = \left( \frac{1}{16} \times \text{ATI TARGET} \times \text{SNR Boost Factor} \right)$$



$$\text{Large ATI Band} = \left( \frac{1}{8} \times \text{ATI TARGET} \times \text{SNR Boost Factor} \right)$$

Note that I<sup>2</sup>C communications are disabled for the duration of the ATI process.

### 6.8.3 ATI Error

After the ATI algorithm is executed, a check is done to see if there are any errors. The *ATI Error* bit in the *System Status* register is set if the following is true for any channel after the ATI has completed:

- > Counts are outside the **Re-ATI Boundary** upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set *ATI Error*. The flag status is only updated again when a new ATI algorithm is performed.

**A Re-ATI will not be automatically triggered if an ATI Error occurs.** If an ATI Error occurs the master should manually trigger a re-ATI by setting the *Re-ATI* bit in the *System Control* register. The *Re-ATI* bit is automatically cleared by the IQS320.



## 7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

*Only certain parameters are described below. The other hardware parameters are not discussed as they should only be adjusted under guidance of Azoteq support engineers.*

### 7.1 Charge Transfer Frequency

The charge transfer frequency ( $F_{xfer}$ ), also known as the conversion frequency, is set using the *Conversion Frequency Fraction* and *Conversion Frequency Period* fields in the *Conversion Frequency Setup* register. For high resistance sensors, it might be needed to decrease  $F_{xfer}$ .

It is recommended to always set the *Conversion Frequency Fraction* to '127' and to select the conversion frequency with the *Conversion Frequency Period*.

The *Dead Time Enable* option in the *Prox Input and Control* register must be considered when setting the conversion frequency. Dead time should always be enabled for capacitance measurements.

Please refer to Table A.1 to select suitable *Conversion Frequency Period* values for the desired conversion frequency.

### 7.2 Reset

#### 7.2.1 Reset Indication

After a reset, the *Reset Event* bit in the *System Status* register will be set to indicate a reset event occurred. The *Reset Event* bit is cleared when the master sets the *ACK Reset* bit in the *System Control* register.

After a reset event, the chip's settings revert to their start-up values. To recover, the master must first acknowledge the reset event by setting the *ACK Reset* bit, and then re-write all the application settings to the IQS320 over I<sup>2</sup>C.

#### 7.2.2 Software Reset

The IQS320 can be forced to reset by setting the *Soft Reset* bit in the *System Control* register.

#### 7.2.3 Hardware Reset

Pulling the Ready / Master Clear (RDY/MCLR) pin low will hard reset the device. When a communications window is open, the IQS320 disables MCLR functionality and pulls RDY/MCLR low. Therefore, the master cannot hard reset the IQS320 when RDY/MCLR is low.

For MCLR reset levels see Section 5.2.

## 8 Additional Features

### 8.1 Reference UI

The IQS320 implements a Reference Tracking User Interface (Reference UI). The Reference UI can be enabled by setting the *Reference Tracking* bit in the *System Control* register.

When *Reference Tracking* is enabled, CH0 is the dedicated sensing channel and CH1 is the dedicated reference channel as illustrated in Figure 8.1. CH0 and CH1 can be configured to be either CRx0/CTx0 or CRx1/CTx1.

The reference channel sensor should be exposed to the same conditions and capacitive loads as the sensing channel, and the user should not be able to affect the counts of the reference channel.

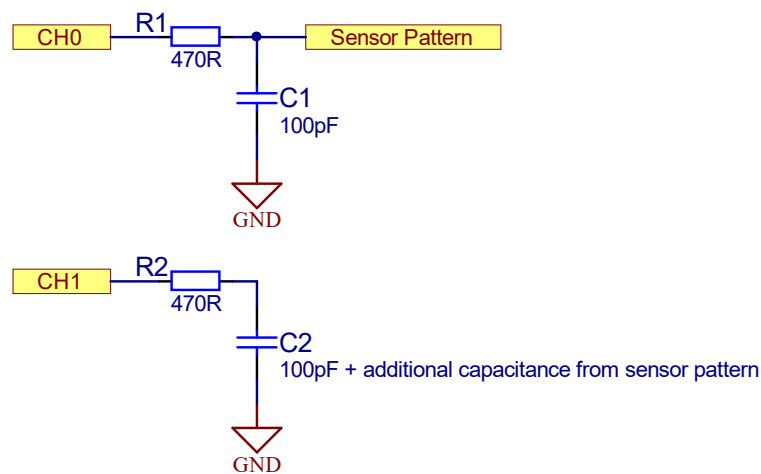


Figure 8.1: Example hardware schematic for Reference UI with 100 pF load capacitor.

The reference channel adjusts the counts of the primary sensing channel by subtracting the change in counts of the reference channel from the counts of the primary sensing channel. The change in counts of the reference channel is calculated by taking a snapshot of the LTA of the reference channel after the device completes an ATI routine and subtracting the counts of the reference channel from the snapshot.

The Reference UI is able to reduce the effects of sensor drift due to temperature. The Reference UI also has the ability to reduce noise that is common to both sensing and reference channels which improves the signal to noise ratio (SNR). The Reference UI performs best when used in conjunction with the *SNR Boost UI*

The *Reference Multiplier* and *Reference Divider* in the *Reference Scaling* register is used to compensate for any differences in the amount of drift between the sensing and reference channel.

$$\text{Counts}_{\text{Adjusted}} = \text{Counts} - (\text{Counts}_{\text{Ref}} - \text{Counts}_{\text{Ref LTA Snapshot}}) \times \frac{\text{Multiplier}_{\text{Ref}}}{\text{Divider}_{\text{Ref}}}$$

### 8.2 Movement UI

The IQS320 implements a Movement User Interface (Movement UI). The Movement UI can be enabled by setting the *Movement Enable* bit in the *Sensor Setup 0* register.



When in a touch state and no movement is detected on a channel, the channel will reseed once the touch timeout expires and the channel will exit the touch state. However, if the Movement UI is enabled, any movement will cause the touch timeout timer to reset, thereby keeping the channel in a touch state.

The movement is calculated by subtracting a filtered version of the counts from the counts of the channel, resulting in a pseudo-gradient function representing the movement of a channel. The damping factor used to calculate the movement can be set by the *Movement Beta* field in the *LTA Fast Filter & Movement Beta* register. A higher value will increase the sensitivity of the movement detector.

### 8.2.1 Movement Threshold

When the *Channel x Movement* value exceeds the *Movement Threshold* set in the *Movement Settings* register, an event will be triggered. Once movement is detected, the relevant *CHx Movement* bit will be set in the *System Status* register, and will remain set until there is no movement detected.

Similar to the *Proximity Threshold*, the *Movement Threshold* uses debouncing to enter and exit a movement event. The *Movement Debounce* settings can be adjusted in the *Movement Settings* register.

## 8.3 SNR Boost UI

The IQS320 implements a Signal to Noise Ratio Boost User Interface (SNR Boost UI).

The signal to noise ratio is drastically improved by oversampling which decreases the quantisation noise while increasing the sampling resolution of the signal. Oversampling the signal will increase the sampling time and current consumption of the device. It should be noted that there is a decrease in the dynamic resolution at High SNR Boost Factors.

The *SNR Boost Factor* setting in the *Events Enable & SNR Boost Factor* register controls how many times the signal should be oversampled. SNR boost is disabled by setting the *SNR Boost Factor* to a value of 1. *SNR Boost Factor* values larger than 50 are not recommended.

## 8.4 Standalone Mode

The IQS320 is able to run in a standalone mode. Standalone mode can be entered by setting the *Interface Selection* to standalone in the *System Control* register.

In standalone mode, InputA is used to toggle the touch event timeout. The timeout can be disabled by connecting InputA to VDD. If InputA is connected to VDD then the touch state will never timeout and the device will remain in touch until the counts are no longer above the touch threshold. Connecting InputA to VSS will enable the touch event timeout. When the touch event timeout is reached, the LTA on that channel will reseed causing the channel to exit the touch state <sup>i</sup>.

The I<sup>2</sup>C lines are used as digital outputs in standalone mode. SDA/OutA is a push-pull active high output and SCL/OutB is an open-drain active low output. These outputs will be active if any channel is in a touch state.

In standalone mode, an I<sup>2</sup>C ready window will occur once on startup to allow the user to enter an I<sup>2</sup>C debugging mode where the user can access the settings and stream data as if in I<sup>2</sup>C streaming mode. To enter the debugging mode, write *0xC0* to the *System Control* register in the startup window. The

<sup>i</sup> Do not leave InputA in a floating state.



device can be set back to standalone mode from the I<sup>2</sup>C debugging mode and will retain any settings written to it<sup>ii</sup>.

### 8.4.1 ATI Indication

ATI indication can be enabled on the IQS320 device in standalone mode. SDA/OutA and SCL/OutB will be active while an ATI is active. An ATI event will always occur on startup which will indicate that the device is powered on. This can be enabled by setting the *ATI Indication* bit in the *System Control* register.

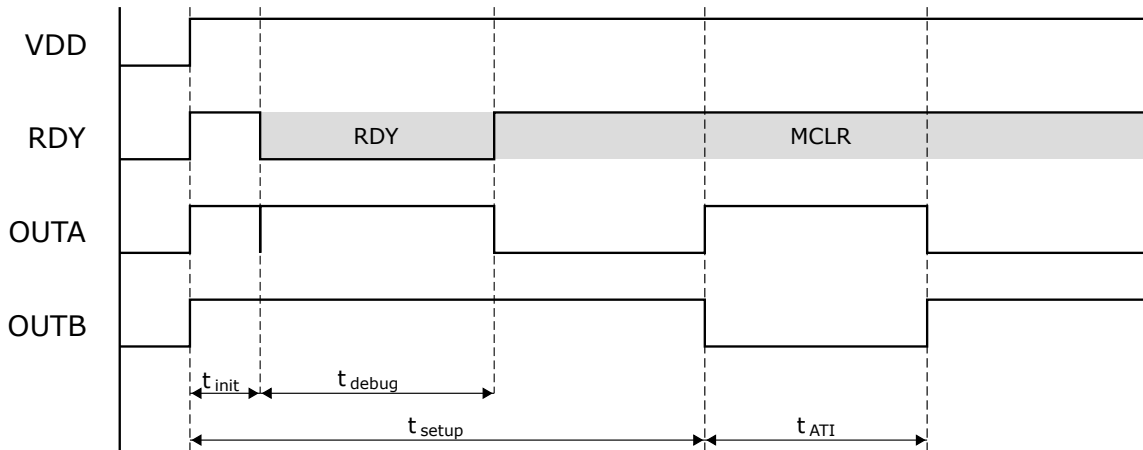


Figure 8.2: Power On Sequence Specification with ATI indication enabled

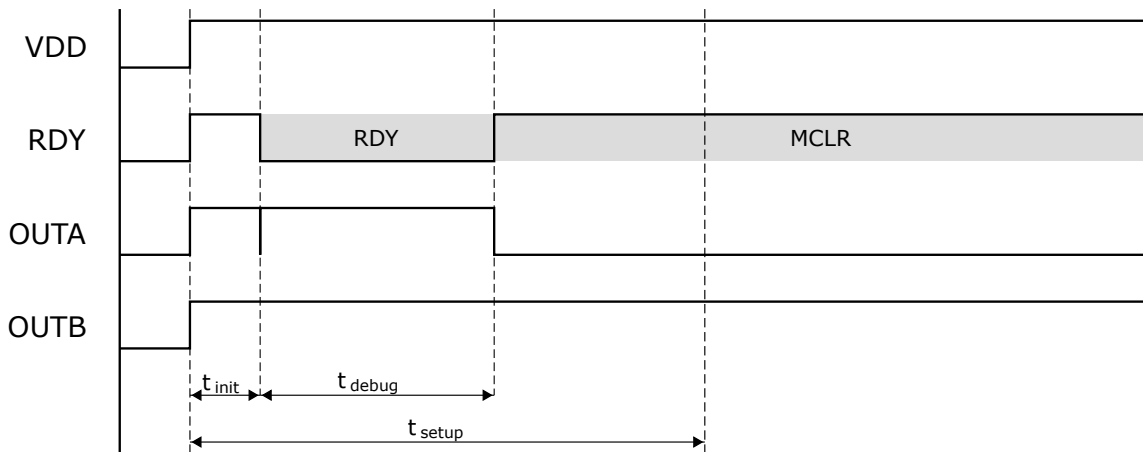


Figure 8.3: Power On Sequence Specification with ATI indication disabled

| Timing Parameter | Nominal | Tolerance | Unit |
|------------------|---------|-----------|------|
| Initialisation   | 10.0    | -         | ms   |
| Setup            | 361.5   | -         | ms   |
| Debug window     | 208.5   | -         | ms   |
| ATI              | 220.0   | ±20       | ms   |

<sup>ii</sup> After the device exits debugging mode, a reset or power cycle is required to start another debugging session.



## 8.5 Watchdog Timer

The IQS320 implements a hardware watchdog timer. The watchdog timer is set to expire after 255ms if not kicked and will trigger a software reset upon expiration.

During I<sup>2</sup>C communication the IQS320 kicks the watchdog timer whenever a byte level read or write occurs. Therefore, if the master initiates communication by sending an I<sup>2</sup>C START condition and does not complete the I<sup>2</sup>C transaction, the IQS320 will reset after 255 ms.

The I<sup>2</sup>C transaction is completed either when an I<sup>2</sup>C STOP notification is sent by the master or when the master ends the communication as described in Section 9.8.

Outside of a communications window, the IQS320 will automatically kick the watchdog every cycle. The master is not required to manually kick the watchdog.



## 9 I<sup>2</sup>C Interface

### 9.1 I<sup>2</sup>C Module Specification

The device supports a standard two wire I<sup>2</sup>C interface with the addition of a RDY (ready interrupt) line. The RDY pin also serves as a Master Clear (MCLR) and can be used to hard reset the device (Section 7.2.3). Byte level clock stretching is allowed. The communications interface of the IQS320 supports the following:

- > *Fast-mode-plus* standard I<sup>2</sup>C up to 1 MHz.
- > Streaming data as well as event mode.
- > The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS320 implements 8-bit addressing with 2 bytes at each address.

### 9.2 I<sup>2</sup>C Address

The 7-bit device address is 0x47 ('01000111') with an alternate address which is 0x48 ('01001000'). The full address byte for address 0x47 will thus be 0x8F (read) or 0x8E (write) and the full address byte for address 0x48 will thus be 0x91 (read) or 0x90 (write)<sup>i</sup>.

The device will check if InputA is set to VSS or VDD<sup>ii</sup>. If it is set to VSS it will choose to use address 0x47 and if it is set to VDD then it will choose to use address 0x48. This check is only performed on start up and the state of InputA will not affect the device address after startup.

### 9.3 I<sup>3</sup>C Compatibility

This device is not compatible with an I<sup>3</sup>C bus due to clock stretching allowed for data retrieval.

### 9.4 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words meaning that two bytes are stored at each address. For example, address 0x10 will provide two bytes. The next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

### 9.5 Ready (RDY) Indicator

The IQS320 has an open-drain active low RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and initiate I<sup>2</sup>C communication only when the RDY signal is low.

The RDY line also serves as a reset pin. Reset functionality is described in Section 7.2.3.

<sup>i</sup> The device will also acknowledge an I<sup>2</sup>C address of 0x46 for address 0x47 and 0x49 for address 0x48. Writing to this address will cause the IQS320 to enter a low level debugging mode and should not be done under normal operating conditions. Therefore, both 0x47 and 0x46 or 0x48 and 0x49 are reserved on the I<sup>2</sup>C bus when using the IQS320.

<sup>ii</sup> Do not leave InputA in a floating state.



## 9.6 Communications Window

When the device has data for the master, it will pull the RDY line low. This indicates that the device has opened its communications window and is expecting the master to address it. When the communication window is closed the IQS320 releases the RDY line. For information on when the communications window is closed see Section 9.8.

Transfer of data between the master and slave must occur during the communications window (RDY is low). If the master wishes to initiate communication outside of a communications window (RDY is high), a force communications request must be made. Section 9.11.2 describes the force communications request sequence.

## 9.7 I<sup>2</sup>C Transaction Timeout

If the communication window is not serviced within the time specified in milliseconds by the *I<sup>2</sup>C Transaction Timeout* register, the communications window is closed (RDY goes high) and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the data for the closed window will be lost. The default *I<sup>2</sup>C Transaction Timeout* is set to 200 ms. The *I<sup>2</sup>C Transaction Timeout* must be between 2 ms and 230 ms. The *I<sup>2</sup>C Transaction Timeout* is measured from the start of the communications window (RDY goes low).

Once communication between the master and the IQS320 has begun (START condition on I<sup>2</sup>C lines), the I<sup>2</sup>C transaction timeout is disabled leaving the watchdog timer in control. For more information on the behaviour of the device under these conditions see Section 8.5.

## 9.8 Terminate Communication

A standard I<sup>2</sup>C STOP will close the current communication window.

If the *Stop Bit Disable* bit in the *I2C Settings* register is set, the device will not respond to a standard I<sup>2</sup>C STOP. The communication window must be terminated using the end communications command (0xFF) shown in Figure 9.1.

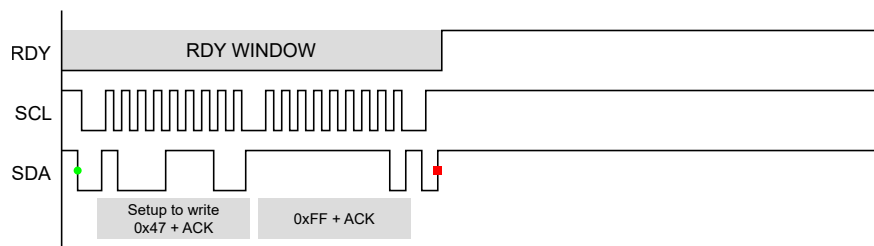


Figure 9.1: Force Stop Communication Sequence

## 9.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- > The host is trying to read from a memory map register that does not exist.
- > The host is trying to read from the device outside of a communication window (i.e. while RDY = high).



## 9.10 I<sup>2</sup>C Interface

The IQS320 has 2 I<sup>2</sup>C interface types. The I<sup>2</sup>C interface is selected by adjusting the *Interface Selection* in the *System Control* register.

### 9.10.1 I<sup>2</sup>C Streaming

I<sup>2</sup>C Streaming mode refers to constant data reporting at the relevant sampling period specified in the *Sampling Period* register.

### 9.10.2 I<sup>2</sup>C Event Mode

In event mode the RDY line will only go low when one or more of the enabled events are triggered or if the device resets. This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred.

## 9.11 Event Mode Communication

For event mode to function correctly the following requirements must be met:

- > Required events must first be enabled from the *Events Enable* register.
- > Enabled events must be serviced by reading from the *System Status* register (0x10) to ensure all event flags are cleared. If these flags are not cleared continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode.

### 9.11.1 Events

Enabled events are reported in the *System Status* register when triggered. Global events can be individually enabled by setting the relevant bit in the *Events Enable* register.

The following events are available:

*Table 9.1: Events Descriptions*

| Event     | Trigger Condition   |
|-----------|---|
| ATI Error | There has been an error during the ATI process                        |
| ATI Event | ATI has been triggered  |
| Movement  | There has been a transition of the movement state for either channels |
| Touch     | There has been a transition of the touch state for either channels    |
| Prox      | There has been a transition of the prox state for either channels     |

### 9.11.2 Force Communication

In streaming mode, the IQS320 I<sup>2</sup>C will provide Ready (RDY) windows at intervals specified by the sampling period. Ideally, communication with the IQS320 should only be initiated in a RDY window. A communication request described in the figure below will force a RDY window to open. In event mode RDY windows are only provided when an event is reported. A RDY window must be requested to write



or read settings outside of this provided window. The time between the communication request and the opening of a RDY window ( $t_{wait}$ ) is typically less than 0.5 ms<sup>iii</sup>.

Communications has a higher priority than sampling on the IQS320. If forced communications occurs while the data is being sampled, the current data sample will be discarded and the previous sample will be retained. The period between force communications should be an integer multiple or longer than the sampling rate.

The communication request sequence is shown in Figure 9.2.

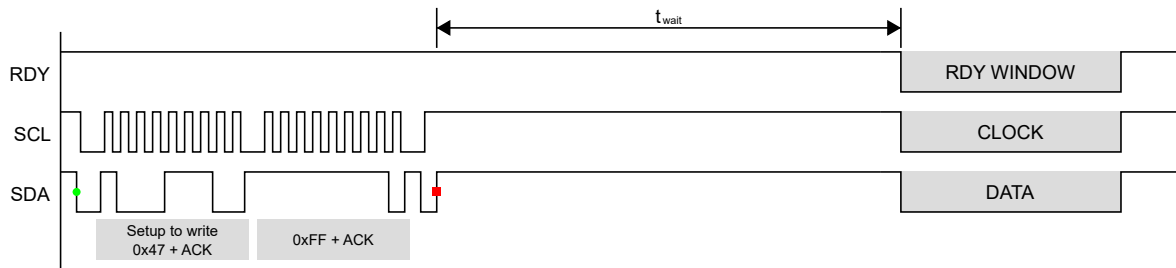


Figure 9.2: Force Communication Sequence

## 9.12 Read/Write Check Disable

By default, some registers such as the counts and LTA values are read only. Writing to these registers over I<sup>2</sup>C will have no effect. Setting the *Read/Write Check Disable* bit in the *I2C Settings* register will allow the master to write to any register and force its value.

<sup>iii</sup> Only applicable for [Default Configuration 200](#).



### 9.12.1 Program Flow Diagram

The program flow for event mode communication is shown in Figure 9.3.

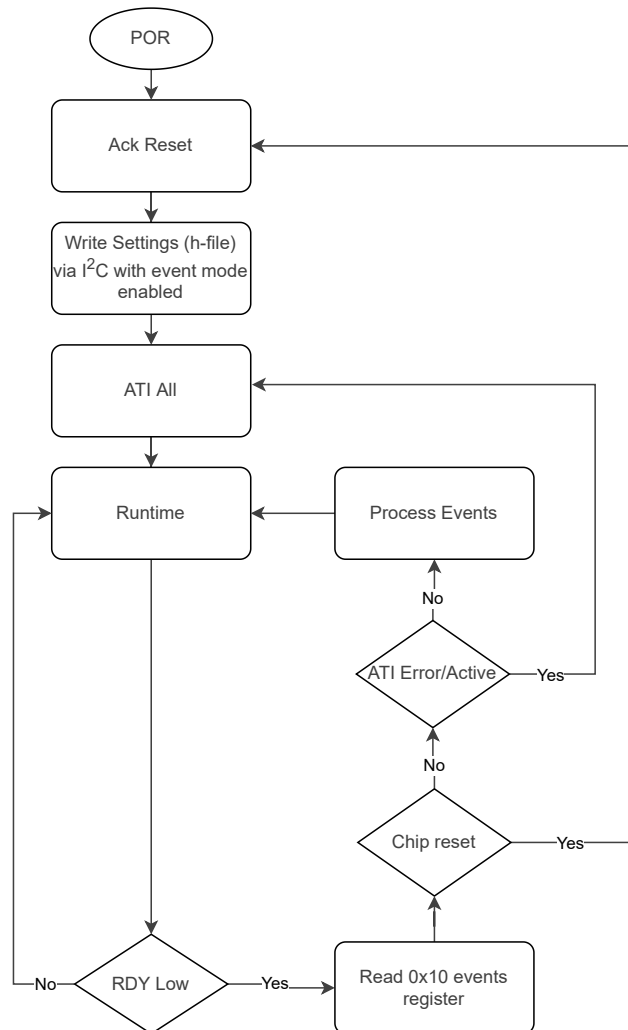


Figure 9.3: Program Flow Diagram



## 10 Memory Map Register Descriptions

| Address           | Data (16bit)                                    | Notes            |
|-------------------|---|------------------|
| 0x00 - 0x09       | Version details                                 | See Section A.1  |
| <b>Read Only</b>  | <b>System Information</b>                       |                  |
| 0x10              | Systems Status                                  | See Section A.2  |
| 0x11              | Channel 0 Filtered Counts                       | 16-bit value     |
| 0x12              | Channel 1 Filtered Counts                       |                  |
| 0x13              | Channel 0 LTA                                   |                  |
| 0x14              | Channel 1 LTA                                   |                  |
| 0x15              | Channel 0 Movement                              |                  |
| 0x16              | Channel 1 Movement                              |                  |
| 0x17              | Channel 0 Pre Reference Tracking                |                  |
| 0x18              | Channel 1 Pre Reference Tracking                |                  |
| 0x19              | Channel 0 Raw                                   |                  |
| 0x1A              | Channel 1 Raw                                   |                  |
| 0x1B              | Channel 0 Post ATI Snapshot                     |                  |
| 0x1C              | Channel 1 Post ATI Snapshot                     |                  |
| <b>Read/Write</b> | <b>Sensor 0 Setup</b>                           |                  |
| 0x20              | Sensor Setup 0                                  | See Section A.3  |
| 0x21              | Conversion Frequency Setup                      | See Section A.4  |
| 0x22              | Prox Control                                    | See Section A.5  |
| 0x23              | Timing Generator Control & Prox Input           | See Section A.6  |
| 0x24              | Inactive Rxs & Calibration Capacitor Selection  | See Section A.7  |
| 0x25              | ATI Setup                                       | See Section A.8  |
| 0x26              | ATI Base  | 16-bit value     |
| 0x27              | ATI Multipliers and Dividers                    | See Section A.9  |
| 0x28              | ATI Compensation                                | See Section A.10 |
| <b>Read/Write</b> | <b>Sensor 1 Setup</b>                           |                  |
| 0x30              | Sensor Setup 0                                  | See Section A.3  |
| 0x31              | Conversion Frequency Setup                      | See Section A.4  |
| 0x32              | Prox Control                                    | See Section A.5  |
| 0x33              | Timing Generator Control & Prox Input           | See Section A.6  |
| 0x34              | Pad Control and Calibration Capacitor Selection | See Section A.7  |
| 0x35              | ATI Setup                                       | See Section A.8  |
| 0x36              | ATI Base  | 16-bit value     |
| 0x37              | ATI Multipliers Selection                       | See Section A.9  |
| 0x38              | ATI Compensation                                | See Section A.10 |
| <b>Read/Write</b> | <b>Channel 0 Setup</b>                          |                  |
| 0x40              | Prox Settings                                   | See Section A.11 |
| 0x41              | Touch Settings                                  | See Section A.12 |
| 0x42              | Movement Settings                               | See Section A.13 |
| <b>Read/Write</b> | <b>Channel 1 Setup</b>                          |                  |
| 0x50              | Prox Settings                                   | See Section A.11 |
| 0x51              | Touch Settings                                  | See Section A.12 |
| 0x52              | Movement Settings                               | See Section A.13 |
| <b>Read/Write</b> | <b>Filter Betas</b>                             |                  |
| 0x60              | Counts Filter Beta & LTA Filter Beta            | See Section A.14 |
| 0x61              | LTA Fast Filter Beta & Movement Beta            | See Section A.15 |
| 0x62              | Fast Filter Band                                | 16 bit value     |
| <b>Read/Write</b> | <b>System Control</b>                           |                  |
| 0x70              | System Control                                  | See Section A.16 |



|                   |  |                                      |
|-------------------|--|--------------------------------------|
| 0x71              | Sampling Period                          | 16-bit value (ms)<br>Range: 0 - 3000 |
| 0x72              | I <sup>2</sup> C Transaction Timeout     | 16 bit value (ms)<br>Range: 2 - 230  |
| 0x73              | Event Timeouts                           | See Section A.17                     |
| 0x74              | Events Enable & SNR Boost Factor         | See Section A.18                     |
| 0x75              | Reference Scaling                        | See Section A.19                     |
| <b>Read/Write</b> | <b>I<sup>2</sup>C Low Level Settings</b> |                                      |
| 0x80              | I <sup>2</sup> C Setup                   | See Section A.20                     |



## 11 Ordering Information

### 11.1 Ordering Code

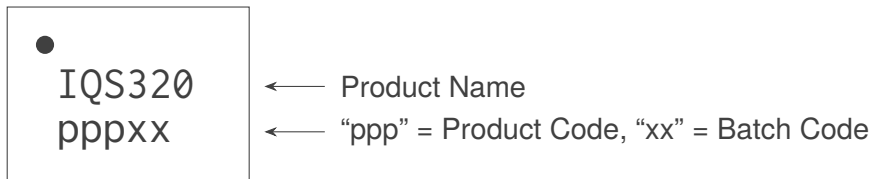
IQS320    zzz    ppb

|                              |     |   |                   |  |
|------------------------------|-----|---|-------------------|--|
| <b>IC NAME</b>               |     | = |                   | IQS320   |
| <b>DEFAULT CONFIGURATION</b> | zzz | = | 100 <sup>i</sup>  | I <sup>2</sup> C   |
|                              |     | = | 200 <sup>ii</sup> | I <sup>2</sup> C   |
| <b>PACKAGE TYPE</b>          | pp  | = | CS                | WLCSP-11 package   |
|                              |     | = | QF                | QFN-20 package   |
|                              |     | = | DN                | DFN-12 package (On special order only <sup>iii</sup> )                                   |
| <b>BULK PACKAGING</b>        | b   | = | R                 | WLCSP-11 Reel (3000pcs/reel)<br>QFN-20 Reel (2000pcs/reel)<br>DFN-12 Reel (6000pcs/reel) |

*Figure 11.1: Order Code Description*

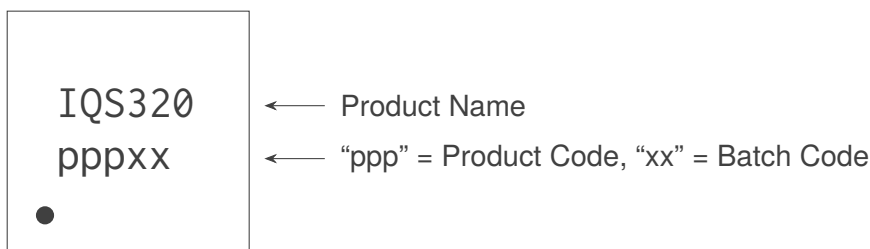
### 11.2 Top Marking

#### 11.2.1 WLCSP11 Package Marking



*Figure 11.2: IQS320-WLCSP11 Package Top Marking*

#### 11.2.2 DFN12 Package Marking Options

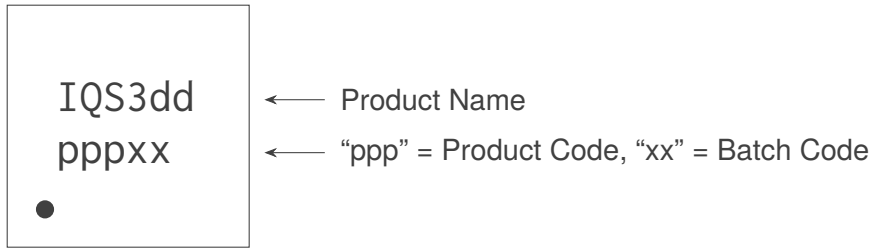


*Figure 11.3: IQS320-DFN12 Package Top Marking*

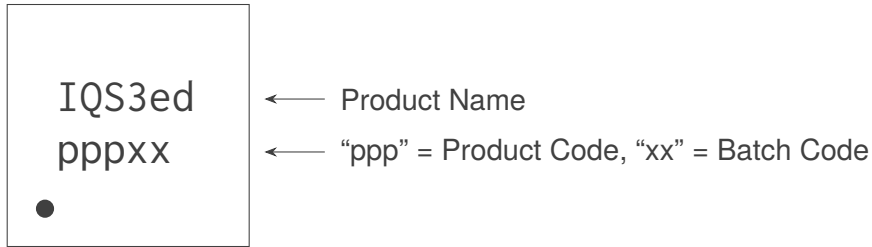
<sup>i</sup> NRFND (not recommended for new designs)

<sup>ii</sup> Improved force communications response time

<sup>iii</sup> Special order codes are subject to larger minimum order quantities, longer lead times, and are non-cancel, non-returnable.

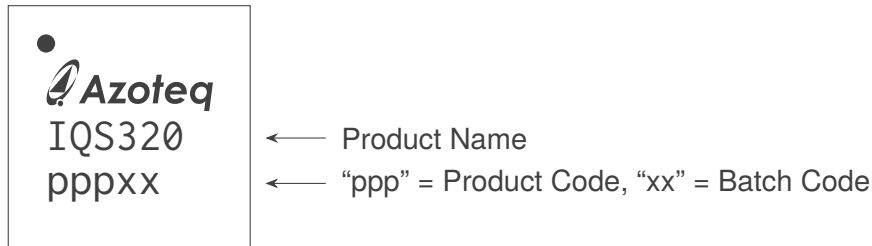


*Figure 11.4: IQS3dd-DFN12 Package Top Marking*



*Figure 11.5: IQS3ed-DFN12 Package Top Marking*

### 11.2.3 QFN20 Package Marking Options



*Figure 11.6: IQS320-QFN20 Package Top Marking*



## 12 Package Specification

### 12.1 Package Outline Description – WLCSP11

This package outline is specific to order codes ending in WLCSP.

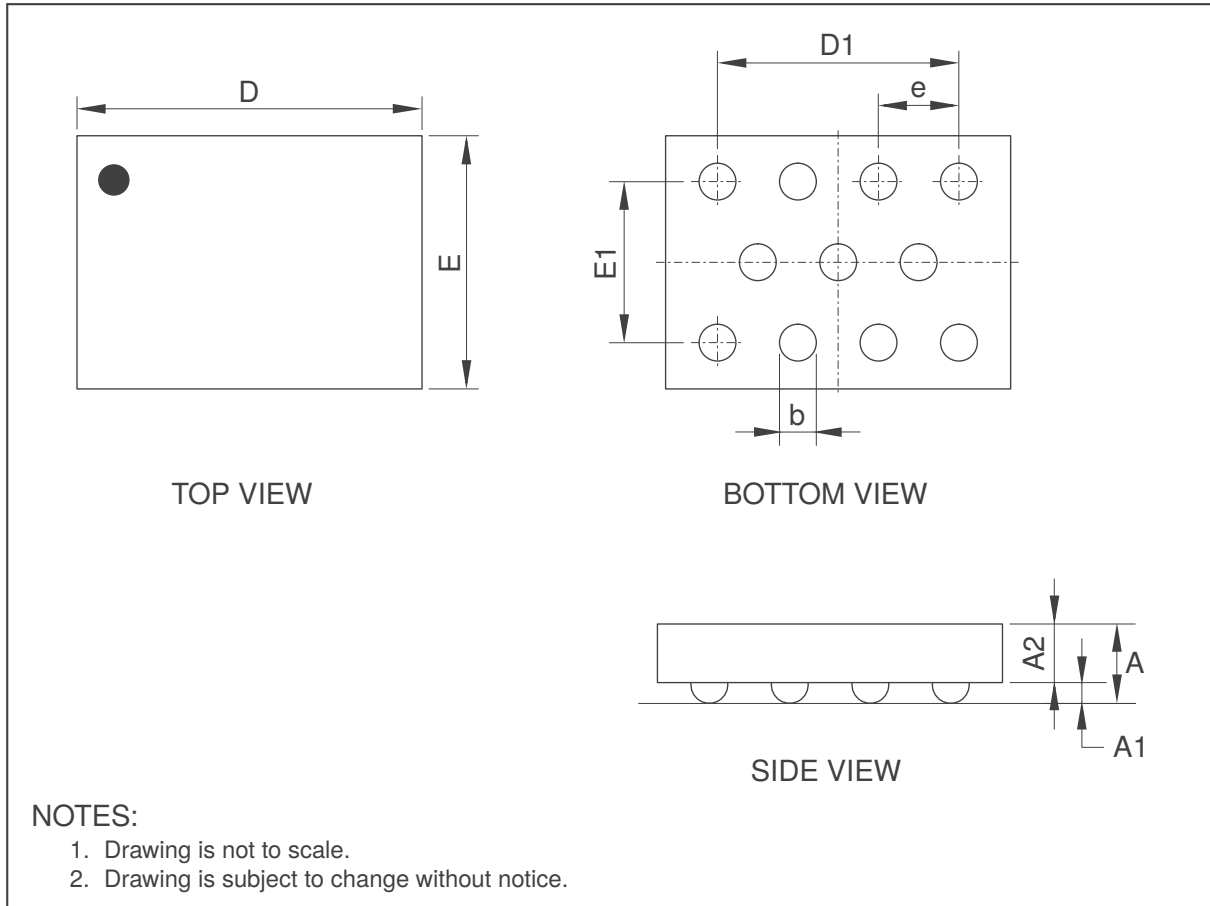


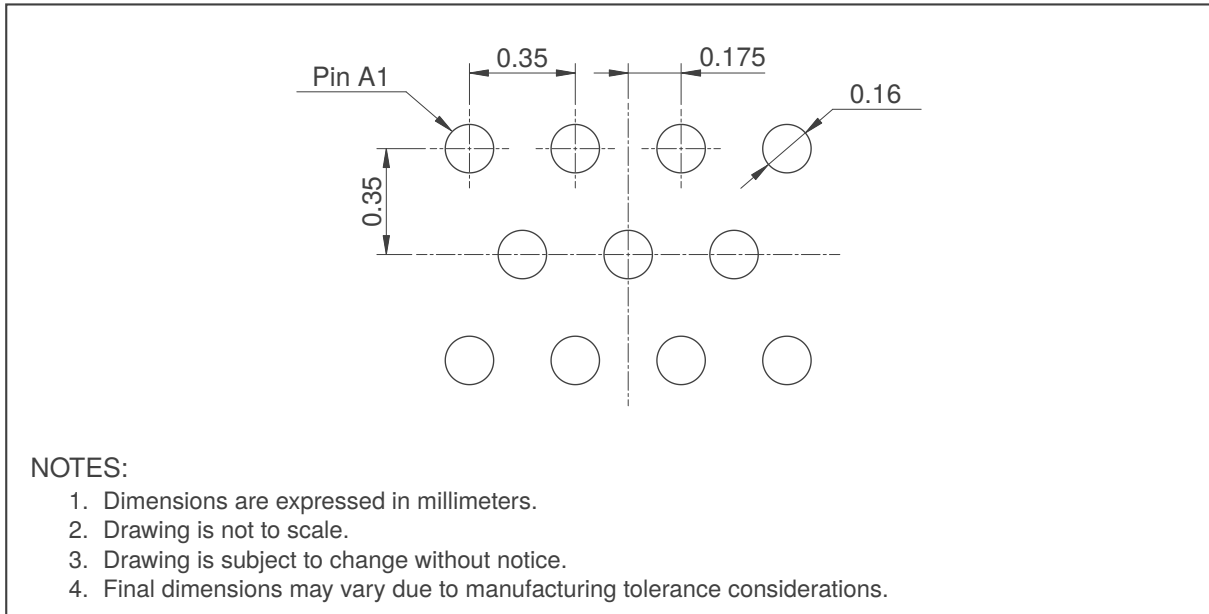
Figure 12.1: WLCSP11 (1.48x1.08) Package Outline Visual Description

Table 12.1: WLCSP11 (1.48x1.08) Package Outline Visual Description (mm)

| Dimension | Min       | Nom   | Max   |
|-----------|-----------|-------|-------|
| A         | 0.303     | 0.345 | 0.387 |
| A1        | 0.076     | 0.090 | 0.104 |
| A2        | 0.227     | 0.255 | 0.283 |
| D         | 1.46      | 1.48  | 1.50  |
| E         | 1.06      | 1.08  | 1.10  |
| D1        | 1.05 BSC  |       |       |
| E1        | 0.700 BSC |       |       |
| b         | 0.136     | 0.160 | 0.184 |
| e         | 0.350 BSC |       |       |



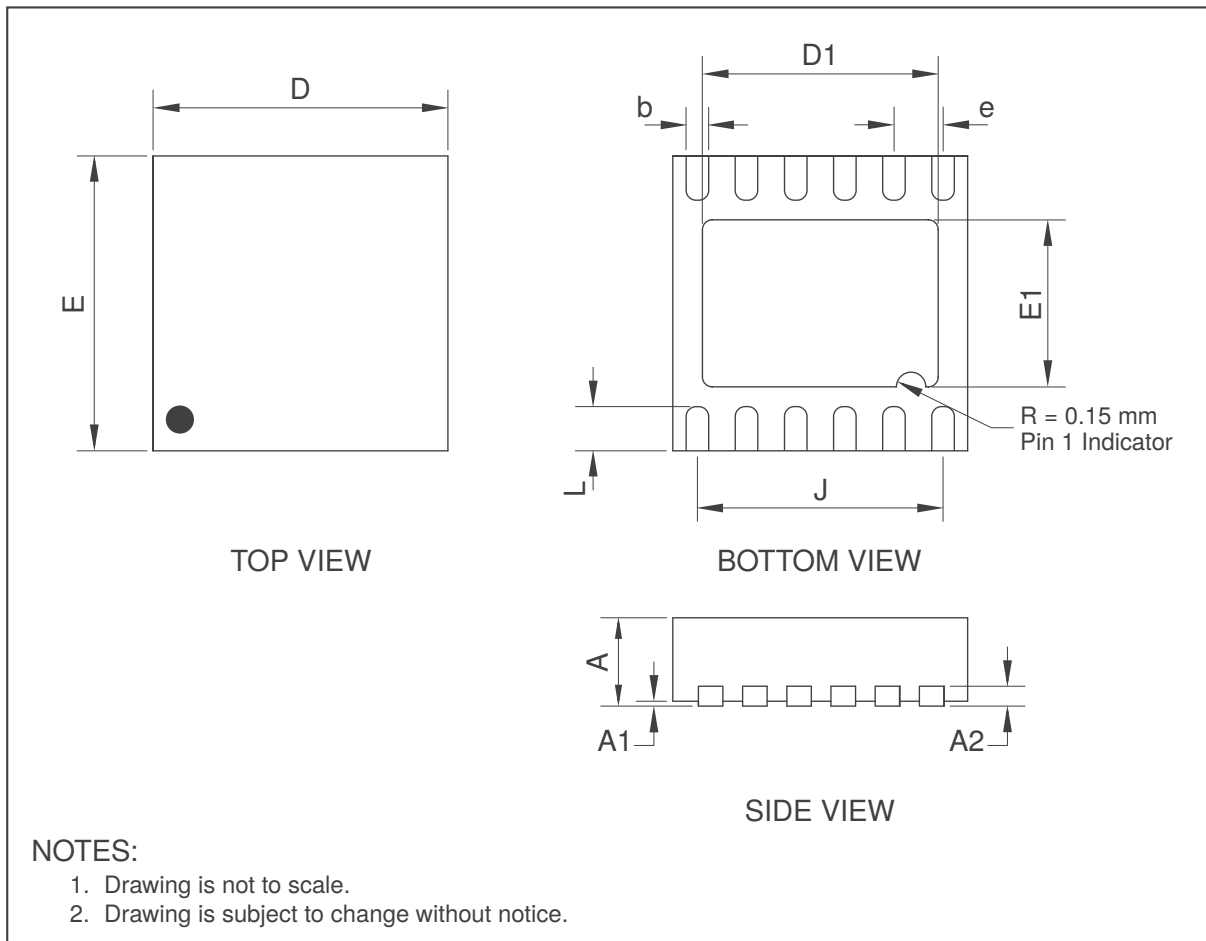
## 12.2 Package Footprint Description – WLCSP11



*Figure 12.2: WLCSP11 Recommended Footprint*



### 12.3 Package Outline Description – DFN12



*Figure 12.3: DFN (3x3)-12 Package Outline Visual Description*

*Table 12.2: DFN (3x3)-12 Package Outline Visual Description (mm)*

| Dimension | Min       | Nom  | Max  |
|-----------|-----------|------|------|
| A         | 0.70      | 0.75 | 0.80 |
| A1        | 0.00      |      | 0.05 |
| A2        | 0.203 REF |      |      |
| D         | 2.95      | 3.00 | 3.05 |
| E         | 2.95      | 3.00 | 3.05 |
| D1        | 2.35      | 2.40 | 2.45 |
| E1        | 1.65      | 1.70 | 1.75 |
| J         | 2.50 REF  |      |      |
| L         | 0.40      | 0.45 | 0.50 |
| b         | 0.18      | 0.23 | 0.28 |
| e         | 0.50 BSC  |      |      |



## 12.4 Package Footprint Description – DFN12

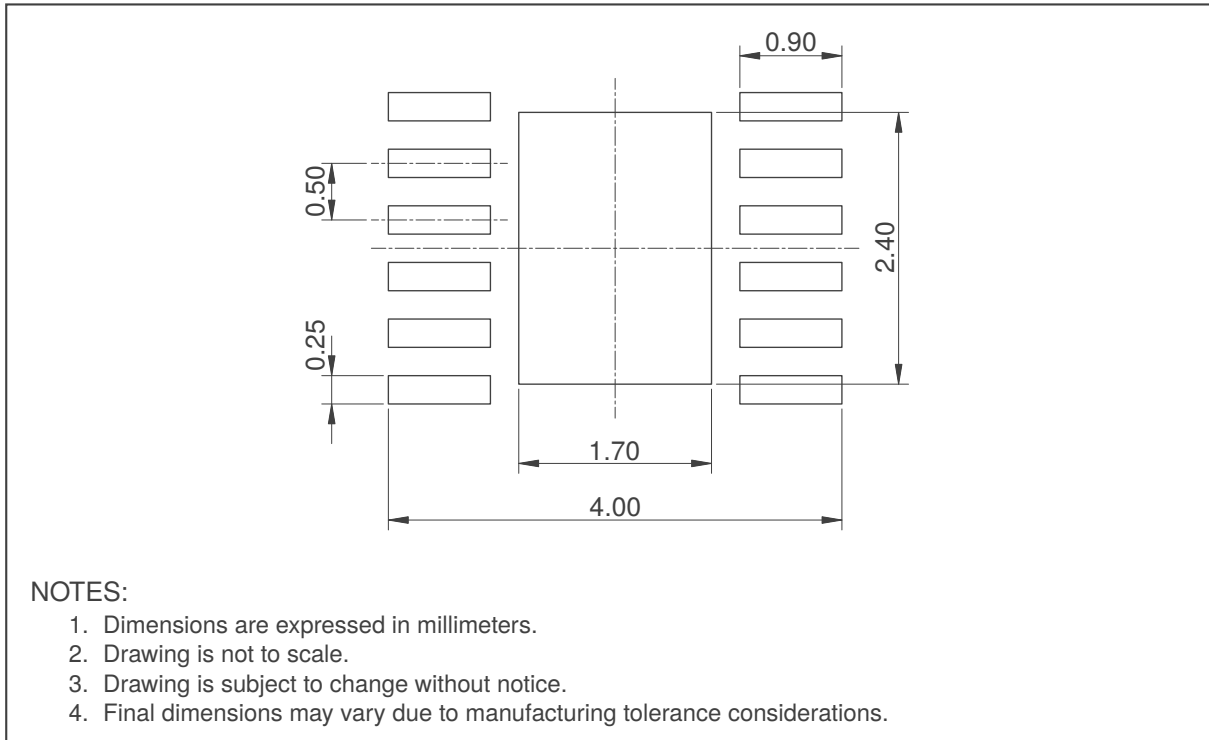


Figure 12.4: DFN12 Recommended Footprint

## 12.5 Package Outline Description – QFN20

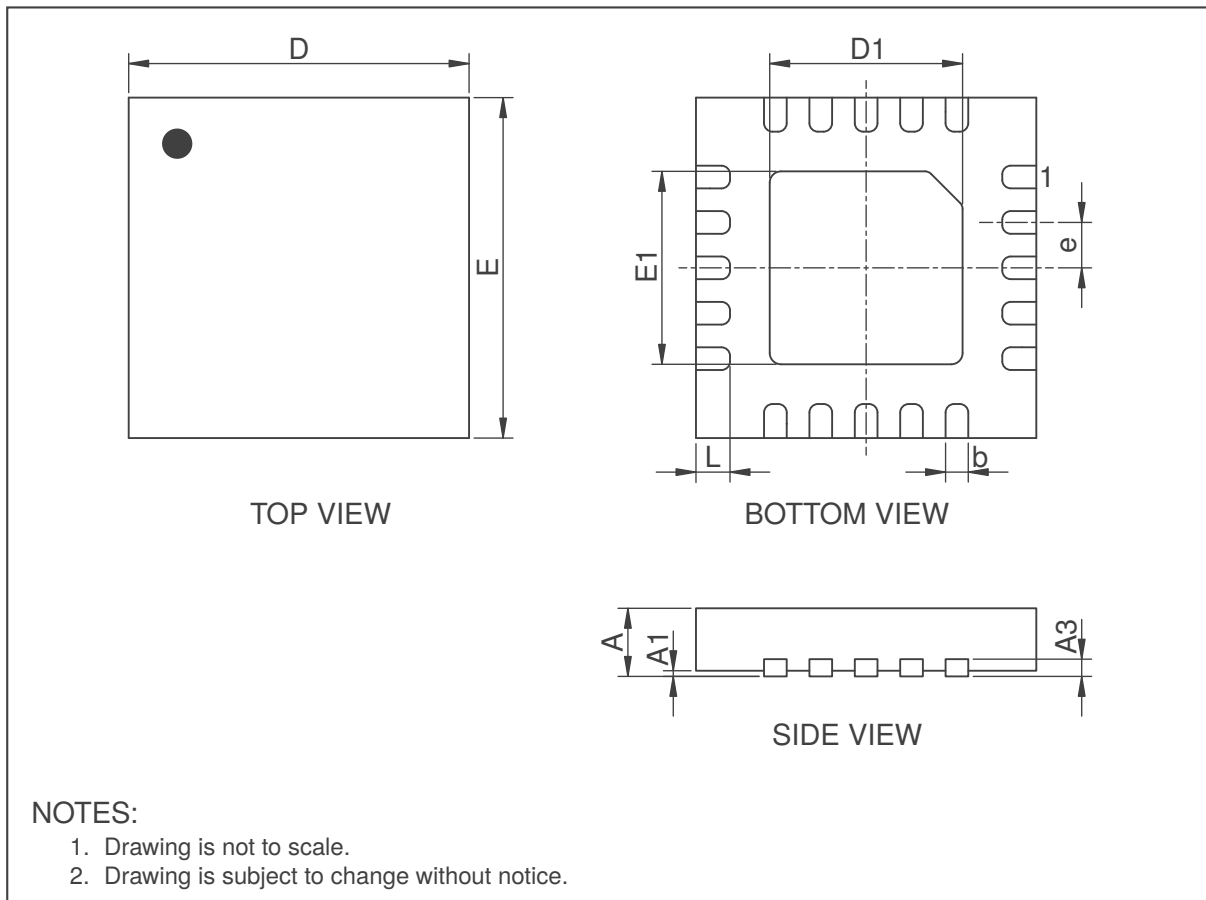


Figure 12.5: QFR (3x3)-20 Package Outline Visual Description

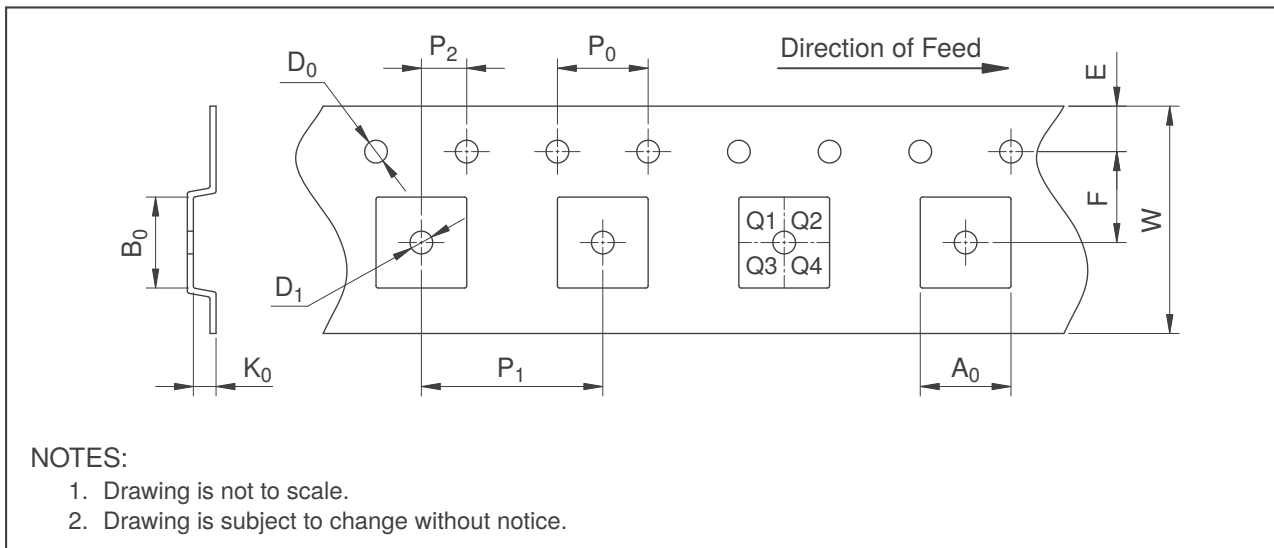
Table 12.3: QFR (3x3)-20 Package Outline Dimensions [mm]

| Dimension | Min       | Nom  | Max  |
|-----------|-----------|------|------|
| A         | 0.50      | 0.55 | 0.60 |
| A1        | 0         | 0.02 | 0.05 |
| A3        | 0.152 REF |      |      |
| b         | 0.15      | 0.20 | 0.25 |
| D         | 2.95      | 3.00 | 3.05 |
| E         | 2.95      | 3.00 | 3.05 |
| D1        | 1.60      | 1.70 | 1.80 |
| E1        | 1.60      | 1.70 | 1.80 |
| e         | 0.40 BSC  |      |      |
| L         | 0.25      | 0.30 | 0.35 |





## 12.7 Tape and Reel Specifications



*Figure 12.7: Carrier Tape Specification*

*Table 12.4: Carrier Tape Dimensions [mm]*

| Dimension      | Package |       |       |
|----------------|---------|-------|-------|
|                | WLCSP11 | DFN12 | QFN20 |
| A <sub>0</sub> | 1.35    | 3.30  | 3.30  |
| B <sub>0</sub> | 1.75    | 3.30  | 3.30  |
| K <sub>0</sub> | 0.50    | 1.10  | 0.75  |
| D <sub>0</sub> | 1.50    | 1.55  | 1.50  |
| D <sub>1</sub> | 0.60    | 1.50  | 1.55  |
| E              | 1.75    | 1.75  | 1.75  |
| F              | 3.50    | 5.50  | 5.50  |
| P <sub>0</sub> | 4.00    | 4.00  | 4.00  |
| P <sub>1</sub> | 4.00    | 8.00  | 8.00  |
| P <sub>2</sub> | 2.00    | 2.00  | 2.00  |
| W              | 8.00    | 12.00 | 12.00 |
| Pin 1 Quadrant | Q2      | Q1    | Q2    |

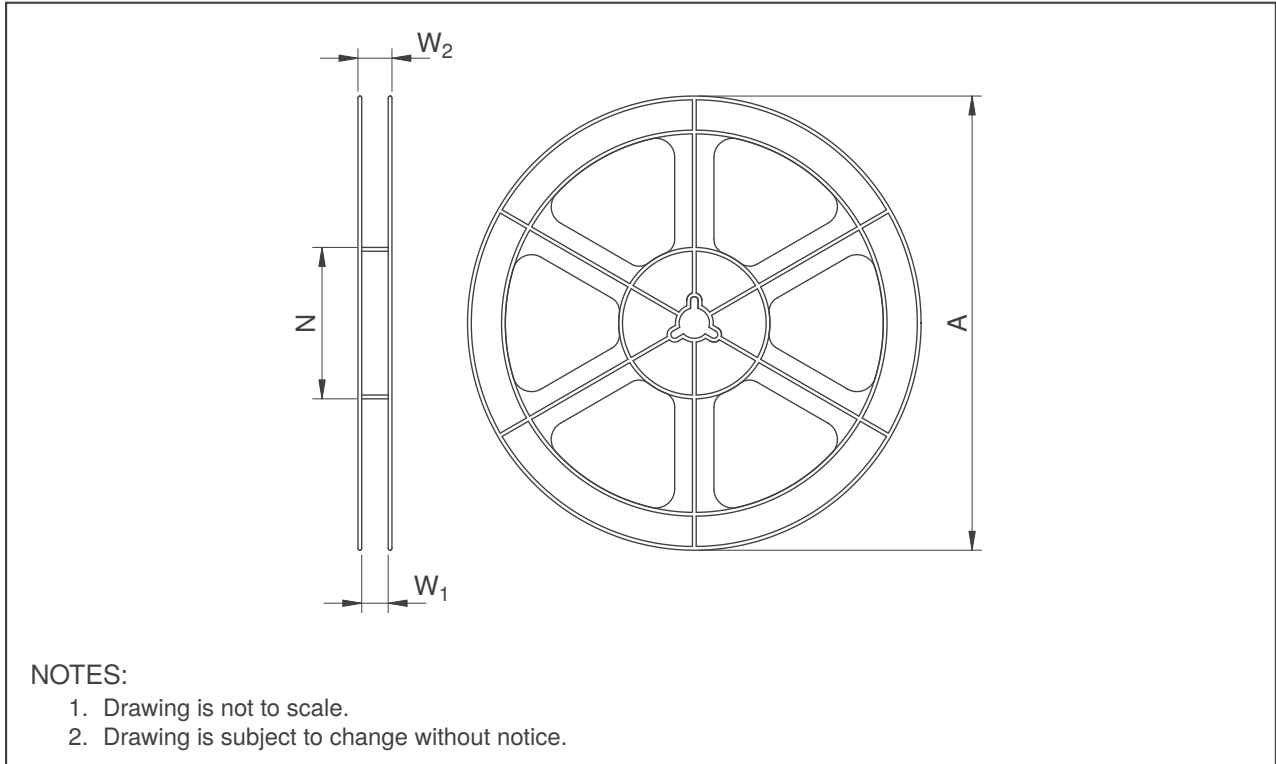


Figure 12.8: Reel Specification

Table 12.5: Reel Dimensions [mm]

| Dimension            | Package |       |       |
|----------------------|---------|-------|-------|
|                      | WLCSP11 | DFN12 | QFN20 |
| A                    | 179     | 330   | 178   |
| N                    | 55      | 100   | 60    |
| W <sub>1</sub>       | 8.4     | 12.4  | 12.4  |
| W <sub>2</sub> (Max) | 14.4    | 18.4  | 18.4  |



## A Memory Map Descriptions

**Please note:** All fields marked *Reserved* should not be modified.

### A.1 Version Information (0x00 – 0x09)

| Address     | Category                        | Name           | Order Code |     |
|-------------|---------------------------------|----------------|------------|-----|
|             |                                 |                | 100        | 200 |
| 0x00        | Application Version Information | Product Number | 1304       |     |
| 0x01        |                                 | Major Version  | 1          |     |
| 0x02        |                                 | Minor Version  | 0          | 1   |
| 0x03        |                                 | Reserved       |            |     |
| 0x04        |                                 | Reserved       |            |     |
| 0x05 - 0x09 |                                 | Reserved       |            |     |

### A.2 System Status (0x10)

| Bit                | 15       | 14 | 13           | 12        | 11       | 10           | 9         | 8        |
|--------------------|----------|----|--------------|-----------|----------|--------------|-----------|----------|
| <b>Description</b> | Reserved |    | CH1 Movement | CH1 Touch | CH1 Prox | CH0 Movement | CH0 Touch | CH0 Prox |

| Bit                | 7        | 6           | 5         | 4          | 3         | 2              | 1           | 0          |
|--------------------|----------|-------------|-----------|------------|-----------|----------------|-------------|------------|
| <b>Description</b> | Reserved | Reset Event | ATI Error | ATI Active | ATI Event | Movement Event | Touch Event | Prox Event |

#### > Bit 13-8: CHx Touch/Prox/Movement

##### For CHx Movement

- 0: CHx not in Movement
- 1: CHx in Movement

##### For CHx Touch

- 0: CHx not in Touch
- 1: CHx in Touch

##### For CHx Prox

- 0: CHx not in Prox
- 1: CHx in Prox

#### > Bit 6: Reset Event

- 0: No Reset Event occurred
- 1: Reset Event occurred

#### > Bit 5: ATI Error

- 0: No ATI Error occurred
- 1: ATI Error occurred

#### > Bit 4: ATI Active

- 0: No ATI routine active
- 1: ATI routine active

#### > Bit 3: ATI Event

- 0: No ATI Event occurred
- 1: ATI Event occurred

#### > Bit 2: Movement Event

- 0: No Movement Event occurred
- 1: Movement Event occurred

#### > Bit 1: Touch Event

- 0: No Touch Event occurred
- 1: Touch Event occurred

#### > Bit 0: Prox Event

- 0: No Prox Event occurred
- 1: Prox Event occurred



### A.3 Sensor Setup 0 (0x20, 0x30)

| Bit         | 15       | 14        | 13        | 12       | 11 | 10 | 9    | 8    |
|-------------|----------|-----------|-----------|----------|----|----|------|------|
| Description | Reserved | CalCap Rx | CalCap Tx | Reserved |    |    | CTx1 | CTx0 |

| Bit         | 7        | 6 | 5 | 4 | 3               | 2      | 1              | 0                |
|-------------|----------|---|---|---|-----------------|--------|----------------|------------------|
| Description | Reserved |   |   |   | Movement Enable | Invert | Dual Direction | Linearise Counts |

- > Bit 14: **CalCap Rx**
  - 0: CalCap Rx not selected
  - 1: CalCap Rx selected
- > Bit 13: **CalCap Tx**
  - 0: CalCap Tx not selected
  - 1: CalCap Tx selected
- > Bit 9-8: **CTxx**
  - 0: CTxx disabled
  - 1: CTxx enabled
- > Bit 2: **Movement Enable**
  - 0: Movement disabled
  - 1: Movement enabled
- > Bit 2: **Invert**
  - 0: Do not invert channel logic
  - 1: Invert channel logic
- > Bit 1: **Dual Direction**
  - 0: Single direction thresholds
  - 1: Dual direction thresholds
- > Bit 0: **Linearise Counts**
  - 0: Do not Linearise counts
  - 1: Linearise counts

### A.4 Conversion Frequency Setup (0x21, 0x31)

| Bit         | 15                          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|-----------------------------|----|----|----|----|----|---|---|
| Description | Conversion Frequency Period |    |    |    |    |    |   |   |

| Bit         | 7                             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------------------------|---|---|---|---|---|---|---|
| Description | Conversion Frequency Fraction |   |   |   |   |   |   |   |

- > Bit 15-8: **Conversion Frequency Period**
  - Range: 0 - 127
- > Bit 7-0: **Conversion Frequency Fraction**
  - Fix to 127

It is recommended to fix the *Fraction* value to 127. For capacitive sensing, please refer to the following table to determine the *Period* value for the desired conversion frequency. The *Dead Time* setting must be enabled.



Table A.1: Supported Conversion Frequency Parameters for Capacitive Sensing

| FRACTION | PERIOD | Conversion Frequency $f_{xfer}$ |
|----------|--------|---------------------------------|
| 127      | 2      | 1.75 MHz                        |
|          | 3      | 1.40 MHz                        |
|          | 5      | 1.00 MHz                        |
|          | 7      | 778 kHz                         |
|          | 12     | 500 kHz                         |
|          | 16     | 389 kHz                         |
|          | 23     | 280 kHz                         |

\* The maximum recommended conversion frequency for self-capacitive sensing is 1 MHz.

### A.5 Prox Control (0x22, 0x32)

| Bit                | 15       | 14            | 13       | 12      | 11       | 10 | 9               | 8 |
|--------------------|----------|---------------|----------|---------|----------|----|-----------------|---|
| <b>Description</b> | Reserved | 0v5 Discharge | Reserved | CS Size | Reserved |    | S/H Bias Select |   |

| Bit                | 7          | 6 | 5        | 4 | 3 | 2 | 1 | 0 |
|--------------------|------------|---|----------|---|---|---|---|---|
| <b>Description</b> | Max Counts |   | Reserved |   |   |   |   |   |

- > Bit 14: **0v5 Discharge**
  - 0: Disabled
  - 1: Enabled
- > Bit 12: **Cs Size**
  - 0: Use 40pF Cs
  - 1: Use 80pF Cs
- > Bit 9-8: **S/H Bias Select**
  - 00: 2µA
  - 01: 5µA
  - 10: 7µA
  - 11: 10µA
- > Bit 7-6: **Max Counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095 (recommended)
  - 11: 16383

### A.6 Timing Generator Control & Prox Input (0x23, 0x33)

| Bit                | 15       | 14 | 13 | 12 | 11                     | 10       | 9   | 8   |
|--------------------|----------|----|----|----|------------------------|----------|-----|-----|
| <b>Description</b> | Reserved |    |    |    | Calibration Cap Select | Reserved | Rx1 | Rx0 |

| Bit                | 7        | 6                | 5        | 4 | 3 | 2 | 1 | 0 |
|--------------------|----------|------------------|----------|---|---|---|---|---|
| <b>Description</b> | Reserved | Dead Time Enable | Reserved |   |   |   |   |   |

- > Bit 11: **Calibration Capacitor Select**
  - 0: Calibration Capacitor enabled
  - 1: Calibration Capacitor disabled
- > Bit 9-8: **Rxx**
  - 0: Rxx Disabled



- 1: Rxx Enabled
- > Bit 6: **Dead Time Enable**
  - 0: Dead Time Disabled
  - 1: Dead Time Enabled

### A.7 Inactive Rxs & Calibration Capacitor Selection (0x24, 0x34)

| Bit         | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----------|----|----|----|----|----|---|---|
| Description | Reserved |    |    |    |    |    |   |   |

| Bit         | 7                     | 6 | 5 | 4 | 3            | 2 | 1 | 0 |
|-------------|-----------------------|---|---|---|--------------|---|---|---|
| Description | Calibration Capacitor |   |   |   | Inactive Rxs |   |   |   |

- > Bit 7-4: **Calibration Capacitor**
  - Calibration Capacitor size = 0.5pF × Calibration Capacitor
  - Max value = 7 (Calibration Capacitor size = 3.5pF)
- > Bit 3-0: **Inactive Rxs**
  - Selects state of CX's when not in use
  - 0x00: Floating
  - 0x05: Bias voltage
  - 0x0A: VSS
  - 0x0F: VREG

### A.8 ATI Setup (0x25, 0x35)

| Bit         | 15                    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|-----------------------|----|----|----|----|----|---|---|
| Description | ATI Resolution Factor |    |    |    |    |    |   |   |

| Bit         | 7                     | 6 | 5 | 4 | 3        | 2        | 1 | 0 |
|-------------|-----------------------|---|---|---|----------|----------|---|---|
| Description | ATI Resolution Factor |   |   |   | ATI Band | ATI Mode |   |   |

- > Bit 15-4: **ATI Resolution Factor**
  - Range: 0-4095
- > Bit 3: **ATI Band**
  - 0: Small ATI Band
  - 1: Large ATI Band
- > Bit 2-0: **ATI Mode**
  - 000: Disabled
  - 001: Compensation Only
  - 010: ATI from Compensation Divider
  - 011: ATI from Fine Fractional Divider
  - 100: Full

### A.9 ATI Multipliers and Dividers (0x27, 0x37)

| Bit         | 15                         | 14 | 13                      | 12 | 11 | 10 | 9 | 8                            |
|-------------|----------------------------|----|-------------------------|----|----|----|---|------------------------------|
| Description | Fine Fractional Multiplier |    | Fine Fractional Divider |    |    |    |   | Coarse Fractional Multiplier |

| Bit         | 7                            | 6 | 5 | 4 | 3                         | 2 | 1 | 0 |
|-------------|------------------------------|---|---|---|---------------------------|---|---|---|
| Description | Coarse Fractional Multiplier |   |   |   | Coarse Fractional Divider |   |   |   |

- > Bit 15-14: **Fine Fractional Multiplier**



- Range: 0 - 3
- > Bit 13-9: **Fine Fractional Divider**
  - Range: 0 - 31
- > Bit 8-5: **Coarse Fractional Multiplier**
  - Range: 0 - 15
- > Bit 4-0: **Coarse Fractional Divider**
  - Range: 0 - 31

### A.10 Compensation (0x28, 0x38)

| Bit         | 15                   | 14 | 13 | 12 | 11 | 10       | 9            | 8 |
|-------------|----------------------|----|----|----|----|----------|--------------|---|
| Description | Compensation Divider |    |    |    |    | Reserved | Compensation |   |

| Bit         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Description | Compensation |   |   |   |   |   |   |   |

- > Bit 15-11: **Compensation Divider**
  - Range: 0 - 31
- > Bit 9-0: **Compensation**
  - Range: 0 - 1023

### A.11 Prox Settings (0x40, 0x50)

| Bit         | 15                 | 14 | 13 | 12 | 11 | 10                  | 9 | 8 |
|-------------|--------------------|----|----|----|----|---------------------|---|---|
| Description | Prox Debounce Exit |    |    |    |    | Prox Debounce Enter |   |   |

| Bit         | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---|---|---|---|---|---|
| Description | Prox Threshold |   |   |   |   |   |   |   |

- > Bit 15-12: **Prox Debounce Exit**
  - 0: Prox Debounce Exit disabled
  - Number of debounce conversions on Prox Exit (4-bit value)
- > Bit 11-8: **Prox Debounce Enter**
  - 0: Prox Debounce Enter disabled
  - Number of debounce conversions on Prox Enter (4-bit value)
- > Bit 7-0: **Prox Threshold**
  - 8 bit value

### A.12 Touch Settings (0x41, 0x51)

| Bit         | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|------------------|----|----|----|----|----|---|---|
| Description | Touch Hysteresis |    |    |    |    |    |   |   |

| Bit         | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|---|---|---|---|
| Description | Touch Threshold |   |   |   |   |   |   |   |

- > Bit 15-12: **Touch Hysteresis**
  - Range: 0-255
- > Bit 7-0: **Touch Threshold**
  - Range: 0-255



### A.13 Movement Settings (0x42, 0x52)

| Bit         | 15                     | 14 | 13 | 12 | 11                      | 10 | 9 | 8 |
|-------------|------------------------|----|----|----|-------------------------|----|---|---|
| Description | Movement Debounce Exit |    |    |    | Movement Debounce Enter |    |   |   |

| Bit         | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|---|---|---|---|---|---|---|
| Description | Movement Threshold |   |   |   |   |   |   |   |

- > Bit 15-12: **Movement Debounce Exit**
  - 0000: Movement Debounce Exit disabled
  - Number of debounce conversions on Movement Exit (4-bit value)
- > Bit 11-8: **Movement Debounce Enter**
  - 0000: Movement Debounce Enter disabled
  - Number of debounce conversions on Movement Enter (4-bit value)
- > Bit 7-0: **Movement Threshold**
  - 8 bit value

### A.14 Counts Filter Beta & LTA Filter Beta (0x60)

| Bit         | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----------|----|----|----|----|----|---|---|
| Description | LTA Beta |    |    |    |    |    |   |   |

| Bit         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Description | Counts Beta |   |   |   |   |   |   |   |

### A.15 LTA Fast Filter Beta & Movement Beta (0x61)

| Bit         | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|---------------|----|----|----|----|----|---|---|
| Description | Movement Beta |    |    |    |    |    |   |   |

| Bit         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Description | LTA Fast Beta |   |   |   |   |   |   |   |

### A.16 System Control (0x70)

| Bit         | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----------|----|----|----|----|----|---|---|
| Description | Reserved |    |    |    |    |    |   |   |

| Bit         | 7              | 6                  | 5                   | 4 | 3      | 2      | 1          | 0         |
|-------------|----------------|--------------------|---------------------|---|--------|--------|------------|-----------|
| Description | ATI Indication | Reference Tracking | Interface Selection |   | Reseed | Re-ATI | Soft Reset | Ack Reset |

- > Bit 7: **ATI Indication**
  - 0: ATI indication disabled
  - 1: ATI indication enabled
- > Bit 6: **Reference Tracking**
  - 0: Reference tracking disabled
  - 1: Reference tracking enabled
- > Bit 5-4: **Interface Selection**
  - 10: Standalone
  - 01: I<sup>2</sup>C Events
  - 00: I<sup>2</sup>C Streaming



- > Bit 3: **Reseed**
  - 0: No Reseed
  - 1: Trigger Reseed
- > Bit 2: **Re-ATI**
  - 0: No Re-ATI
  - 1: Trigger Re-ATI
- > Bit 1: **Soft Reset**
  - 0: No Soft Reset
  - 1: Trigger Soft Reset
- > Bit 0: **ACK Reset**
  - 0: No ACK Reset
  - 1: ACK Reset

### A.17 Event Timeouts (0x73)

| Bit         | 15                 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|--------------------|----|----|----|----|----|---|---|
| Description | Prox Event Timeout |    |    |    |    |    |   |   |

| Bit         | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|---|---|---|---|---|
| Description | Touch Event Timeout |   |   |   |   |   |   |   |

- > Bit 15-8: **Prox Event Timeout**
  - Prox Event Timeout = Prox Event Timeout × 512ms
  - Set to 0 to disable
  - Maximum value: 127
- > Bit 7-0: **Touch Event Timeout**
  - Touch Event Timeout = Touch Event Timeout × 512ms
  - Set to 0 to disable
  - Maximum value: 127

### A.18 Events Enable & SNR Boost Factor (0x74)

| Bit         | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|------------------|----|----|----|----|----|---|---|
| Description | SNR Boost Factor |    |    |    |    |    |   |   |

| Bit         | 7        | 6 | 5 | 4 | 3         | 2              | 1           | 0          |
|-------------|----------|---|---|---|-----------|----------------|-------------|------------|
| Description | Reserved |   |   |   | ATI Event | Movement Event | Touch Event | Prox Event |

- > Bit 15-8: **SNR Boost Factor**
  - Recommended values: 1-50
- > Bit 5: **ATI Error Mask**
  - 0: ATI error disabled
  - 1: ATI error enabled
- > Bit 3: **ATI Event Mask**
  - 0: ATI event disabled
  - 1: ATI event enabled
- > Bit 2: **Movement Event Mask**
  - 0: Movement event disabled
  - 1: Movement event enabled
- > Bit 1: **Touch Event Mask**
  - 0: Touch event disabled
  - 1: Touch event enabled
- > Bit 0: **Prox Event Mask**
  - 0: Prox event disabled
  - 1: Prox event enabled



### A.19 Reference Scaling (0x75)

| Bit         | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|-------------------|----|----|----|----|----|---|---|
| Description | Reference Divider |    |    |    |    |    |   |   |

| Bit         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Description | Reference Multiplier |   |   |   |   |   |   |   |

- > Bit 15-8: **Reference Divider**
  - Range: 0 - 255
- > Bit 7-0: **Reference Multiplier**
  - Range: 0 - 255

### A.20 I<sup>2</sup>C Settings (0x80)

| Bit         | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-------------|----------|----|----|----|----|----|---|---|
| Description | Reserved |    |    |    |    |    |   |   |

| Bit         | 7        | 6 | 5 | 4 | 3 | 2 | 1                 | 0                |
|-------------|----------|---|---|---|---|---|-------------------|------------------|
| Description | Reserved |   |   |   |   |   | R/W Check Disable | Stop Bit Disable |

- > Bit 1: **Read/Write Check Disable**
  - 0: Read/Write Check enable
  - 1: Read/Write Check disabled
- > Bit 0: **Stop Bit Disable**
  - 0: Stop Bit enabled
  - 1: Stop Bit disabled



## B Revision History

| Release | Date           | Changes  |
|---------|----------------|--|
| v1.0    | September 2022 | Initial release  |
| v1.1    | September 2022 | Updated reference schematics   |
| v1.2    | September 2022 | Updated naming convention for VDD  |
| v1.3    | October 2022   | Update description for reference UI and SNR boost UI   |
| v1.4    | October 2022   | Update description for reference UI  |
| v1.5    | October 2022   | Grammar correction   |
| v1.6    | November 2022  | Updated counts register memory map description<br>Updated format   |
| v1.7    | September 2023 | Updated I <sup>2</sup> C section<br>Updated force communication description<br>Updated Count Value description<br>Updated SNR Boost UI description<br>Updated memory map description<br>Updated order code information                 |
| v1.8    | April 2024     | Added program flow diagram<br>Changed report rate to sampling period<br>Moved equations from appendix to relevant sections<br>Update MCLR capacitor to 1nF<br>Updated current consumption section<br>Fixed DFN12 package pin 1 marking |
| v1.9    | February 2025  | Added QFN20 package<br>Update ordering information to list DFN12 as special order  |
| v1.10   | December 2025  | Updated formatting<br>Updated reference schematics<br>Added revision history and known issues section  |
| v1.11   | June 2026      | Minor update to block diagram.<br>Removed 1 nF capacitor on RDY pin in reference schematics.<br>Removed 1 nF capacitor on MCLR pin in MCLR Pin Diagram.<br>Corrected Digital I/O Characteristics                                       |



## C Known Issues

### Two Channel "Cross-talk"

*Versions Affected:*

v1.1 and below.

*Issue Description:*

On the IQS320, a known issue arises when two channels are active without reference tracking and oversampling is enabled by setting the SNR boost factor larger than 1. If one channel automatically triggers an ATI (due to a timeout or because it drifts out of the ATI band), the second channel behaves incorrectly. Only a single sample is captured during the ATI instead of accumulating the expected set of samples.

*Recommended Workaround*

It is recommended to ignore events on the other channel during the ATI routine or simply disable the oversampling by setting the SNR boost factor to 1.



## Contact Information

|                         | South Africa (Headquarters)                       | China  |
|-------------------------|---|--|
| <b>Physical Address</b> | 1 Bergsig Avenue<br>Paarl<br>7646<br>South Africa | Room 501A, Block A<br>T-Share International Centre<br>Taoyuan Road, Nanshan District<br>Shenzhen, Guangdong, PRC |
| <b>Tel</b>              | +27 21 863 0033                                   | +86 755 8303 5294<br>ext 808   |
| <b>Email</b>            | info@azoteq.com                                   | info@azoteq.com  |

|                         | USA   | Taiwan  |
|-------------------------|---|---|
| <b>Physical Address</b> | 7000 North Mopac Expressway<br>Suite 200<br>Austin<br>TX 78731<br>USA | Xintai 5th Road, Sec. 1<br>No. 99, 9F-12C<br>Xizhi District<br>221416 New Taipei City<br>Taiwan |
| <b>Tel</b>              | +1 512 538 1995   | +886 932 219 444  |
| <b>Email</b>            | info@azoteq.com   | info@azoteq.com   |

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