



ProxSense[®] IQS259 Datasheet

9-Channel Mutual Capacitive Touch and Proximity Sensor with I²C compatible communication interface

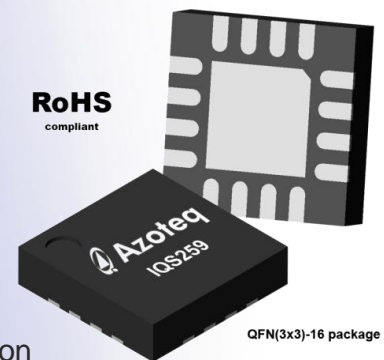
Unparalleled Features

- ☞ **Automatic Tuning Implementation (ATI)** - Automatic tuning for optimal operation in various environments & compensation against sensitivity reducing objects
- ☞ **Internal Capacitor Implementation (ICI)** – Reference capacitor on-chip
- ☞ **Small QFN(3x3)-16** outline with minimal external components

The **IQS259** ProxSense[®] IC is a fully integrated 9-channel mutual capacitive touch and proximity sensor with market leading sensitivity and automatic tuning to the sense electrodes. The **IQS259** provides a cost effective implementation in a small outline package. The device is ready for use in a large range of applications while the 3-wire I²C interface provides full control to a host MCU.

Main Features

- ☞ 9-Channel input device
- ☞ Proximity & Touch on each channel
- ☞ I²C[™] compatible data output
- ☞ ATI: Automatic tuning to optimum sensitivity
- ☞ Supply Voltage: 1.8V to 3.6V
- ☞ Low Power Operation (Sub 5uA Low Power)
- ☞ Event-driven (Event Mode) or continuous-data I²C operation
- ☞ Large proximity detection range
- ☞ Automatic drift compensation
- ☞ Development tools available (Software and USB dongles)
- ☞ Internal voltage regulator and reference capacitor (minimal external components required)
- ☞ Small outline QFN(3x3)-16 pin package



Applications

- ☞ White goods and appliances
- ☞ Office equipment, toys, sanitary ware
- ☞ Proximity detection that enables backlighting activation (Patented)
- ☞ Wake-up from standby applications
- ☞ Replacement for electromechanical switches and keypads
- ☞ GUI trigger and GUI control proximity detection
- ☞ Electronic Keypads or Pin pads

Available options

T_A	QFN(3x3)-16
-40°C to 85°C	IQS259



Contents

FUNCTIONAL OVERVIEW	4
1 INTRODUCTION	4
1.1 APPLICABILITY.....	4
2 ANALOGUE FUNCTIONALITY	4
3 DIGITAL FUNCTIONALITY	4
4 HARDWARE CONFIGURATION	5
4.1 IQS259 PIN-OUT.....	5
FIGURE 4.1 IQS259 PIN LAYOUT.....	5
TABLE 4.1 IQS259 PIN-OUTS.....	5
4.2 REFERENCE DESIGN.....	6
FIGURE 4.2 IQS259 REFERENCE DESIGN.....	6
4.3 POWER SUPPLY AND PCB LAYOUT.....	6
4.4 DESIGN RULES FOR HARSH EMC ENVIRONMENTS.....	7
4.5 HIGH SENSITIVITY.....	7
5 USER CONFIGURABLE OPTIONS	8
5.1 CONFIGURING OF DEVICES.....	8
FIGURE 5.1 IQS259 SETUP WINDOW.....	8
5.2 ACTIVE CHANNELS.....	8
FIGURE 5.2 IQS259 CHANNEL MAPPING.....	8
5.3 PROXIMITY THRESHOLD.....	9
5.4 TOUCH THRESHOLD.....	9
5.5 HALT TIMES.....	9
5.6 AC FILTER.....	10
5.7 POWER MODES.....	10
5.7.1 LP Modes.....	10
FIGURE 5.3 IQS259 CHARGE CYCLE TIMING ($T_{SAMPLE} = LP_{VALUE} \times 16MS$).....	10
5.7.2 Turbo Mode.....	10
5.8 ATI METHOD.....	11
5.9 BASE VALUE.....	11
5.10 TARGET VALUE.....	11
5.11 CHARGE TRANSFER SPEED.....	11
5.12 ADDITIONAL FEATURES.....	11
5.12.1 Noise Detect.....	11
5.12.2 Halt Charge.....	12
5.12.3 Distributed Proximity.....	12
5.12.4 Force Halt.....	12
5.12.5 CTX / CRX Float.....	12
6 PROXSENSE® MODULE	13
6.1 CHARGE TRANSFER CONCEPT.....	13
6.2 RATE OF CHARGE CYCLES.....	13
6.2.1 Boost Power rate.....	13
FIGURE 6.1 IQS259 CHARGE SEQUENCE.....	14
6.2.2 Low Power rate.....	14
6.3 TOUCH REPORT RATE.....	14
6.4 LONG TERM AVERAGE.....	15
6.5 DETERMINE TOUCH OR PROX.....	15
6.6 ATI.....	15
6.6.1 ATI Sensitivity.....	15
6.6.2 ATI Target.....	16
6.6.3 ATI Base (Multiplier).....	16
6.6.4 Re-ATI.....	16
6.6.5 Reseed.....	16
6.6.6 Alternative ATI.....	17
7 COMMUNICATION	18



7.1	I ² C SUB-ADDRESS.....	18
7.1.1	<i>External sub-address selection</i>	18
TABLE 7.1	I ² C SUB-ADDRESS EXTERNAL SELECTION.....	18
7.1.2	<i>Internal sub-address selection</i>	18
TABLE 7.2	I ² C SUB-ADDRESS INTERNAL SELECTION.....	18
7.2	EVENT MODE.....	18
7.3	RDY HAND-SHAKE ROUTINE.....	19
7.4	I ² C SPECIFIC COMMANDS	19
7.4.1	<i>Show Reset</i>	19
7.4.2	<i>WDT disable</i>	19
7.4.3	<i>Timeout Disable</i>	19
7.4.4	<i>Default Comms Pointer</i>	19
7.5	I ² C R/W SPECIFICS	19
7.6	I ² C I/O CHARACTERISTICS.....	19
TABLE 7.3	IQS259 I ² C INPUT VOLTAGE.....	19
TABLE 7.4 PROVIDES THE OUTPUT VOLTAGE LEVELS OF THE IQS259 DEVICE DURING I²C COMMUNICATION.		
TABLE 7.4	IQS259 I ² C OUTPUT VOLTAGE.....	19
8	RF NOISE	20
8.1	RF NOISE DETECTION	20
8.1.1	<i>RF Detector Sensitivity</i>	20
8.2	RF NOISE IMMUNITY	20
8.2.1	<i>Notes for layout:</i>	20
9	IQS259 MEMORY MAP	21
9.1	MEMORY REGISTERS	21
TABLE 9.1	IQS259 MEMORY REGISTERS.....	21
9.2	MEMORY REGISTERS DESCRIPTION	22
9.2.1	<i>Device Information</i>	22
9.2.2	<i>Device Specific Data</i>	22
9.2.3	<i>Proximity Status Bytes</i>	23
9.2.4	<i>Touch Status Bytes</i>	23
9.2.5	<i>Halt Bytes</i>	24
9.2.6	<i>Channel Number</i>	24
9.2.7	<i>Count (CS) Values</i>	24
9.2.8	<i>Long-Term Averages</i>	25
9.2.9	<i>Device Settings</i>	25
10	IQS259 OTP OPTIONS	39
10.1	USER SELECTABLE OTP OPTIONS	39
TABLE 10.1	USER SELECTABLE OTP OPTIONS : BANK3	39
11	SPECIFICATIONS	40
11.1	ABSOLUTE MAXIMUM SPECIFICATIONS.....	40
TABLE 11.1	IQS259 GENERAL OPERATING CONDITIONS	40
TABLE 11.2	START-UP AND SHUT-DOWN SLOPE CHARACTERISTICS.....	40
TABLE 11.3	EVENT MODE RESPONSE TIMES	41
TABLE 11.4	REPETITIVE TOUCH RATES	41
12	PACKAGE INFORMATION	42
12.1	IQS259 PACKAGE DIMENSIONS.....	42
FIGURE 12.1	QFN(3X3)–16 PACKAGE DIMENSIONS	42
12.2	RECOMMENDED PCB FOOTPRINT	42
FIGURE 12.1	IQS259 RECOMMENDED PCB FOOTPRINT	42
13	DEVICE MARKING	43
14	ORDERING INFORMATION	43
15	CONTACT INFORMATION	44



Functional Overview

1 Introduction

The **IQS259** is a nine channel mutual capacitive proximity and touch sensor featuring an internal voltage regulator and reference capacitor (Cs).

The device has six dedicated pins for the connection of the sense electrodes, which consist of three receivers, and three transmitters. Three pins are used for serial data communication through the I²C™ compatible protocol, including an optional RDY pin.

The device automatically tracks slow varying environmental changes via various filters, detects noise and is equipped with an Automatic Tuning Implementation (ATI) to adjust the device for optimal sensitivity.

1.1 Applicability

All specifications, except where specifically mentioned otherwise, provided by this datasheet are applicable to the following ranges:

- Temperature -40°C to +85°C
- Supply voltage (V_{DDHI}) 1.8V to 3.6V

2 Analogue Functionality

CRX and CTX electrodes are arranged in a suitable configuration that results in a mutual capacitance (C_m) between the two electrodes. CTX is charged up to a set positive potential during a charge cycle which results in a negative charge buildup at CRX.

The resulting charge displacement is then measured within the IQS259 device

through a charge transfer process that is periodically initiated by the digital circuitry. The capacitance measurement circuitry makes use of an internal reference capacitor C_s and voltage reference (VREF).

The measuring process is referred to as a conversion and consists of the discharging of C_s and C_x capacitors, the charging of C_x and then a series of charge transfers from C_x to C_s until a trip voltage is reached. The number of charge transfers required to reach the trip voltage is referred to as the Counts (CS) value.

The analogue circuitry further provides functionality for:

- Power On Reset (POR) detection.
- Brown Out Detection (BOD).
- Internal regulation provides for accurate sampling.

3 Digital Functionality

The digital processing functionality is responsible for:

- Managing BOD and WDT events.
- Initiation of conversions at the selected rate.
- Processing of CS and execution of algorithms.
- Monitoring and execution of the ATI algorithm.
- Signal processing and digital filtering.
- Detection of PROX and TOUCH events.
- Managing outputs of the device.
- Managing serial communications.



4 Hardware Configuration

4.1 IQS259 Pin-out

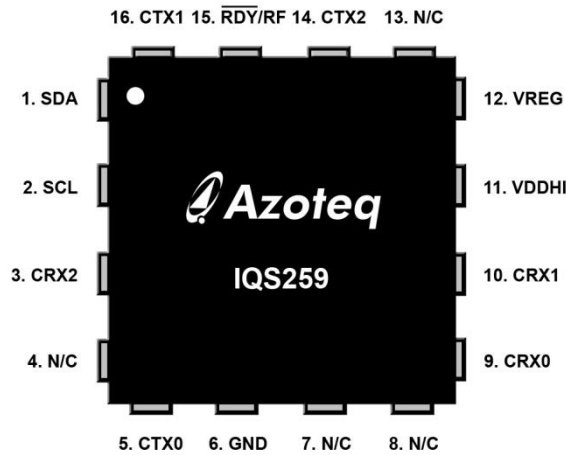


Figure 4.1 IQS259 Pin layout

Table 4.1 IQS259 Pin-outs.

IQS259 Pin-out			
Pin	Name	Type	Function
1	SDA	Digital	Serial Data
2	SCL	Digital	Serial Clock
3	CRX2	Analogue	Receive Electrode
4	N/C	-	Not Connected
5	CTX0	Transmitter	Transmit Electrode
6	GND	Supply Input	GND Reference
7	N/C	-	Not Connected
8	N/C	-	Not Connected
9	CRX0	Analogue	Receive Electrode
10	CRX1	Analogue	Receive Electrode
11	VDDHI	Supply Input	Supply Voltage Input
12	VREG	Analogue Output	Internal Regulator Pin (connect 1µF capacitor)
13	N/C	-	Not connected
14	CTX2	Transmitter	Transmit electrode
15	RDY/RF	Digital Output / Analogue receiver	Serial Ready Interrupt / RF receiver
16	CTX1	Transmitter	Transmit electrode



4.2 Reference Design

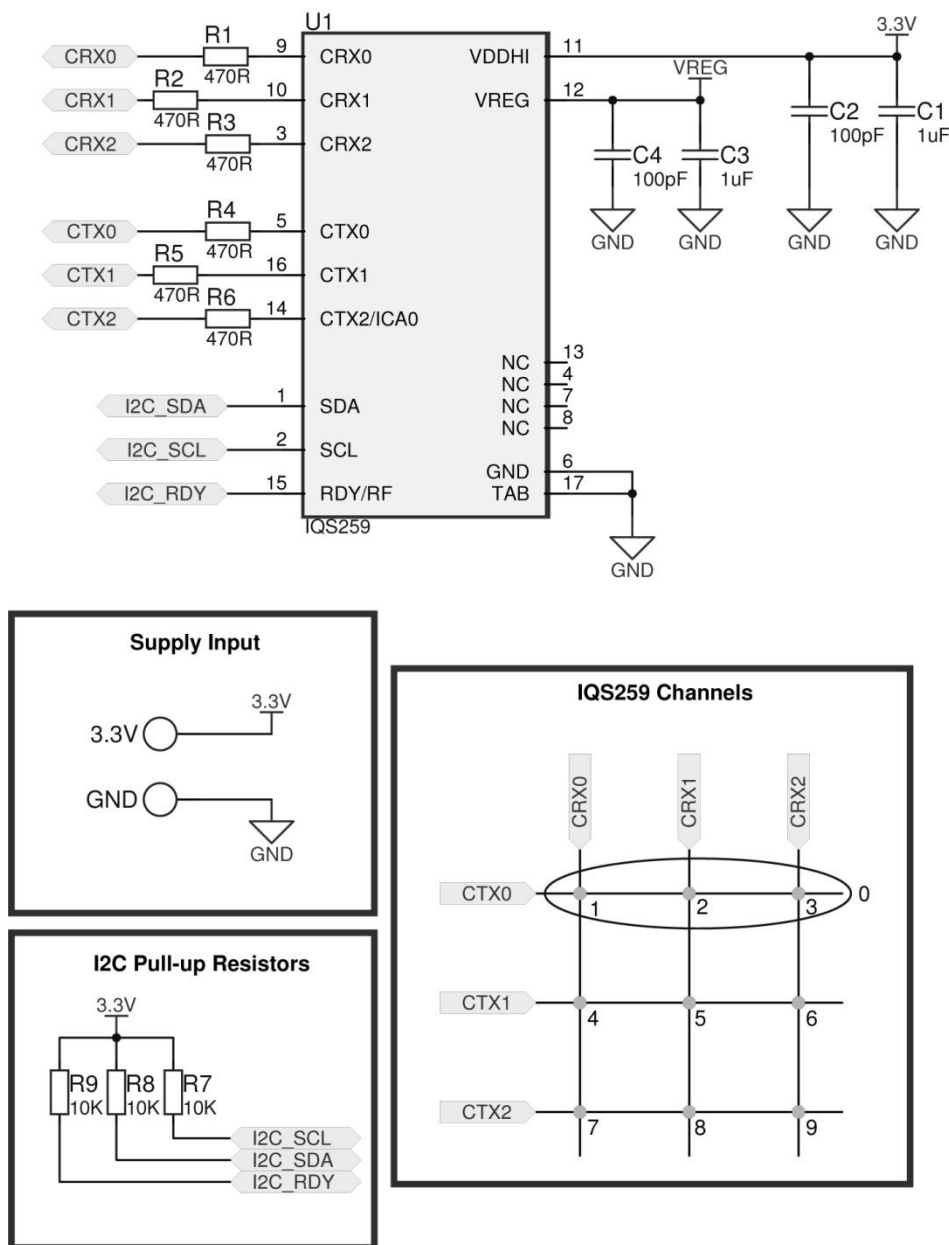


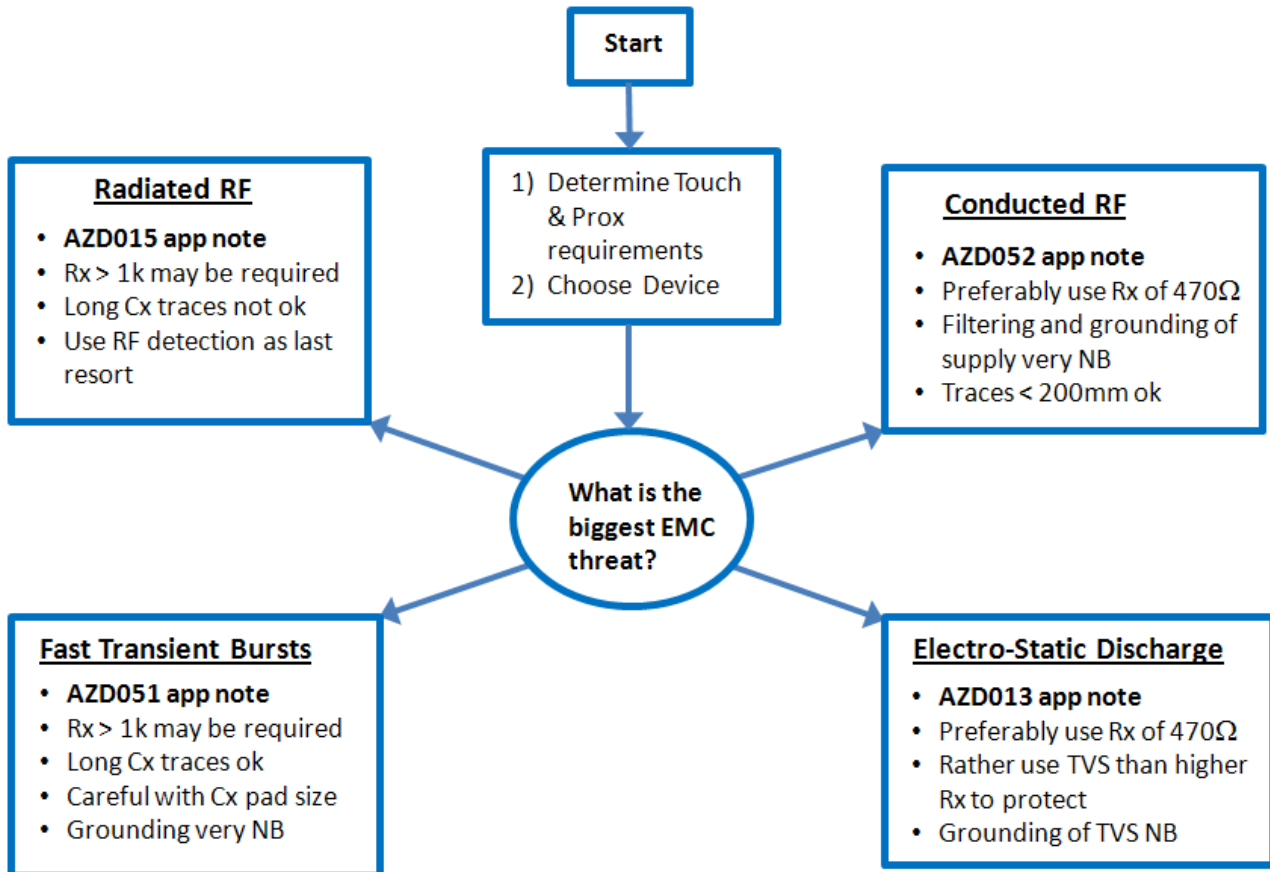
Figure 4.2 IQS259 Reference Design.

4.3 Power Supply and PCB Layout

Azoteq IC's provide a high level of on-chip hardware and software noise filtering and ESD protection (refer to application note "AZD013 – ESD Overview"). Designing PCB's with better noise immunity against EMI, FTB and ESD in mind, it is always advisable to keep the critical noise suppression components like the de-coupling capacitors and series resistors in **Figure 4.2** as close as possible to the IC. Always maintain a good ground connection and ground pour underneath the IC. For more guidelines please refer to the relevant application notes as mentioned in **Section 4.4**.



4.4 Design Rules for Harsh EMC Environments



➤ *Applicable application notes: AZD013, AZD015, AZD051, AZD052.*

4.5 High Sensitivity

Through patented design and advanced signal processing, the device is able to provide extremely high sensitivity to detect proximity. This enables designs to detect proximity at distances that cannot be equaled by most other products. When the device is used in environments where high levels of noise or floating metal objects exist, a reduced proximity threshold is proposed to ensure reliable functioning of the sensor. The high sensitivity also allows the device to sense through overlay materials with low dielectric constants, such as wood or porous plastics.

For more guidelines on the layout of capacitive sense electrodes, please refer to application note **AZD008**, available on the Azoteq web page: www.azoteq.com.



5 User Configurable Options

The **IQS259** requires a configuration setup by a master/host controller or MCU. The user needs to select the number of channels and corresponding touch and proximity thresholds.

5.1 Configuring of Devices

At power-up the **IQS259** will enter an initialization state (after $t_{POR} \approx 12ms$) with a setup window as shown in **Figure 5.1**, during which communication with the device must be established (START condition) within a time of $t_{START} < t_{COMMS}$ (see **Section 7.4.3**). In this state the various settings in the device memory map can be configured as required by the user. Once the appropriate settings have been setup, the master needs to generate a STOP condition after which charge transfers will commence according to the setup in the device memory map.

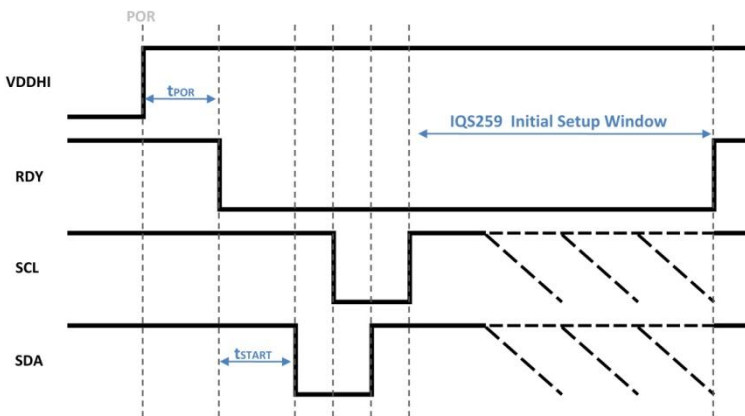


Figure 5.1 IQS259 Setup Window

However, if the initial setup window is missed, the device can be initialized by the host MCU during the next communications window, by performing a RDY (ready) hand-shake routine. (See **Section 7.3**)

Please refer to Application Note: “**AZD064: IQS259 Communication Interface Guideline**” for additional I²C information.

5.2 Active Channels

The **IQS259** can be configured to have up to 9 active touch/proximity channels (CH1-CH9) with one additional proximity channel (CH0). By default CH0 is a distributed proximity channel, comprised of charging CH1-CH3 simultaneously. However, each touch channel also has an independent proximity indication bit, which can be accessed in the **PROX_STAT** registers (0x31, 0x32).

The desired channels can be enabled or disabled in the **CHAN_ENABLE** registers (0xEC, 0xED).

Figure 5.2 illustrates the **IQS259** channels mapped to the respective transmit (CTX) and receive (CRX) sense electrodes.

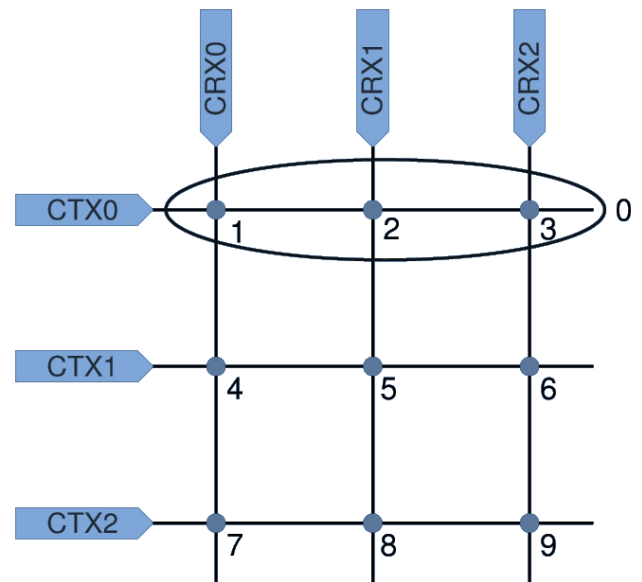


Figure 5.2 IQS259 Channel Mapping



5.3 Proximity Threshold

A proximity threshold for each channel can be selected by the designer to obtain the desired proximity sensitivity and is selectable between 1 (most sensitive) and 254 (least sensitive). These threshold values (i.e. 1-254) are specified in current samples (CS) or counts. (See **Section 6.5**) Proximity thresholds (between the specified limits) are individually selectable for channels 0 to 3 and combined for channels 4 to 9.

Proximity thresholds can be setup in the **PROX_THx** registers (0xDA to 0xDE).

Note: The **IQS259** has default proximity thresholds of $P_{TH} = 4$ for all channels. Selecting a proximity threshold greater than the touch threshold for a given channel is not recommended (See **Section 5.5**).

5.4 Touch Threshold

A touch threshold for each channel can be selected by the designer to obtain the desired touch sensitivity and is selectable between 1/255 (most sensitive) to 254/255 (least sensitive). The touch threshold is calculated as a fraction of the Long-Term Average (LTA) given by,

$$T_{TH} = \frac{x}{255} \times LTA$$

With lower target values (therefore lower LTA's) the touch threshold will be lower and vice versa. Please refer to **Sections 6.4 to 6.6**.

Individual touch thresholds can be set for each channel (excl. CH0) in the **TOUCH_THx** registers (0xDF to 0xE7).

Note: The **IQS259** has a default touch threshold of $32/255 \times LTA$ for all 9 channels.

5.5 Halt times

The Halt Timer is started when a proximity or touch event occurs and is restarted when that event is removed or reoccurs. When a proximity condition occurs on any of the channels, the LTA value for that channel will be "halted", thus its value will be kept fixed, until the proximity event is cleared, or the halt timer reaches the halt time. The halt timer will count to the selected halt time (t_{HALT}), which can be configured in the **PROX_SETTINGS2** register (0xEA, bit1:0) and if the timer expires, all outputs will be cleared.

It is possible that the CS ("Current Sample" or "Count" value) could be outside the ATI boundary (ATI Target +/- 12.5%) when the timer expires, which will cause the device to perform a re-ATI event on that channel.

The designer needs to select a halt timer value (t_{HALT}) to best accommodate the required application:

- **20 seconds** : Halt LTA for 20s after the last proximity or touch event.
- **40 seconds** : Halt LTA for 40s after the last proximity or touch event.
- **Never** : Never halt LTA.
- **Always** : Always halt LTA.

* *With the 'Never' option, the detection of a proximity or touch event will not halt the LTA and the LTA will adjust towards the CS value until the CS value is reached. The touch and proximity output of a channel will thus be cleared automatically when the difference between the LTA and CS is less than the specified threshold value.*



5.6 AC Filter

The AC filter can be implemented (**CH0 only**) to provide better stability of current samples (CS) or count measurements in electrically noisy environments.

The AC filter also enforces a longer minimum sample time for detecting proximity events on CH0, which will result in a slower response rate when the device enters low power modes. The AC filter can be disabled by setting the ACF_disable bit in the **PROX_SETTINGS2** register (0xEA, bit4).

Note: The AC filter reduces touch report rate and hence cannot be imposed on CH1-CH9.

5.7 Power Modes

5.7.1 LP Modes

The **IQS259** IC has a wide range of configurable low power modes, specifically designed to reduce current consumption for low power and battery applications.

The power modes are implemented around the occurrence of a charge cycle every t_{SAMPLE} seconds. The value of t_{SAMPLE} is determined by the custom (LP_{value}) value between 1 and 256 in the **LOW_POWER**

register (0xEE, bit7:0) multiplied by 16ms. Boost Power (BP) mode is set by default, with the **LOW_POWER** value = 0.

Lower sampling frequencies typically yield significant lower power consumption (but also decreases the response time)

NOTE: While in any power mode the device will zoom to Boost Power (BP) mode whenever the condition $(CS - LTA) > PROX_TH$ or $TOUCH_TH$ holds, indicating a possible proximity or touch event. This improves the response time. The device will remain in BP for t_{ZOOM} and then return to the selected power mode. The Zoom function allows reliable detection of events with current samples being produced at the BP rate. The LP charge cycle timing is illustrated in **Figure 5.3**. The Zoom bit in the **SYSFLAGS** register (0x10, bit0) will be set when BP mode is active.

Note: During LP modes, CH0 is forced enabled to wake the device upon proximity events. Also, during LP only CH0 is active. However, after the device has zoomed in to BP mode, charging of CH0 is NOT automatically disabled again. This requires the use of at least CH1, CH2 or CH3 in the intended application.

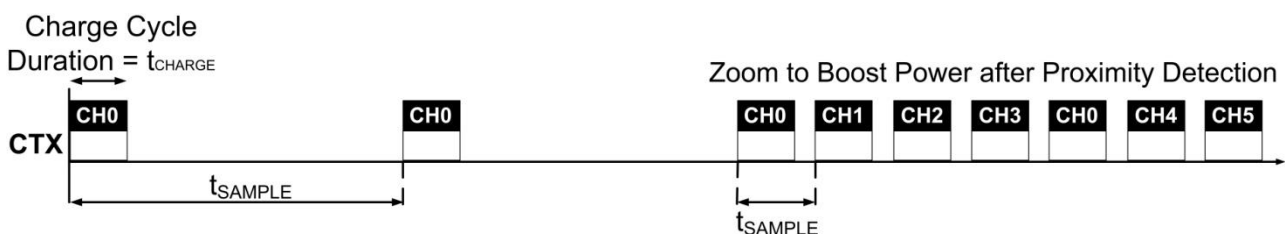


Figure 5.3 IQS259 Charge Cycle Timing ($t_{SAMPLE} = LP_{value} \times 16ms$)

5.7.2 Turbo Mode

Setting the Turbo Mode bit in the **PROX_SETTINGS1** register (0xE9, bit5) will enable the **IQS259** device to perform conversions (charge transfers) as fast

processing and communication allows, thereby maximizing detection speeds, but also increasing current consumption.



5.8 ATI Method

The **IQS259** can be set up to perform sensor calibration in two ways: Full ATI and Partial ATI, configurable in the **PROX_SETTINGS0** register (0xE8).

In Full ATI mode, the device automatically selects the multipliers through the ATI algorithm to setup the **IQS259** as close as possible to its default sensitivity for the environment where it was placed.

The user can however, select Partial ATI, and set the multipliers to a pre configured value. This will cause the **IQS259** to only calculate the compensation (not the compensation and multipliers as in Full ATI), which allows the freedom to make the **IQS259** more or less sensitive for its intended environment of use. The Partial ATI also reduces start-up and re-ATI times. (Refer to **Section 6.6**)

5.9 Base Value

The **IQS259** has the option to individually change the base value of each channel during the ATI algorithm. Depending on the application, this provides the user with another option to select the sensitivity of the **IQS259** without changes in the hardware (CRX/CTX sizes and routing, etc).

By setting the base value bits in the **MULT_CHx** registers (0xD0 to 0xD9, bit7:6), the base value can be selected to be **50, 100, 200** (default) or **250**.

The base value influences the overall sensitivity of the channel and establishes a base count from where the ATI algorithm starts executing. A lower base value will typically result in a higher sensitivity of the respective channel. (Refer to **Section 6.6.3**)

5.10 Target Value

The default target values of the **IQS259** are 1024 for the proximity channel and 512 for the touch channels. However, for some applications, a more sensitive device and higher target is required. (Refer to **Section 6.6.2**)

The target values for CH0 and CH1-9 are calculated by multiplying the value in the respective **TARGET_CNTx** registers (0xC4 and 0xC5) by 8.

Example: CH0 target = **TARGET_CNT0**] x 8
= 128 x 8 = 1024.

5.11 Charge Transfer Speed

The frequency at which charge cycles are performed can be adjusted by the Charge Xfer Speed bits in the **PROX_SETTINGS3** register (0xEB, bit1:0).

Adjusting the charge transfer speed will change the charge cycle duration (t_{CHARGE}) as shown in **Figure 5.3**.

The charge transfer frequency is a fraction of the main oscillator (FOSC =4MHz) and can be set at **1MHz** (default), **500kHz**, **250kHz** or **125kHz**.

Higher charge transfer speeds are preferred for applications that require increased immunity against aqueous substances.

5.12 Additional Features

5.12.1 Noise Detect

The **IQS259** has advanced integrated immunity to RF noise sources such as GSM cellular telephones, DECT, Bluetooth and WIFI devices.

Noise detection can be enabled by setting the Noise Detect On bit in the **PROX_SETTINGS1** register (0xE9, bit3).



Connecting a suitable RF antenna and enabling the RF noise detection functionality, will allow the device to identify RF interference and disregard any changes in CS values, blocking changes in touch or proximity status bits if RF noise is detected.

Design guidelines should however be followed to ensure the best noise immunity. Please refer to **Section 8**.

5.12.2 Halt Charge

Setting the Halt Charge bit in the [PROX_SETTINGS1](#) register (0xE9, bit4), will stop all conversions.

This function is typically useful for ultra low power requirements, where the [IQS259](#) can be controlled by a host MCU and does not require wake-up on proximity or touch events.

5.12.3 Distributed Proximity

The [IQS259](#) is setup to charge the proximity channel (i.e. CH0) by default with the charge being distributed between the CTX0, CRX0, CRX1 and CRX2 electrodes. This results in charging channels 1, 2 and 3 simultaneously.

In certain applications the combined capacitive load on the three distributed mutual capacitive channels may exceed the allowable range, causing the ATI algorithm to not reach the intended target value. In such cases, the distributed proximity channel can be changed to function as a self capacitance electrode, with the capacitance distributed over the CRX0, CRX1 and CRX2 electrodes only.

This can be done by setting the Distributed Channel SELF bit in the [PROX_SETTINGS3](#) register (0xEB, bit2).

5.12.4 Force Halt

The Force Halt bit in the [PROX_SETTINGS2](#) register (0xEA, bit5) can be set to halt all current LTA values and prevent them from being adjusted towards the CS values.

Setting this bit overrides all filter halt settings and prevents the device from performing re-ATI events in cases where the CS values persist outside the ATI boundaries for extended periods of time.

The Force Halt can also be used to manually halt all channels LTA's upon detection of proximity on CH0, disabling CH0 for a specified time and processing the active touch channels at a faster rate. The Force Halt condition will thus prevent desensitized touch channels. This method may be used for "touch only" type applications, but care should be taken to avoid stuck proximity conditions in mobile devices.

5.12.5 CTX / CRX Float

During the charge transfer process (see [Figure 6.1](#)), the channels that are not being processed during the current cycle, are effectively grounded to decrease the effects of noise-coupling between the sense electrodes.

Selecting the "Float CTX" and/or "Float CRX" option, will thus result in the non-current channels to float (i.e. not grounded) during the charge cycle of the current channel. The floating options can be enabled by setting the respective bits in the [PROX_SETTINGS1](#) register (0xE9, bit7:6).



6 ProxSense® Module

The **IQS259** contains a ProxSense® module that uses patented technology to provide detection of proximity and touch conditions on numerous sensing lines.

The ProxSense® module is a combination of hardware and software, based on the principles of charge transfer measurements.

6.1 Charge Transfer Concept

On ProxSense® devices like the **IQS259**, capacitance measurements are taken with a charge transfer process that is periodically initiated.

For mutual capacitive sensing, the device measures the capacitance between 2 electrodes referred to as the transmitter (CTX) and receiver (CRX).

The measuring process is referred to as a charge transfer cycle and consists of the following:

- Discharging of an internal sampling capacitor (Cs) and the electrode capacitors (mutual: CTX & CRX) on a channel.
- charging of CTX's connected to the channel
- and then a series of charge transfers from the CRX's to the internal sampling capacitors (Cs), until the trip voltage is reached.

The number of charge transfers required to reach the trip voltage on a channel is referred to as the Current Sample (**CS**) or Count value.

The device continuously repeats charge transfers on the sense electrodes connected to the CRX pins. For each channel a Long Term Average (**LTA**) is calculated (12 bit unsigned integer values).

The count (CS) values (12 bit unsigned integer values) are processed and compared to the LTA to detect Touch and Proximity events.

For more information regarding capacitive sensing, refer to the application note: "**AZD004 – Azoteq Capacitive Sensing**".

Please note: Attaching scope probes to the CTX/CRX pins will influence the capacitance of the sense electrodes and therefore the related CS values of those channels. This will have an instant effect on the CS measurements.

6.2 Rate of Charge Cycles

The **IQS259** samples its channels in 10 timeslots. The charge sequence (as measured on the receive electrodes) is shown in **Figure 6.1**, where CH0 is the Proximity channel, which charges before each set of 3 touch channels.

The charging of CH0 comprises the simultaneous charging of the three receive electrodes (CRX0, CRX1 and CRX2) in conjunction with one transmit electrode (CTX0), thus realising a distributed load mutual capacitive sense electrode. Refer to **Figure 5.2** for **IQS259** channel numbering.

6.2.1 Boost Power rate

With the **IQS259** zoomed to Boost Power (BP) mode, the sense channels are charged at a fixed sampling period (t_{SAMPLE}) per channel. This is done to ensure regular samples for processing of results.

It is calculated as each channel having a time ($t_{\text{SAMPLE}} = \text{charge period } (t_{\text{CHARGE}}) + \text{computation time} + \text{comms time}$) of approximately $t_{\text{SAMPLE}} = 6.9\text{ms}$. Thus the time between consecutive samples on a specific channel (t_{CH}) will depend on the



number of enabled channels, the charge transfer speed and the length of communication between the **IQS259** and the host MCU.

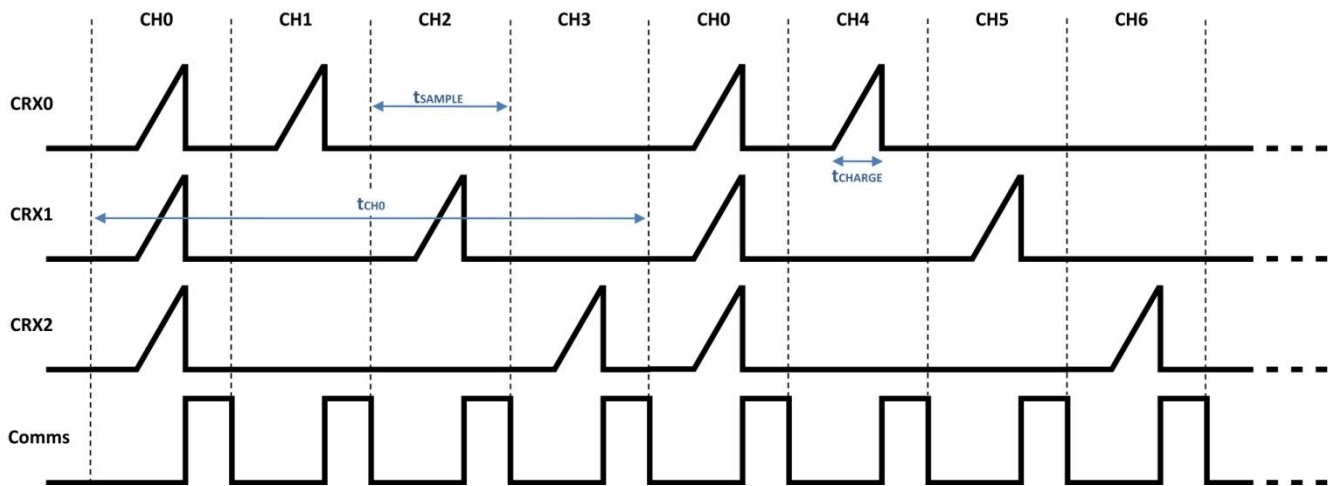


Figure 6.1 IQS259 Charge Sequence

6.2.2 Low Power rate

A wide range of low current consumption charging modes is available on the **IQS259**.

In any Low Power (LP) mode, there will be an applicable low power time (t_{LP}). This is determined by the **LOW_POWER** register (0xEE). The value written into this register multiplied by 16ms will yield the LP time (t_{LP}).

With the detection of an undebounced proximity event the IC will zoom to BP mode, allowing a very fast reaction time for further possible touch / proximity events.

During any LP mode, only CH0 (forced enabled) will be consecutively charged every T_{LP} . The LP to BP charge timing is illustrated in **Figure 5.3**.

If a low power rate is selected through the **LOW_POWER** register and charging is not in the zoomed state (BP mode), the Zoom bit (SYSFLAGS register) will be cleared.

Please refer to **Section 5.7**.

6.3 Touch report Rate

During Boost Power (BP) mode, the touch report rate of the **IQS259** device depends on the charge transfer frequency, the number of channels enabled and the length of communications performed by the host MCU or master device.

Several factors may influence the touch report rate:

- **Enabled channels:** Disabling channels (especially CH0 which has a higher target value and is charged more frequently) that are not used will not only increase the touch report rate, but will also reduce the device's current consumption.
- **Turbo Mode:** See **Section 5.7.2**
- **Target Values:** Lower target values requires shorter charge transfer periods (t_{CHARGE}), thus reducing the overall sampling period (t_{SAMPLE}) of



each channel and increasing the touch report rate.

- **Charge Transfer Speed:** Increasing the charge transfer frequency will reduce the conversion period (t_{CHARGE}) and increase the touch report rate.

6.4 Long Term Average

The Long-term Average (LTA) filter can be seen as the baseline or reference value. The LTA is calculated to continuously adapt to any environmental drift. The LTA filter is calculated from the CS value for each channel. The LTA filter allows the device to adapt to environmental (slow moving) changes/drift. Actuation (Touch or Prox) decisions are made by comparing the CS value with the LTA reference value.

The 12bit LTA value for the indicated active channel (`ACT_CHAN` register [0x3D]) is contained in the `LTA_HI` and `LTA_LO` registers (0x83 and 0x84).

Please refer to **Section 5.5** for LTA Halt Times.

6.5 Determine Touch or Prox

An event is determined by comparing the CS value with the LTA. Since the CS reacts differently when comparing the self- with the mutual capacitance technology, the user should consider only the conditions for the technology used.

An event is recorded if:

- Self: $CS < LTA - \text{Threshold}$
- Mutual: $CS > LTA + \text{Threshold}$

Threshold can be either a Proximity or Touch threshold, depending on the current channel being processed.

Note that a proximity condition will be forced enabled on a certain channel if a touch condition exists on that channel, even if the P_{TH} is greater than the T_{TH} .

Please refer to **Section 5.3** and **5.4** for proximity and touch threshold selections.

6.6 ATI

The **Automatic Tuning Implementation (ATI)** is a sophisticated technology implemented on the new ProxSense® series devices. It allows for optimal performance of the devices for a wide range of sense electrode capacitances, without modification or addition of external components.

The ATI allows the tuning of two parameters, an ATI Multiplier and an ATI Compensation, to adjust the sample value for an attached sense electrode.

ATI allows the designer to optimize a specific design by adjusting the sensitivity and stability of each channel through the adjustment of the ATI parameters.

The **IQS259** has a full ATI function. The full-ATI function is default enabled, but can be disabled by setting the `ATI_OFF` and `ATI_Partial` bits in the `PROX_SETTINGS0` register (0xE8, bit7:6).

The `ATI_Busy` bit in the `SYSFLAGS` register (0x10, bit2) will be set while an ATI event is busy.

For more information regarding the ATI algorithm, please contact Azoteq at: ProxSenseSupport@azoteq.com

6.6.1 ATI Sensitivity

On the **IQS259** device, the user can specify the `BASE` value (**Section 5.9**) for each channel individually and the `TARGET` values (**Section 5.10**) for the proximity (CH0) and touch (CH1-CH9) channels.



A rough estimation of sensitivity can be calculated as:

$$\text{Sensitivity} = \frac{\text{TARGET}}{\text{BASE}}$$

As can be seen from this equation, the sensitivity can be increased by either increasing the Target value or decreasing the Base value. It should, however, be noted that a higher sensitivity will yield a higher noise susceptibility.

6.6.2 ATI Target

The target value is reached by adjusting the COMPENSATION bits for each channel (ATI target limited to 2096 counts).

The target value is written into the respective channel's TARGET registers. The value written into these registers multiplied by 8 will yield the new target value. (Please refer to **Section 5.10**)

6.6.3 ATI Base (Multiplier)

The following parameters will influence the base value:

- CS_SIZE¹: Size of sampling capacitor.
- PROJ_BIAS bits: Adjusts the biasing of some analogue parameters in the mutual capacitive operated IC. (Only applicable in mutual capacitance mode.)
- MULTIPLIER bits.

The base value used for the ATI function can be implemented in 2 ways:

1. ATI_PARTIAL = 0. ATI automatically adjusts MULTIPLIER bits to reach a selected base value². Please refer

¹ Changing CS_SIZE if ATI_OFF = 0 will change CS

² ATI function will use user selected CS_SIZE and PROJ_BIAS (if applicable) and will only adjust the MULTIPLIER bits to reach the base values.

to **Section 5.9** for available base values.

2. ATI_PARTIAL = 1. The designer can specify the multiplier settings. These settings will give a custom base value from where the compensation bits will be automatically implemented to reach the required target value. The base value is determined by two sets of multiplier bits. Sensitivity Multipliers which will also scale the compensation to normalise the sensitivity and Compensation Multipliers to adjust the gain.

6.6.4 Re-ATI

An automatic re-ATI event will occur if the CS is outside its re-ATI limits. The re-ATI limit or ATI boundary is calculated as the target value divided by 8. For example:

- Target = 512, Re-ATI will occur if CS is outside 512±64.

A re-ATI event can also be issued by the host MCU by setting the REDO_ATI bit in the PROX_SETTINGS0 register (0xE8, bit4). The REDO_ATI bit will clear automatically after the ATI event was started.

Note: Re-ATI will automatically clear all proximity, touch and halt status bits.

6.6.5 Reseed

Setting the Reseed bit in the PROX_SETTINGS0 register (0xE8, bit3), will reseed all LTA filters to a value of $LTA_{\text{new}} = CS + 8$. The LTA will then track the CS value until they are even.

Performing a reseed action on the LTA filters, will effectively clear any proximity and/or touch conditions that may have been established prior to the reseed call.



6.6.6 Alternative ATI

The Alternative ATI implementation ensures that the base and multiplier values are identical for all the channels and adjusts only the compensation in order to achieve the desired count value. The Alternative ATI can be enabled in the [PROX_SETTINGS3](#) register (0xEB, bit3).



7 Communication

The **IQS259** device interfaces to a master controller via a 3-wire (SDA, SCL and RDY) serial interface bus that is I²C™ compatible, with a maximum communication speed of 400kbit/s.

Please refer to Application note: “**AZD064: IQS259 Communication Interface Guideline**” for additional I²C information on the **IQS259** communications interface and sample code.

7.1 I²C Sub-address

The **IQS259** has four available sub addresses, 44H (default) to 47H, which allows up to four devices on a single I²C bus.

7.1.1 External sub-address selection

The I²C sub-address can be configured on the CTX2 pin (pin14), allowing the designer to select two sub-addresses without the need of configuring a floating gate (One Time Programmable (OTP) option). The internal pull-up/down on CTX2 (pin 14) needs to be enabled during start-up. If the designer wants to select a sub-address, a pull-up/down resistor needs to be connected to CTX2. The firmware will then set the I²C-address, which will be selected according to **Table 7.1**.

Table 7.1 I²C sub-address external selection

CTX2	Device Address
No resistor	0x44
Pull-Down resistor	0x45
Pull-Up resistor	0x46

7.1.2 Internal sub-address selection

Selecting the sub-address via OTP bits (see **Section 10**) will allow the designer to get the same functionality as with an external resistor, without dissipating unnecessary current.

Table 7.2 I²C sub-address internal selection

FG26	FG25	Device Address
0	0	0x44
0	1	0x45
1	0	0x46
1	1	0x47

7.2 Event Mode

By default the device operates in an event-driven I²C communication mode (also called “Event Mode”), with the RDY pin ONLY indicating a communication window after a prescribed event has occurred (except for the Setup Window after POR).

These events include:

- Proximity events
- Touch events
- ATI events
- Noise events (Noise detect enabled)

Event Mode can be disabled by setting the Event Mode Disable bit in the **PROX_SETTINGS2** register (0xEA, bit2). The device will then enter a continuous streaming mode, during which the RDY line will indicate the communications windows after each charge transfer.

Note: The device is also capable of functioning **without** a RDY line on a polling basis.



7.3 RDY Hand-Shake Routine

The master or host MCU has the capability to force a communication window at any time, by pulling the RDY line low. The communication window will open directly following the current conversion.

7.4 I²C Specific Commands

7.4.1 Show Reset

The SHOW_RESET bit can be read in the PROX_STAT1 register (0x32, bit7), to determine whether a reset has occurred on the device. This bit will be set '1' after a reset.

The SHOW_RESET bit will be cleared (set to '0') by writing a '1' into the ACK_RESET bit in the PROX_SETTINGS2 register (0xEA, bit7). A reset will typically take place of a timeout during communication occurs.

7.4.2 WDT disable

The WDT (watchdog timer) is used to reset the IC if a problem (for example a voltage spike) occurs during communication. The WDT will time-out (and thus reset the device) after t_{WDT} if no valid communication occurred during this time.

The WDT can be disabled by setting the WDT Off bit in the PROX_SETTINGS2 register (0xEA, bit6).

7.4.3 Timeout Disable

If no communication is initiated from the master/host MCU within the first t_{COMMS} ($t_{COMMS} = 20ms$) of the RDY line indicating that data is available (i.e. RDY = low), the device will resume with the next channel's charge transfer process and the data from the previous conversion will be lost.

This time-out function can be disabled by setting the TIME_OUT_DISABLE bit in the PROX_SETTINGS2 register (0xEA, bit3).

7.4.4 Default Comms Pointer

The Default Comms Pointer (DCP) holds the address (0x10 default) in the IQS259 memory map, from where the first data will be read in the communications window.

The user can change the DCP by writing the address of another location in the IQS259 memory map into the DFLT_COMMS_PTR register (0xF0).

7.5 I²C R/W specifics

Please refer to Application note: “AZD064: IQS259 Communication Interface Guideline” for the I²C read and write (R/W) specifics as implemented on most ProxSense® devices.

7.6 I²C I/O Characteristics

The IQS259 requires the input voltages given in **Table 7.3**, for detecting high (“1”) and low (“0”) input conditions on the I²C communication lines (SDA, SCL and RDY).

Table 7.3 IQS259 I²C Input voltage

	Input Voltage (V)
V _{in} LOW	0.3*VDDHI
V _{in} HIGH	0.7*VDDHI

Table 7.4 provides the output voltage levels of the IQS259 device during I²C communication.

Table 7.4 IQS259 I²C Output voltage

	Output Voltage (V)
V _{out} LOW	VSS +0.2 (max.)
V _{out} HIGH	VDDHI – 0.2 (min.)



8 RF Noise

8.1 RF Noise Detection

In cases of extreme RF interference, enabling the **IQS259** on-chip RF detection is suggested.

The RF Noise Detection can be enabled by setting the Noise Detect On bit in the **PROX_SETTINGS1** register (0xE9, bit3).

By connecting a suitable antenna to the RF pin (pin 15), it allows the device to detect RF noise and notify the master of possible corrupt data. Noise affected samples are not allowed to influence the LTA filter, and also do not contribute proximity or touch detection. With the detection of RF noise, the RF NOISE bit in the **SYSFLAGS** register (0x10, bit1), will be set.

8.1.1 RF Detector Sensitivity

The sensitivity of the RF detector can be selected by setting an appropriate RF detection voltage through the RF_TRIM bits. Please see application note: “**AZD015: RF Immunity and detection in ProxSense devices**” for further details regarding this option.

8.2 RF Noise Immunity

The **IQS259** has advanced immunity to RF noise sources such as GSM cellular telephones, DECT, Bluetooth and WIFI devices. Design guidelines should however be followed to ensure the best noise immunity on a hardware level.

In general, the design of capacitive sensing applications may encompass a large range of configurations; however, following the guidelines in **Section 8.2.1** may improve a capacitive sensing design.

8.2.1 Notes for layout:

- A ground plane should be placed under the IC, except under the CRX lines.
- Place the sensor IC as close as possible to the sense electrodes.
- All the tracks on the PCB must be kept as short as possible.
- The capacitor between VDDHI and GND as well as between VREG and GND must be placed as close as possible to the IC.
- A 100 pF capacitor can be placed in parallel with the 1uF capacitor between VDDHI and GND. Another 100 pF capacitor can be placed in parallel with the 1uF capacitor between VREG and GND.
- When the device is too sensitive for a specific application a parasitic capacitor (max 5pF) can be added between the CX line and ground.
- Proper sense electrode and button design principles must be followed.
- Unintentional coupling of sense electrodes to ground and other circuitry must be limited by increasing the distance to these sources.
- In some instances a ground plane some distance from the device and sense electrode may provide significant shielding from undesirable interference.
 - * However, if after proper layout, interference from an RF noise source persists, please refer to application note: “**AZD015: RF Immunity and detection in ProxSense devices**”.

*



9 IQS259 Memory Map

9.1 Memory Registers

Table 9.1 IQS259 Memory Registers

Address	Size (Bytes)	Description	Access
00h-0Fh	16	Device Information	R
10h-30h	32	Device Specific Data	R
31h-34h	4	Proximity Status Bytes	R
35h-38h	4	Touch Status Bytes	R
39h-3Ch	4	Halt Bytes	R
3Dh-41h	4	Active Bytes (Cycle Indication)	R
42h-82h	64	Current samples (CS) / Counts	R
83h-C3h	64	LTAs	R
C4h-FDh	64	Device Settings	R/W



9.2 Memory registers Description

9.2.1 Device Information

Information regarding the device type and version is recorded here. Any other information specific to the device version can be stored here. Each Azoteq ROM has a unique Product- and Version number.

00H		Product Number (PROD_NUM)							
Access	Bit	7	6	5	4	3	2	1	0
R	Value	36 (Decimal)							

01H		Version Number (VERSION_NUM)							
Access	Bit	7	6	5	4	3	2	1	0
R	Value	02 (Decimal)							

9.2.2 Device Specific Data

10H		System Flags (SYSFLAGS)							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	System use	System use	System use	System use	System use	ATI Busy	RF Noise	Zoom

ATI Busy	Indicates whether the device is performing an ATI ‘0’: ATI not Busy ‘1’: ATI Busy
RF Noise	Indicates whether RF noise is detected “0”: Not Detected “1”: Detected
Zoom	Indicates whether the device is in Zoom mode “0”: Not in Zoom “1”: In Zoom



9.2.3 Proximity Status Bytes

The proximity status of all the channels on the device are shown here. If a bit is set it indicates a proximity condition on the specified channel.

31H		Proximity Status 0 (PROX_STAT0)							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

32H		Proximity Status 1 (PROX_STAT1)							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	SHOW RESET	System use	System use	System use	System use	System use	CH9	CH8

SHOW RESET	The SHOW RESET bit is automatically set whenever the device is reset. Setting the ACK Reset bit in the ProxSense Module Settings 2 register clears the SHOW RESET bit.
------------	---

9.2.4 Touch Status Bytes

The touch status of all the channels on the device are shown here. If a bit is set it indicates a touch condition on the specified channel.

35H		Touch Status 0 (TOUCH_STAT0)							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	CH7	CH6	CH5	CH4	CH3	CH2	CH1	System use

36H		Touch Status 1 (TOUCH_STAT1)							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	System use	System use	System use	System use	System use	System use	CH9	CH8



9.2.5 Halt Bytes

The filter halt status of all the channels on the device are shown here. If a bit is set it indicates that the filters have been halted on the specified channel.

39H		Halt 0 (HALT_STAT0)							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

3AH		Halt 1 (HALT_STAT1)							
Access	Bit	7	6	5	4	3	2	1	0
R	Name	System use	System use	System use	System use	System use	System use	CH9	CH8

9.2.6 Channel Number

The decimal number in the Active Channel register indicates the active channel.

3DH		Active Channel (ACT_CHAN)							
Access	Bit	7	6	5	4	3	2	1	0
R	Value	Decimal Number indicating active (current) channel (0-9)							

Note: This byte indicates which channel's data is currently available in the CS and LTA bytes.

9.2.7 Count (CS) Values

The Count (CS) Values stored in this register are from the current cycle only as indicated in the Active Channel register.

42H		Count (CS) Value High byte (CS_HI)							
Access	Bit	7	6	5	4	3	2	1	0
R	Value	Variable (High byte)							



43H		Count (CS) Value Low byte (CS_LO)							
Access	Bit	7	6	5	4	3	2	1	0
R	Value	Variable (Low byte)							

9.2.8 Long-Term Averages

The Long-Term Averages stored in these registers are from the current cycle only. (See active channel).

83H		Long-Term Average High byte (LTA_HI)							
Access	Bit	7	6	5	4	3	2	1	0
R	Value	Variable (High byte)							

84H		Long-Term Average Low byte (LTA_LO)							
Access	Bit	7	6	5	4	3	2	1	0
R	Value	Variable (Low byte)							

9.2.9 Device Settings

Target Count 0 and 1 sets the target CS value for the respective channels. For the ATI routine to execute, the ATI-off bit in PROX_SETTINGS0 needs to be set to “0”. If data is written to one of these channels and the LTA is out of range a re-ATI event will occur, unless a touch condition is active on the channel where the re-ATI will wait until the touch condition is lifted. The default target CS for CH0 with a register value Target Count 0 (CH0) = 128 then becomes $128 \times 8 = 1024$. The device initiates the ATI routine for a specific channel when the LTA drifts out of the Target Count \pm decimal value stored in the Target Count registers and no Touch or Prox conditions exists on the specific channel. The ATI routine can also be initiated by the master by setting the Redo-ATI bit in PROX_SETTINGS0 to “1”.

C4H		ATI Target Count CH0 (TARGET_CNT0)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Target Count Value (x8)							
		Default: 128 Decimal (Re-ATI boundary \pm 128)							



C5H		ATI Target Count CH1-CH9 (TARGET_CNT1)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Target Count Value (x8)							
		Default: 64 Decimal (Re-ATI boundary \pm 64)							

The compensation for each channel can be set by writing the appropriate value to the corresponding channels Compensation Register. The Compensation directly influences the Count value of a Channel and will trigger a re-ATI when the LTA of the respective channels are out of range and the ATI-off bit in PROX_SETTINGS0 is not set 1.

C6H		Channel 0 Compensation Setting (CH0_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 0 <7:0>							

C7H		Channel 1 Compensation Setting (CH1_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 1 <7:0>							

C8H		Channel 2 Compensation Setting (CH2_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 2 <7:0>							

C9H		Channel 3 Compensation Setting (CH3_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 3 <7:0>							

CAH		Channel 4 Compensation Setting (CH4_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 4 <7:0>							



CBH		Channel 5 Compensation Setting (CH5_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 5 <7:0>							

CCH		Channel 6 Compensation Setting (CH6_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 6 <7:0>							

CDH		Channel 7 Compensation Setting (CH7_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 7 <7:0>							

CEH		Channel 8 Compensation Setting (CH8_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 8 <7:0>							

CFH		Channel 9 Compensation Setting (CH9_COMP)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Compensation 9 <7:0>							



The Multiplier Setting register for each channel sets the gain values which determine the sensitivity and compensation to reach the ATI routine target. The Table below provides a description of the bits that can be set in the CH0 – CH9 Multiplier Setting registers. By writing to the Multiplier Settings of a channel, the individual channel that is active in that specific time slot (indicated in the Channel Sequence 0 and 1 registers) will undergo a re-ATI event if the new multiplier settings result in the LTA being out of range and the ATI-off bit is cleared in PROX_SETTINGS0. To prevent the User selected Multiplier Settings to be over written by the ATI routine, the Partial ATI bit in PROX_SETTINGS0 need to be set to 1.

Mul5:Mul4	Sensitivity Multiplier
Mul3:0	Compensation Multiplier
Base7:6	<p>The base value influences the overall sensitivity of the channel and establishes a base count from where the ATI algorithm starts executing.</p> <p>The following options are available:</p> <p>“00” – 200 “01” – 50 “10” – 100 “11” – 250</p>

D0H		Channel 0 Multiplier Setting (MULT_CH0)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D1H		Channel 1 Multiplier Setting (MULT_CH1)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D2H		Channel 2 Multiplier Setting (MULT_CH2)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0



D3H		Channel 3 Multiplier Setting (MULT_CH3)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D4H		Channel 4 Multiplier Setting (MULT_CH4)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D5H		Channel 5 Multiplier Setting (MULT_CH5)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D6H		Channel 6 Multiplier Setting (MULT_CH6)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D7H		Channel 7 Multiplier Setting (MULT_CH7)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D8H		Channel 8 Multiplier Setting (MULT_CH8)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0

D9H		Channel 9 Multiplier Setting (MULT_CH9)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Base1	Base0	Mul5	Mul4	Mul3	Mul2	Mul1	Mul0



The proximity sensitivity settings of each respective channel sets the $\Delta = \text{Counts} - \text{LTA}$ threshold for a proximity event on the specified channel (refer to **Section 6.5**). A custom value between 1 and 254 can be selected by setting bits PT_7 to PT_0.

DAH		Channel 0 Proximity Threshold (PROX_TH_CH0)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254							
		Default: 4 Decimal							

DBH		Channel 1 Proximity Threshold (PROX_TH_CH1)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254							
		Default: 4 Decimal							

DCH		Channel 2 Proximity Threshold (PROX_TH_CH2)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254							
		Default: 4 Decimal							

DDH		Channel 3 Proximity Threshold (PROX_TH_CH3)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254							
		Default: 4 Decimal							

DEH		Channel 4-9 Proximity Threshold (PROX_TH_CH4_CH9)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254							
		Default: 4 Decimal							



The touch sensitivity setting of each respective channel sets the Touch Delta = Count - LTA threshold for a touch event on the specified channel. A custom value between 1 and 254 can be selected by setting bits used as TOUCH_TH = (value/255)*LTA. A Touch event will be triggered when Touch Delta > TOUCH_TH.

DFH		Channel 1 Touch Threshold (TOUCH_TH_CH1)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							

E0H		Channel 2 Touch Threshold (TOUCH_TH_CH2)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							

E1H		Channel 3 Touch Threshold (TOUCH_TH_CH3)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							

E2H		Channel 4 Touch Threshold (TOUCH_TH_CH4)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							

E3H		Channel 5 Touch Threshold (TOUCH_TH_CH5)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							



E4H		Channel 6 Touch Threshold (TOUCH_TH_CH6)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							

E5H		Channel 7 Touch Threshold (TOUCH_TH_CH7)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							

E6H		Channel 8 Touch Threshold (TOUCH_TH_CH8)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							

E7H		Channel 9 Touch Threshold (TOUCH_TH_CH9)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 254, used as value/255 * ATI Target							
		Default: 32/255							



The IQS259 is setup using the ProxSense® Module Settings registers.

E8H		ProxSense® Module Settings 0 (PROX_SETTINGS0)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	ATI Off	Partial ATI	ATI Current CH	Redo-ATI	Reseed	CS Size	Bias1	Bias0
	Default	0	0	0	0	0	1	1	0

ATI Off	If this bit is set, the ATI routine will be disabled: ‘0’: Disabled ‘1’: Enabled
Partial ATI	Uses the Multipliers to determine the sensitivity and compensation to reach the ATI target, instead of the full ATI routine. “0”: Disabled “1”: Enabled
ATI Current Channel	Performs a re-ATI on the current channel, as indicated by the Sequence register 3DH
Redo ATI	Forces the ATI routine to run when a ‘1’ is written into this bit position. ATI Off in address E8H bit 7 takes priority
Reseed	All channels are reseeded when a ‘1’ is written into this bit position. The LTA’s are set to 8 counts below the current samples
CS Size	The internal charge capacitor is 29.9pF or 59.8pF. This bit is set by default.
Bias1:0	Set the projected op-amp bias current: “00” : 1.25uA “01” : 2.5uA “10” : 5uA “11” : 10uA

* Note: It is not recommended to adjust the projected (internal) op-amp Bias1:0 bits. These bits are reserved for advanced design configurations. Please contact Azoteq for more information regarding this subject: www.azoteq.com.



E9H		ProxSense® Module Settings 1 (PROX_SETTINGS1)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	CTX Float	CRX Float	Turbo Mode	Halt Charge / ULP	Noise Detect On	System use	System use	System use
	Default	0	0	0	0	0	0	0	0

CTX Float	During conversions the inactive channels are grounded in order to minimize noise coupling. If this bit is set the transmitter electrodes will float when inactive
CRX Float	During conversions the inactive channels are grounded in order to minimize noise coupling. If this bit is set the receiver electrodes will float when inactive
Turbo mode	If this bit is set, conversions are performed as fast as processing and communication allows, thereby maximizing detection speed
Halt Charge/ULP	Set this bit to stop all conversions. The device will now draw the minimum amount of power
Noise Detect On	Enables the noise detection '0': Disabled '1': Enabled

* Note: PROX_SETTINGS1 register bits 2:0 are used for adjusting the sensitivity level of the on-chip RF detection features. We recommend contacting Azoteq ProxSense® Support before altering these settings: ProxSenseSupport@azoteq.com



EAH		ProxSense® Module Settings 2 (PROX_SETTINGS2)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	ACK Reset	WDT Off	Force Halt	AC Filter Disable	Time-out Disable	Event Mode Disable	Halt1	Halt0
	Default	0	0	0	0	0	0	0	0

Ack Reset	<p>Clears the reset bit:</p> <p>0 = Default</p> <p>1 = Clears SHOW_RESET</p>
WDT Off	<p>Disable the watchdog timer:</p> <p>0 = Enabled</p> <p>1 = Disabled</p>
Force Halt	<p>Forces the Long Term Average of all channels to stop being calculated</p> <p>'0': LTA updates normally</p> <p>'1': LTA is halted</p>
AC filter Disable	<p>Set the AC filter. Disabling the AC filter will enable a faster response time</p> <p>0 = Enabled</p> <p>1 = Disabled</p>
Timeout Disable	<p>If this bit is set, a timeout will be allowed on the communication</p> <p>0 = Disabled</p> <p>1 = Enabled</p>
Event Mode Disable	<p>Sets Event driven I²C™ communication</p> <p>0 = Enabled</p> <p>1 = Disabled</p>
Halt1:Halt0	<p>Sets the Halt time for the LTA (time before recalibration):</p> <p>00 = 20 Seconds</p> <p>01 = 40 Seconds</p> <p>10 = Never</p> <p>11 = Permanent</p>



EBH		ProxSense® Module Settings 3 (PROX_SETTINGS3)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	Beta1 CH0	Beta0 Ch0	Beta1	Beta0	Alt ATI Enable	Distributed CH0 SELF	Charge Xfer Speed1	Charge Xfer Speed0
	Default	0	1	0	1	0	0	0	0

Beta1:0 CH0	Beta CH0 "00": 1/32 "01": 1/64 "10": 1/128 "11": 1/256
Beta1:0	Beta "00": 1/32 "01": 1/64 "10": 1/128 "11": 1/256
Alternative ATI Enable	Set the alternative ATI function "0" = Disable "1" = Enable
Distributed channel surface	"0" = Disabled: Prox channel normal operation "1" = Enabled: Prox channel operates in surface mode
Charge Xfer Speed0:1	Charge Transfer Speed "00": 1MHz "01": 500kHz "10": 250kHz (Period will be too long and negatively impact times) "11": 125kHz (Period will be too long and negatively impact times)



ECH		Channel Enable CH0-CH7 (CHAN_ENABLE0)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	Default	1	1	1	1	1	1	1	1

CH7:CH0	<p>Software enable or disable of channels: 0 = Channel Disabled 1 = Channel Enabled</p>
---------	---

EDH		Channel Enable CH8-CH9 (CHAN_ENABLE1)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Name	System use	System use	System use	System use	System use	System use	CH9	CH8
	Default							1	1

CH9:CH8	<p>Software enable or disable of channels: 0 = Channel Disabled 1 = Channel Enabled</p>
---------	---



EEH		Low Power Settings (LOW_POWER)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Value	Custom value between 1 and 256, used as value * 16ms = LP period							
	Default	Normal Power (00h). See note below.							

NOTE: While in any power mode the device will zoom to Boost Power (BP) mode whenever the (Count – LTA) > T_THR or P_THR indicating a possible proximity or touch event. This improves the response time. The device will remain in BP for t_{ZOOM} seconds and then return to the selected power mode. The Zoom function allows reliable detection of events with current samples being produced at the BP rate.

F0H		Default Comms Pointer (DFLT_COMMS_PTR)							
Access	Bit	7	6	5	4	3	2	1	0
R/W	Default	10H							



10 IQS259 OTP Options

The **IQS259** only provide OTP (One-Time Programmable) options for configuration of the device I²C sub-address.

Configuration of the I²C sub-address can be done on packaged devices or in-circuit. In-circuit configuration may be limited by values of external components chosen.

Azoteq offers a Configuration Tool (CT220 or later) and associated software that can be used to program the OTP user options for prototyping purposes. For further information regarding this subject, please contact your local distributor or submit enquiries to Azoteq at: ProxSenseSupport@azoteq.com

10.1 User Selectable OTP options

Table 10.1 User Selectable OTP options : Bank3

bit7	Bank 3						bit0
System use	System use	System use	System use	System use	I ² C SubAddr1	I ² C SubAddr0	System use

Bank3: bit7	System Use
Bank3: bit6	System Use
Bank3: bit5	System Use
Bank3: bit4	System Use
Bank3: bit3	System Use
Bank3: bit 2:1	I ² C SubAddr1: I ² C SubAddr0 : I ² C Sub-Address selection
	00 = 0x44 01 = 0x45 10 = 0x46 11 = 0x47
Bank3: bit 0	System Use



11 Specifications

11.1 Absolute Maximum Specifications

The following absolute maximum parameters are specified for the device:

Exceeding these maximum specifications may cause damage to the device.

- Operating temperature -40°C to 85°C
- Supply Voltage (VDDHI – VSS) 3.6V
- Maximum pin voltage VDDHI + 0.5V (may not exceed VDDHI max)
- Maximum continuous current (for specific Pins) 10mA
- Minimum pin voltage VSS - 0.5V
- Minimum power-on slope 100V/s
- ESD protection ±4kV (Human body model)
- Package Moisture Sensitivity Level (MSL) 3

Table 11.1 IQS259 General Operating Conditions¹

DESCRIPTION	Conditions	PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage		V _{DDHI}	1.8	3.3V	3.6	V
Internal regulator output	1.8 ≤ V _{DDHI} ≤ 3.6	V _{REG}	1.62	1.7	1.79	V
Default Operating Current	3.3V	I _{IQS259NP}	-	150	430	µA
Low Power Setting 1*	3.3V, LP=32	I _{IQS259LP32}	-	6.2	30	µA
Low Power Setting 2*	3.3V, LP=128	I _{IQS259LP128}	-	3.5	7	µA
Low Power Setting 3*	3.3V, LP=256	I _{IQS259LP256}	-	3	5	µA

*LP interval period = Low power value x 16ms

Table 11.2 Start-up and shut-down slope Characteristics

DESCRIPTION	Conditions	PARAMETER	MIN	MAX	UNIT
Power On Reset	V _{DDHI} Slope ≥ 100V/s @25°C	POR	1.2	1.6	V
Brown Out Detect	V _{DDHI} Slope ≥ 100V/s @25°C	BOD	1.15	1.6	V

¹Operating current shown in this datasheet, does not include power dissipation through I²C pull up resistors.



Table 11.3 Event Mode Response Times

DESCRIPTION	PARAMETER	MIN	MAX	Unit
TURBO MODE ¹	Response time	60	70	ms
NORMAL	Response time	90	200	ms

Table 11.4 Repetitive Touch Rates

DESCRIPTION	Conditions	PARAMETER	Sample rate = 5ms	Sample rate = 9ms	UNIT
All power modes	Zoom active	Response Rate ²	>9	>4	Touches/second

The sample rate of the **IQS259** is increased by:

- Faster communication.
- Less data transfer.
- Using the fast charge selection (Turbo Mode) of the **IQS259**.

¹Communication and charge frequency to comply with sample rate as reported earlier in this datasheet.

²Debounce of 6 up and 3 down



12 Package information

12.1 IQS259 Package dimensions

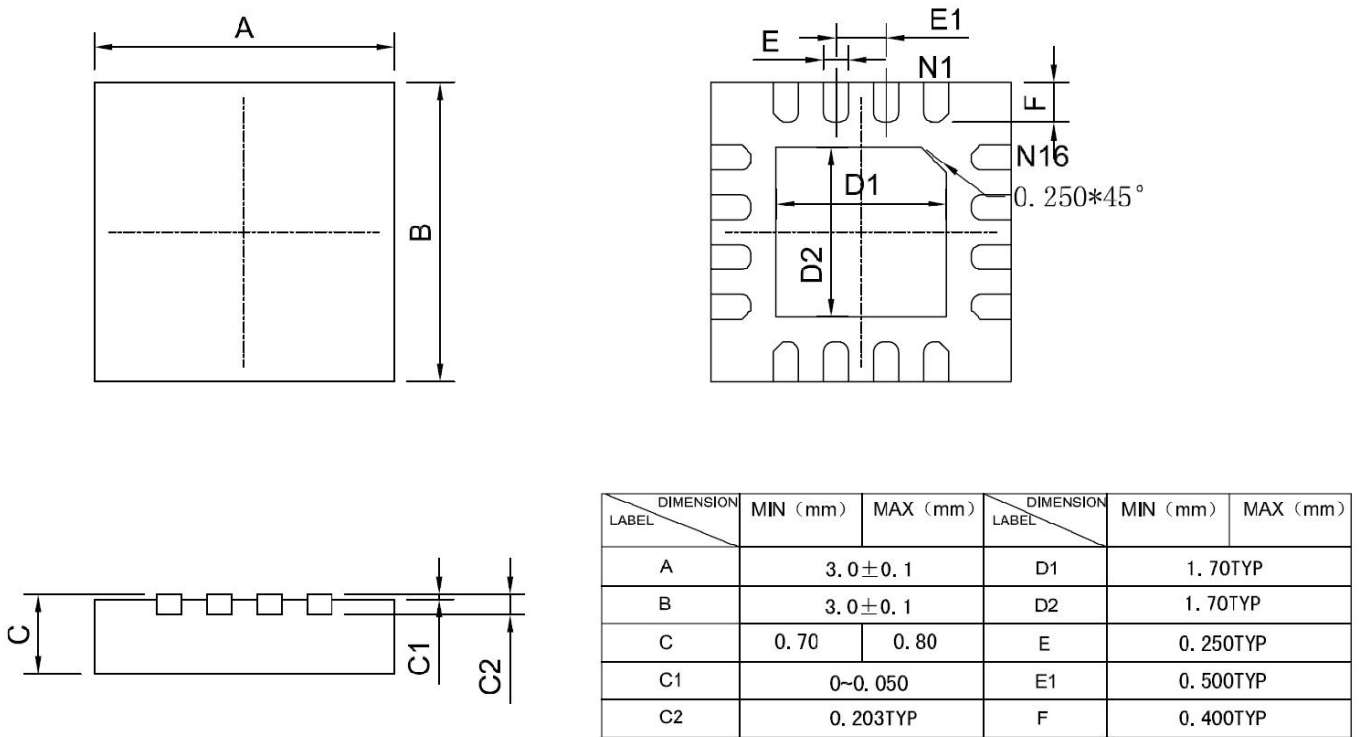


Figure 12.1 QFN(3x3)-16 Package Dimensions

12.2 Recommended PCB footprint

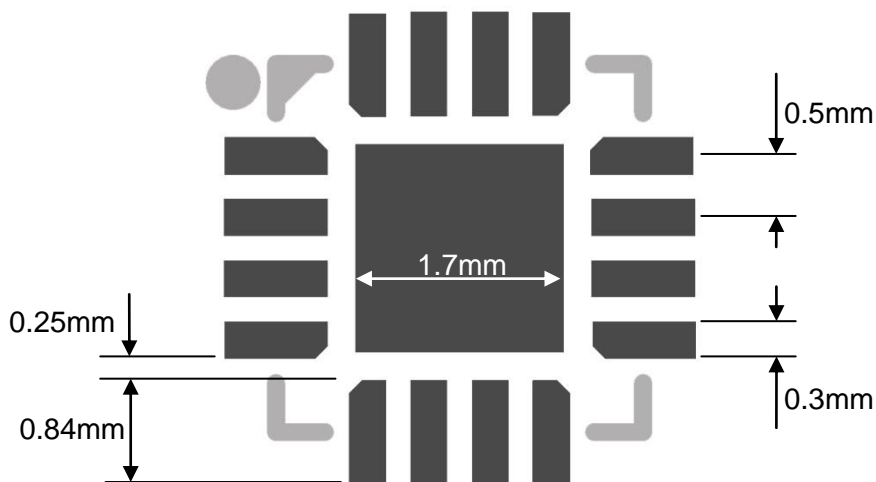
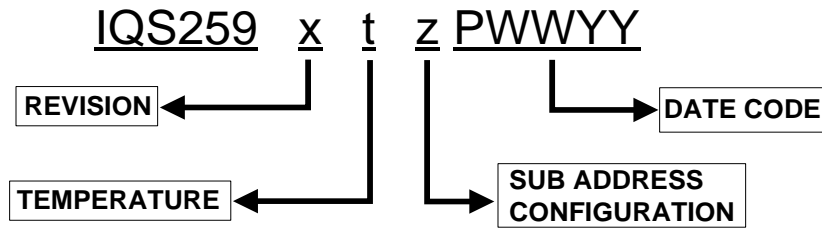


Figure 12.1 IQS259 Recommended PCB footprint



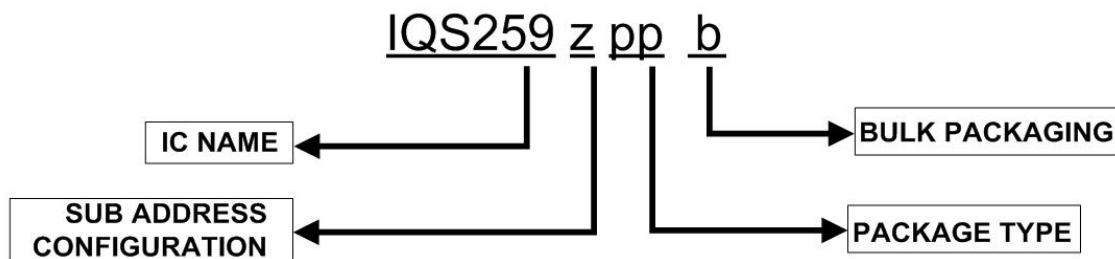
13 Device Marking



REVISION	x	=	IC Revision Number
TEMPERATURE RANGE	t	=	I -40°C to 85°C (Industrial) C 0°C to 70°C (Commercial)
IC CONFIGURATION	z	=	Sub Address Configuration (Hexadecimal) 0 = 44H 1 = 45H 2 = 46H 3 = 47H
DATE CODE	P	=	Package House
	WW	=	Week
	YY	=	Year

14 Ordering Information

Order quantities will be subject to multiples of a full reel. Contact the official distributor for sample quantities. A list of the distributors can be found under the “Distributors” section of www.azoteq.com.



IC NAME	IQS259	=	IQS259
CONFIGURATION	z	=	Sub Address Configuration (hexadecimal)
PACKAGE TYPE	QN	=	QFN(3x3)-16
BULK PACKAGING	R	=	Reel (3000pcs/reel)



15 Contact Information

PRETORIA OFFICE

Physical Address
160 Witch Hazel Avenue
Hazel Court 1, 1st Floor
Highveld Techno Park
Centurion, Gauteng
Republic of South Africa
Tel: +27 12 665 2880
Fax: +27 12 665 2883
Postal Address
PO Box 16767
Lyttelton
0140
Republic of South Africa

PAARL OFFICE

Physical Address
109 Main Street
Paarl
7646
Western Cape
Republic of South Africa
Tel: +27 21 863 0033
Fax: +27 21 863 1512
Postal Address
PO Box 3534
Paarl
7620
Republic of South Africa

** Please visit the Azoteq website for a list of distributors and representations worldwide.*

The following patents relate to the device or usage of the device: US 6,249,089 B1, US 6,621,225 B2, US 6,650,066 B2, US 6,952,084 B2, US 6,984,900 B1, US 7,084,526 B2, US 7,084,531 B2, US 7,119,459 B2, US 7,265,494 B2, US 7,291,940 B2, US 7,329,970 B2, US 7,336,037 B2, US 7,443,101 B2, US 7,466,040 B2, US 7,498,749 B2, US 7,528,508 B2, US 7,755,219 B2, US 7,772,781, US 7,781,980 B2, US 7,915,765 B2, EP 1 120 018 B1, EP 1 206 168 B1, EP 1 308 913 B1, EP 1 530 178 B1, ZL 99 8 14357.X, AUS 761094

IQ Switch®, ProxSense®, LightSense™, AirButton® and the  logo are trademarks of Azoteq.

The information in this Datasheet is believed to be accurate at the time of publication. Azoteq assumes no liability arising from the use of the information or the product. The applications mentioned herein are used solely for the purpose of illustration and Azoteq makes no warranty or representation that such applications will be suitable without further modification, nor recommends the use of its products for application that may present a risk to human life due to malfunction or otherwise. Azoteq products are not authorized for use as critical components in life support devices or systems. No licenses to patents are granted, implicitly or otherwise, under any intellectual property rights. Azoteq reserves the right to alter its products without prior notification. For the most up-to-date information, please refer to www.azoteq.com.

WWW.AZOTEQ.COM

ProxSenseSupport@azoteq.com