# IQS222 Datasheet
# IQ Switch® - ProxSense® Series
## Wheel/Slider and Touch Key Controller with Proximity Detection

With human-machine interfacing requiring ever higher functionality and intuitiveness, touch panel type interfaces are rapidly becoming the norm for the new millennium.

The IQS222 offers industry leading resolution for a wheel/slider controller. The IQS222 is an 8 channel capacitive sensing device, 3 of which can be used for a wheel/slider type interface. The device can operate as a controller for 8 keys **OR** for a wheel or slider and up to 5 keys.

### Features

- Single device controls a wheel/slider (using 3 channels) and up to 5 keys, or up to 8 keys
- System cost reduction (lower BOM count)
- Class leading wheel/slider resolution with up to 11 bits
- Reliability through reducing system complexity
- Class leading proximity sensitivity – suitable for wake-up from sleep or launching a menu screen on a user approaching
- 2-wire serial interface bus, $I^2C^{TM}$ compatible
- Noise immunity and detection
- 8 touch sensitivity settings per channel
- Available in QFN(4x4)-20 and SO-20 package


### Applications

- Personal Navigation Devices
- Personal Media Players
- Consumer Electronics
- White goods and appliances
- Keypads
- Kiosk and POS Terminals
- E-Book Readers
- PDA's
- Flame Proof, Hazardous environment Human Interface Devices

# Contents

# Overview

## 1. Introduction

The ProxSense® IQS222 is a fully integrated eight-channel capacitive sensor. It can control a wheel/slider and up to 5 independent keys. The device also features an internal system regulator, ensuring class leading proximity sensitivity and stability at an unparalleled cost. The device interfaces to a master controller via a 2 wire serial interface bus that is I²C™ compatible. The device is available in QFN (4x4)-20 and SO-20 packages, making it ideal for devices where there is a severe space constraint.

Through unique patented technology a cost effective solution is offered to replace conventional electromechanical switches and dials. ProxSense® is capable of detecting a differentiated touch or proximity condition through almost any dielectric, allowing designers to project touch pads or sliders through a variety of materials. A further benefit is the reduced cost associated with mechanical deterioration over time or from working in harsh environments.

### 1.1 Wheel and Slider Design

The IQS222 can control either a wheel or slider, (refer to Figure 1.1 and Figure 1.2). As with normal touch pads, these wheels and sliders can be etched onto a standard PCB. Downloadable CAD files for wheels and sliders can be found on the Azoteq website, www.azoteq.com.

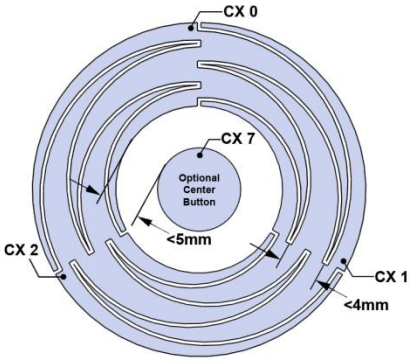



**Figure 1.1 Wheel Configuration**

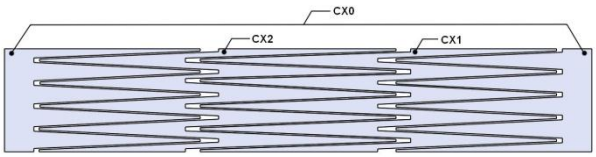



**Figure 1.2 Slider Configuration**

## 1.2 Pin Diagrams

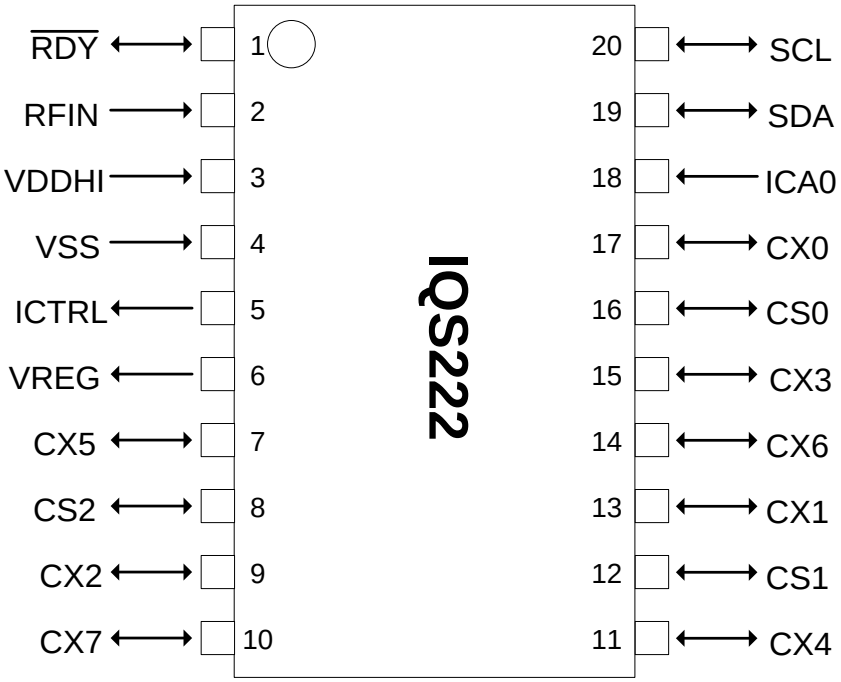



**Figure 1.3 SO-20 Pin diagram**

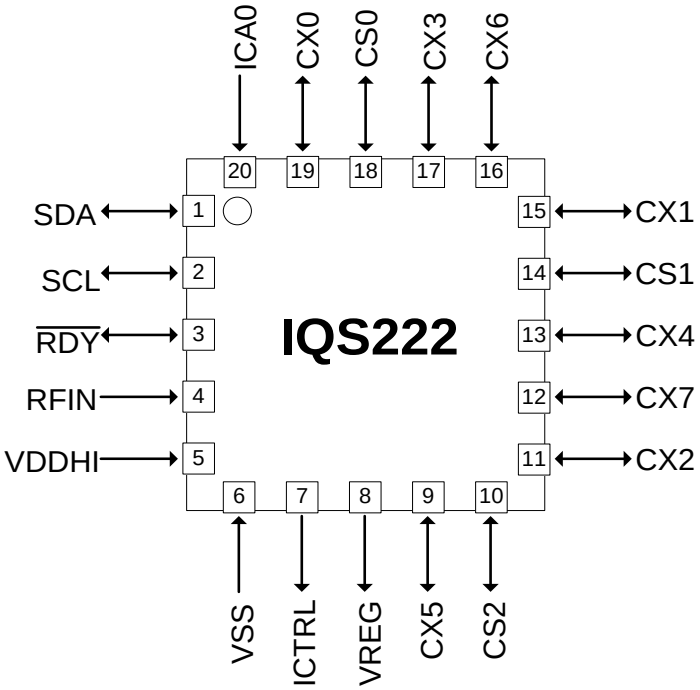



**Figure 1.4 QFN (4x4)-20 Pin diagram**

## 1.3 Pin Description

**Table 1.1 I/O Description**

| SO-20 Pin | QFN(4x4)-20 Pin | Name | I/O | Description |
|---|---|---|---|---|
| 19 | 1 | SDA | Bi-directional/ Open Drain | Serial data line |
| 20 | 2 | SCL | Bi-directional/ Open Drain | Serial clock line |
| 1 | 3 | $\overline{\text{RDY}}$ | Bi-directional/ Open Drain | Data available indication/ Wakeup from sleep |
| 2 | 4 | RFIN | Input | RF detector antenna input |
| 3 | 5 | VDDHI | Supply Input | Supply Voltage input |
| 4 | 6 | VSS | Ground Input | GND reference |
| 5 | 7 | ICTRL | Custom | Current reference |
| 6 | 8 | VREG | Analogue Output | Internal regulator output |
| 7 | 9 | CX5 | Bi-directional | Sense electrode 5 |
| 8 | 10 | Cs2 | Bi-directional | Reference capacitor 2 |
| 9 | 11 | Cx2 | Bi-directional | Sense electrode 2 |
| 10 | 12 | Cx7 | Bi-directional | Sense electrode 7 |
| 11 | 13 | Cx4 | Bi-directional | Sense electrode 4 |
| 12 | 14 | Cs1 | Bi-directional | Reference capacitor 1 |
| 13 | 15 | Cx1 | Bi-directional | Sense electrode 1 |
| 14 | 16 | Cx6 | Bi-directional | Sense electrode 6 |
| 15 | 17 | Cx3 | Bi-directional | Sense electrode 3 |
| 16 | 18 | Cs0 | Bi-directional | Reference capacitor 0 |
| 17 | 19 | Cx0 | Bi-directional | Sense electrode 0 |
| 18 | 20 | ICA0 | Input | Device address selection bit 0 |

# 2 Circuit Overview

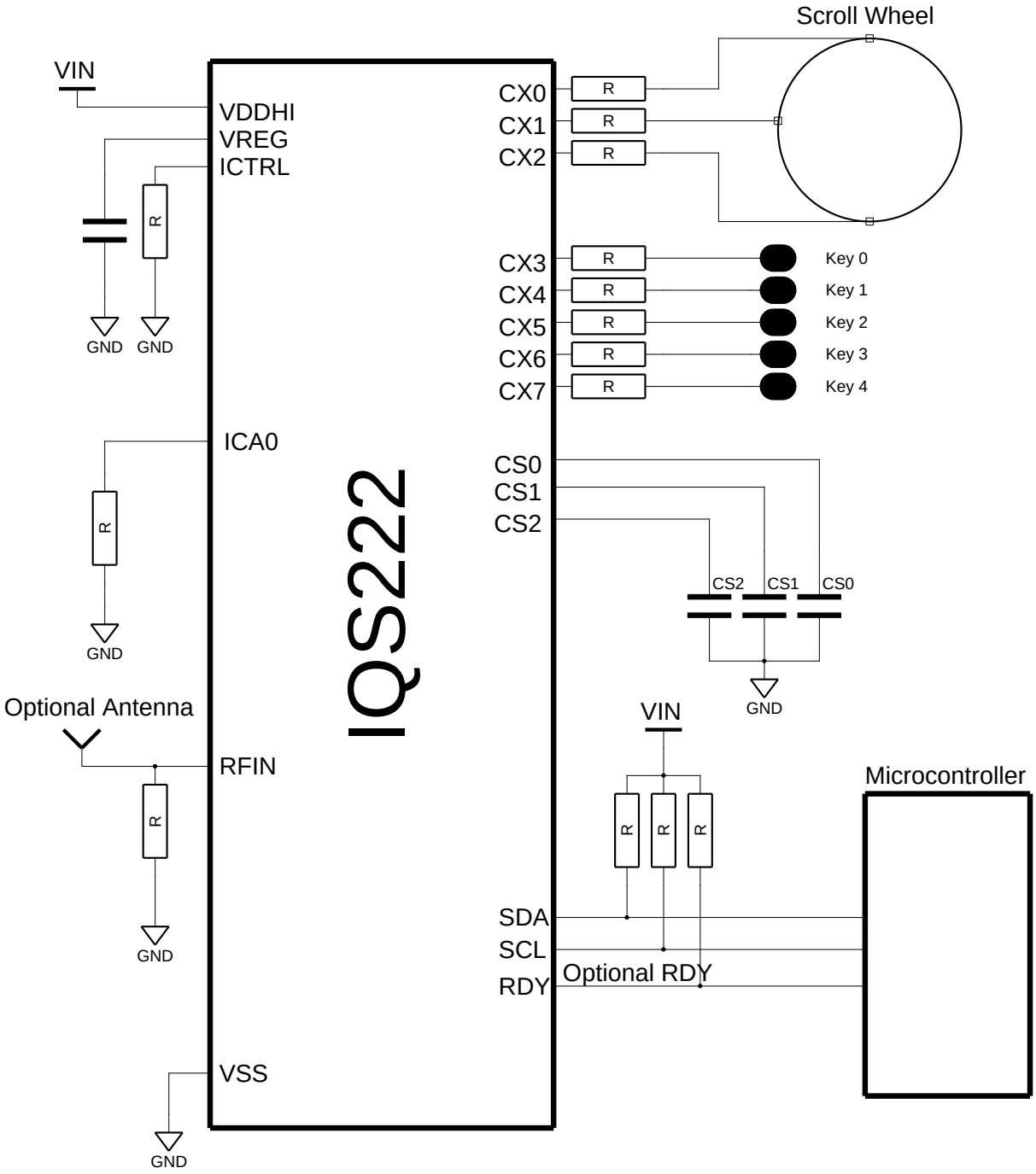



**Figure 2.1 Typical Connection Diagram**

# 3 IQS222 Demo GUI

The IQS222 Demo GUI is used for demonstration and development purposes. This allows designers to get a feel for the operation of the IQS222 and to experiment with the various settings that are available. The IQS222 Demo GUI is available on the Azoteq website, www.azoteq.com. Refer to the following application note: "AZD020 – IQS222 GUI Overview.pdf" for more information.


**Figure 3.1 IQS222 Demo GUI**

# 4 ProxSense Module

The charge transfer method of capacitive sensing is employed on the IQS222. Refer to the application note "AZD004: Azoteq Capacitive Sensing", which thoroughly describes the charge transfer principle. A Charge cycle is used to detect either a physical contact or proximity event, depending on the application.

Three Cx channels are multiplexed into one Cs capacitor as indicated in Table 4.1(excluding Cs2). The charge cycles of the IQS222 can be measured on the Cs pins (Refer to Figure 4.1).

For applications requiring proximity, Cx7 is recommended as the proximity sensing channel, since the Dynamic Noise Threshold is implemented on Cx7 (refer to Section 5.1) and Cx7 has separate proximity and touch thresholds (refer to Section 4.2). Refer to application note: "AZD008 – Design Guidelines for Touch Pads" for information of designing optimal sense pads.

**Table 4.1 Multiplexed charging scheme**

| CX | | | CS |
|---|---|---|---|
| **Group A** | **Group B** | **Group C** | |
| Cx0 | Cx3 | Cx6 | Cs0 |
| Cx1 | Cx4 | Cx7 | Cs1 |
| Cx2 | Cx5 | - | Cs2 |

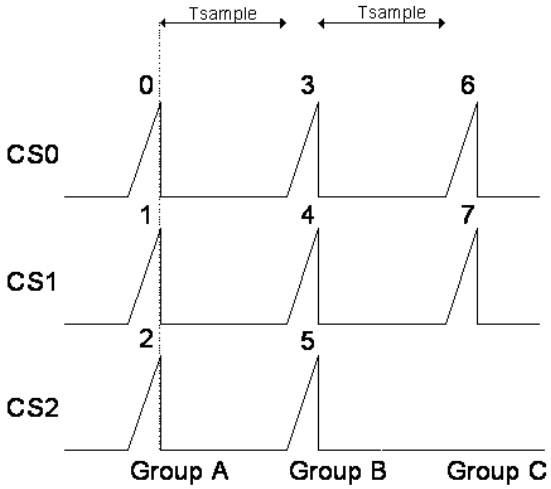



**Figure 4.1 Multiplexed charging scheme**

## 4.2 Threshold Selections

### 4.2.1 Touch Threshold Selections

The touch thresholds are set in THRESH_CFG_1 and THRESH_CFG_2 registers. The touch threshold value is expressed as a factor of the long term average value. This setting is used to calculate the individual CX channels' touch states. The channels are divided into the following groups for touch thresholds:

- Cx0 to Cx2 (normally the wheel/slider)
- Cx3 to Cx6 (normally discrete keys)
- Cx7 (normally a key or dedicated proximity detector)

### 4.2.2 Proximity Threshold Selections

The proximity thresholds are set in the THRESH_CFG_1 and THRESH_CFG_2 registers. The proximity threshold selection value is a delta that is subtracted from the average filter value to determine an individual CX channels' proximity threshold. The channels are divided into the following groups for proximity thresholds:

- Cx0 to Cx6 (normally wheel/slider and/or discrete keys)

- Cx7 (normally a key or dedicated proximity detector)

## 4.3 Low Power and Normal Power Modes

The IQS222 can operate in either a Normal Power mode (NP) or in a Low-Power mode (LP). The device operates in NP mode by default; however, the LP mode can be selected in the POWER_CFG register.

If the device is in LP mode, the conversion rate can be set to one of the selections shown in Table 4.2 within the POWER_CFG register.

## 4.4 Zoom Mode

Zoom mode is only available if the Low Power (LP) mode is selected in the POWER_CFG register. In the LP mode, conversions are done according to TLP in Table 4.2.

With the detection of a proximity condition, the conversion rate zooms in to the NP (Normal Power) Mode ($T_{Sample}$). The device then operates in the zoomed in state for 3s after the last proximity has been detected. When 3 seconds elapses, the conversion rate returns to the LP timing selection.

## 4.5 Extra Low Power Mode

This power mode can be used to put the IQS222 into a semi-sleep mode. This setting can be selected in the POWER_CFG register.

In this additional low power mode the device will switch off all Cx channels except Cx7 if no proximity condition is detected for 50s or more. Cx7 will continue to charge according to the selected charge frequency, while the other channels will be periodically charged every 3 seconds to keep their filters updated. When a proximity condition is detected on Cx7 the device will revert back to its normal conversion rate. This setting can be used in conjunction with normal or low power modes.

## 4.6 Charge Period in Low Power Mode

In low power mode four charge cycle times are selectable. The low power modes are ideal for battery applications. The different power modes control the duty cycle between charge transfers (TLP). The Charge transfers are set in the POWER_CFG register (refer to Section 8.14). The timings ($T_{LP}$) given in Table 4.2 and are measured from the beginning of the first conversion to the start of the following conversion.

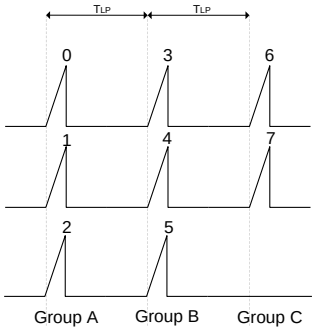



**Figure 4.2 Measurement of $T_{LP}$**

**Table 4.2 LP timings**

| Power Mode | Timing[1] (TLP) |
|---|---|
| LP1 | 74ms |
| LP2 | 133ms |
| LP3 | 192ms |
| LP4 | 250ms |

[1] Timings are approximate.

## 4.7 Long Term Average (LTA) Filter Halt

The IQS222 intelligently filters the capacitive samples to keep track of environmental changes. The filter averages the samples for each Cx channel. The measured value is compared to the average to determine if a proximity or touch condition occurred.

If a touch or prox condition is detected on a channel it will freeze to keep the average value as a reference for determining touch and prox states.

The averaging filter halt time can be set to the values shown in Table 4.3. These values are set in the FILTER_CFG register. The IQS222 can also be manually recalibrated by setting the 'Reseed' bit in the POWER_CFG register. In this way stuck conditions can be easily dealt with (refer to Section 8.14).

**Table 4.3 Filter Adaptation Conditions**

| THALT | Filter |
|---|---|
| Short | Filter halts for ~45s, and then recalibrates |
| Long | Filter halts for ~90s, and then recalibrates |
| Never | Filter Adaptation NEVER halts |
| Permanent | Filter Adaptation ALWAYS halts |

# 5 Additional Features

## 5.1 Long Term Noise (LTN) Filter

The IQS222 makes use of a dynamic noise threshold on the dedicated proximity sensing channel (Cx7). The LTN monitors the average amount of ambient noise in the operational environment and adjusts the proximity threshold of Cx7 accordingly. If the device is operational in a very noisy environment the proximity sensitivity is adjusted dynamically to desensitize the device. The LTN filter can be deactivated in the FILTER_CFG register (refer to Section 8.17).

## 5.2 RF Noise Detection

The IQS222 has advanced immunity to RF high power noise typically transmitted by GSM cellular telephones, DECT, Bluetooth and WIFI devices. Design guidelines can be followed to help with the noise immunity:

- A ground plane should be placed under the IC, except under the CX lines.
- All the tracks on the PCB must be kept as short as possible.
- The capacitor between VDDHI and VSS as well as between VREG and VSS, must be placed as close as possible to the IC.
- A 100 pF capacitor can be placed in parallel with the 1uF capacitor between VDDHI and VSS. Another 100 pF capacitor can be placed in parallel with the 1uF capacitor between VREG and VSS.

There is, however, still a small possibility that the device may detect false prox or touch conditions if a cellular telephone is placed in extreme close proximity to the device. For this exception, the IQS222 has a built-in noise detection circuit. The IQS222 is therefore able to detect cellular telephone noise or any other high power transmitted noise on the RFIN pin. In some applications the RFIN pin may require an external antenna to increase detection efficiency. Please refer to the application note: “AZD015 – RF Detection Antenna.pdf” for more information.

When noise is detected, the IQS222 will halt and keep all outputs in their respective states before the noise was detected. The Noise Detection circuit can be disabled in the FILTER_CFG register.

## 5.3 Stop Transmit

When the STOP TRANSMIT bit is set within the FILTER_CFG register, the $\overline{\text{RDY}}$ pin will stop indicating that the device is ready for data transmission. The device will, however, continue doing conversions if the $\overline{\text{RDY}}$ Timeout Enable bit is set (refer to Section 8.16). The device will resume communications if a proximity condition is detected, or can be manually restarted by temporarily pulling the $\overline{\text{RDY}}$ line low.

By using this feature a master device can ignore data from the IQS222 until a proximity condition is detected.

## 5.4 Sleep

When the IQS222 is not required to sense it can be put into sleep mode, to conserve power, by setting the ‘sleep’ bit in the POWER_CFG register. To resume conversions the master device should temporarily pull the $\overline{\text{RDY}}$ line low. The device will wake up on a rising edge on the $\overline{\text{RDY}}$ line.

## 5.5 Fast Charge

The IQS222 has a fast charge selection option (refer to Section 8.14 for bit selections) to change the charge frequency from 50Hz to 65Hz. Choosing

the faster charge time, will increase the response rate of the device. Other methods of increasing the response rate are discussed in Section 5.5.1.

### 5.5.1 Response Rate

Except for using the faster charge time, there are two more methods of increasing the response rate of the IQS222:

Choosing smaller Cs capacitors (Range 10nF:100nF) and disabling unused channels (10k pull-down, see Figure 5.1) will shorten the charge cycle, which will increase the response rate. Refer to application note “AZD004-Overview of Capacitive Touch and Proximity Sensing Technology” for more details on the charge cycle. Smaller Cs caps will, however, reduce the sensitivity. Choosing a faster $I^2C$ speed will also increase the response rate of the IQS222 as observed in applications.

## 5.6 Disable Channels

Disabling a channel is done with a pull-down resistor on the Cx pin to GND. Typical values used for pull-down resistors are 10k.

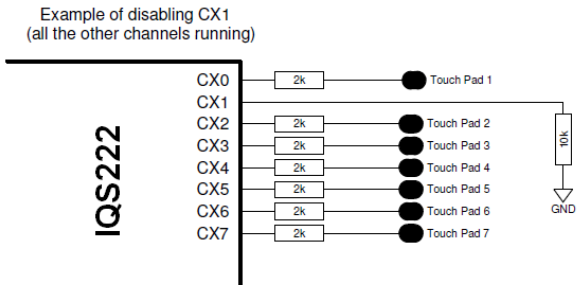



**Figure 5.1 Disable Cx1.**

# 6 Serial Interface

The IQS222 uses 100 kHz bi-directional 2-wire bus and data transmission protocol. The serial protocol is I²C™ compatible. The IQS222 has an optional $\overline{\text{RDY}}$ pin which indicates when the device enters its communication window period. Communication with the device can only take place during this window period, this can be determined by monitoring the $\overline{\text{RDY}}$ line or by using ACK polling (Refer to Section 6.3)

The IQS222 can only function as a slave device on the bus. The bus must be controlled by a master device which generates the serial clock (SCL), controls bus access, and generates the START and STOP conditions.

The serial clock (SCL) and serial data lines (SDA) are open-drain and therefore must be pulled high to the operating voltage with a pull-up resistor (typically 10k).

It is important to remember that the IQS222 will pull down the SCL line (between 50us and 100us) before it will ACK. Therefore, when implementing a software I²C protocol on the master, it is important to realise clock stretching.

## 6.1 $\overline{RDY}$ Line Operation

The $\overline{\text{RDY}}$ line provides the following functions:

- During normal operation $\overline{\text{RDY}}$ indicates that the devices has entered its communication window period by pulling the $\overline{\text{RDY}}$ line low
- Used to force the resumption of communication with the device after a STOP_TRANSMIT instruction has been sent (Refer to Section 5.3)
- Used to wake the device from sleep (Refer to Section 5.4)

The $\overline{\text{RDY}}$ pin functions as an open-drain pin and should always be pulled to the operating voltage of the master device via a resistor (typically 100k).

When the device enters the communications window the $\overline{\text{RDY}}$ line will be pulled low by the IQS222 device. The $\overline{\text{RDY}}$ line will remain low for the duration of the communications window.

By default the communication window is entered and the device will not exit until the device receives a STOP condition. A timeout can be enabled for the communication window by setting the $\overline{\text{RDY}}$ Timeout Enable bit (refer to Section 8.16). When the $\overline{\text{RDY}}$ Timeout is enabled the device will enter the communications window and will wait for the master to initiate communications for a fixed duration of 2ms. If the master does not initiate a data transfer during this time, the device will exit the communications window and continue doing conversions. At the start of the communications window the address pointer will default to the value specified in the DEFAULT_ADDR register (refer to Section 8.18). In this way the user can simply start reading without having to set the address pointer first. The $\overline{\text{RDY}}$ line will remain low for the duration of the communication window period.

## 6.2 Communication Timeout

The IQS222 has a communication timeout (“watchdog”) function which is automatically initiated after data transfer initiation.

The IQS222 will exit the communication window, and release the $\overline{\text{RDY}}$ line to go high, if data transfer has been initiated (after a start condition) and consecutive data bytes are more than 13ms apart. The communication timeout timer is:

- Fixed at 13.26ms.
- Cannot be switched off.

- Will reset at the start of each data byte received.

## 6.3 Bus Characteristics

The following bus protocol has been defined:

- Data transfer may only be initiated when the bus is not busy
- During data transfer the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock is HIGH will be interpreted as START and STOP conditions.

The following conditions have been defined for the bus (refer to Figure 6.1).

### 6.3.1 Bus Idle (A)

The SCL and SDA line are both HIGH.

### 6.3.2 START Condition (B)

A HIGH to LOW transition of the SDA while the SCL is HIGH. All serial communication must be preceded by a START condition.

### 6.3.3 STOP Condition (C)

A LOW to HIGH transition of the SDA while the SCL is HIGH. All serial communication must be ended by a STOP condition. NOTE: When a STOP condition is sent the device will exit the communications window and continue with conversions.

### 6.3.4 Data Valid (D)

The state of the SDA line represents valid data when, after a START condition, the SDA is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition.

### 6.3.5 Acknowledge

The slave device must generate an acknowledge after the reception of each byte. The master device must generate an extra (9th) clock pulse which is associated with this acknowledge bit. The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse. NOTE: The IQS222 does not generate any acknowledge bits while it is not in its communication window.

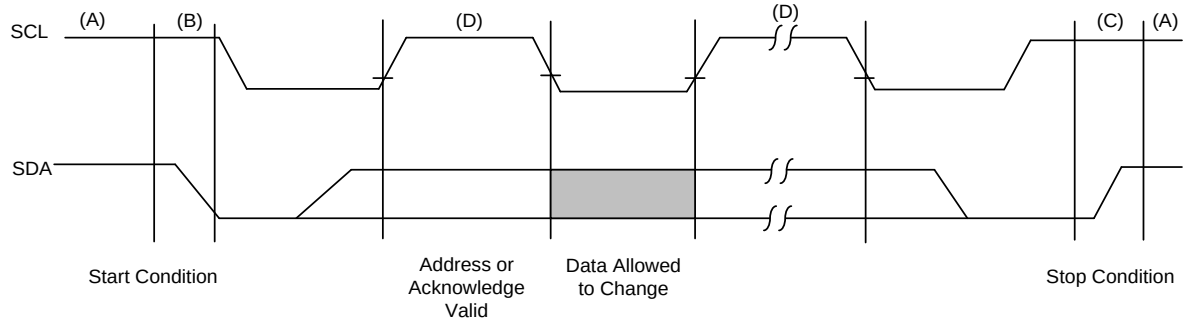



**Figure 6.1 Data Transfer Sequence on the Serial Bus**

## 6.4 Acknowledge Polling

If the master device does not have an I/O available for the $\overline{RDY}$ line, ACK polling can be used to determine when the device is ready for communication.

The device will not acknowledge during a conversion cycle, this can be used to determine when a cycle is complete and whether the device has entered its communication window.

Once a stop condition is sent by the master the device will perform the next conversion cycle. ACK polling can be initiated at any time during the conversion cycle to determine if the device has entered its communication window.

To perform ACK polling the master sends a start condition followed by the control byte. If the device is still busy then no ACK will be returned. If the device has completed its cycle the device will return an ACK, and the master can proceed with the next read or write operation (Refer to Figure 6.2).

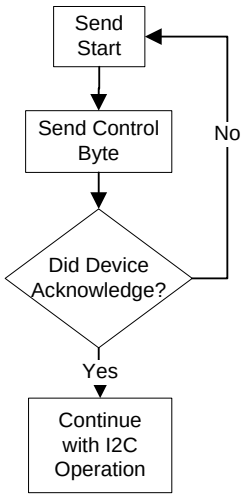



**Figure 6.2 ACK Polling**

## 6.5 Control Byte Format

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 7 bit device address and the Read/ $\overline{Write}$ indicator bit (refer to Figure 6.3).


**Figure 6.3 Control Byte Format**

### 6.5.2 Sub addressing

Each slave device on the serial bus requires a unique 7 bit device identifier. When the control byte is sent by the master the device will be able to determine if it is the intended recipient of a data transaction. The Device address selection is controlled with the ICA0 pin and an OTP fuse (ICA1). If more than 2 addresses are required please contact your local distributor for devices with ICA1 set to '1'. I2CA0 is set to 0 by pulling the pin low with a 1M resistor (to ground), or to 1 by pulling the pin high (to VREG).

**Table 6.1 $I^2C$ Sub Addresses**

| I2CA1 | I2CA0 | Address (7-bit) |
|---|---|---|
| 0 | 0 | 0x70[1] |
| 0 | 1 | 0x71 |
| 1 | 0 | 0x72 |
| 1 | 1 | 0x73 |

## 6.6 Address Pointer Operation

When the device enters the communications window period the address pointer defaults to the position

[1] The address for engineering versions of the IC's is 0x04. Sub addressing is not possible on engineering versions.

specified in the DEFAULT_ADDR register (refer to Section 8.18). The DEFAULT_ADDR is set to 0x10 at POR.

The address pointer will auto increment when reading or writing across sections of reserved address spaces. In this way all data can read out in a single continuous read operation.

## 6.7 Current Address Read Operation

Once the communications window is entered and a data transfer is initiated the required data can simply be read. The read transfer is in the format shown in Figure 6.4.Once all the required data has been read the master must send a NACK. The master can then either generate another start condition to perform another read or write operation or it can generate a stop condition, at which point the device will exit the communications window and will continue with conversions.

## 6.8 Random Read Operation

In order to do a random read operation the address pointer must first be written, after which the master must generate another start condition and must then initiate a sequential read operation as shown in Figure 6.5. The master can then either generate another start condition to perform another read or write operation or it can generate a stop condition, at which point the device will exit the communications window and will continue with conversions.

## 6.9 Write Operation

Once the communications window is entered and a data transfer is initiated, a write operation can be executed. Write operations are in the format shown in Figure 6.6. Once the master is finished writing the master can then either generate another start condition to perform another read or write operation or it can generate a stop condition, at which point the device will exit the communications window and will continue with conversions.

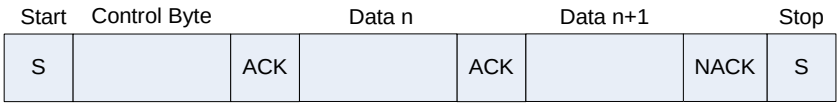


Figure 6.4 Current Address Read Operation


Figure 6.5 Random Read

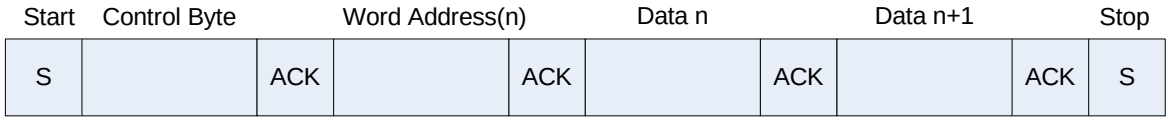



Figure 6.6 I²C Write Operation

## 6.10 Reset

The IQS222 does not have a reset option available through an I²C command. To reset the device, a power cycle is required.

# 7 Serial Memory Map

The table below give a listing of the addresses for serial interface.

| Name | Description | Type | Address | Comment |
|---|---|---|---|---|
| PROD_NR | Product Number | r | 0x00 | |
| FW_VER | Firmware Version | r | 0x01 | |
| Reserved (do not modify) | | | 0x02-0x09 | Reserved |
| WHEEL_DATA_H | Wheel Data | r | 0x10 | |
| WHEEL_DATA_L | | r | 0x11 | |
| Reserved (do not modify) | | | 0x12-0x30 | Reserved |
| PROX_STATE | Prox States | r | 0x31 | |
| Reserved (do not modify) | | | 0x32-0x34 | Reserved |
| TOUCH_STATE | Touch States | r | 0x35 | |
| Reserved (do not modify) | | | 0x36-0x38 | Reserved |
| HALT_STATE | Halt States | r | 0x39 | |
| Reserved (do not modify) | | | 0x3A-0x3C | Reserved |
| ACTIVE_CHAN | Active Channel States | r | 0x3D | |
| Reserved (do not modify) | | | 0x3E-0x41 | Reserved |
| CSA_H | Count Value A | r | 0x42 | |
| CSA_L | | r | 0X43 | |
| CSB_H | Count Value B | r | 0x44 | |

| | | | | |
|---|---|---|---|---|
| CSB_L | | r | 0x45 | |
| CSC_H | Count Value C | r | 0x46 | |
| CSC_L | | r | 0x47 | |
| Reserved (do not modify) | | | 0x48-0x82 | Reserved |
| LTA_H | Long Term Average A | r | 0x83 | |
| LTA_L | | r | 0X84 | |
| LTB_H | Long Term Average B | r | 0x85 | |
| LTB_L | | r | 0x86 | |
| LTC_H | Long Term Average C | r | 0x87 | |
| LTC_L | | r | 0x88 | |
| Reserved (do not modify) | | | 0x89-0xC3 | Reserved |
| POWER_CFG | Power Configuration | rw | 0xC4 | |
| THRESH_CFG_1 | Threshold Configuration | rw | 0xC5 | |
| THRESH_CFG_2 | | rw | 0xC6 | |
| FILTER_CFG | Filter Configuration | rw | 0xC7 | |
| DEFAULT_ADDR | Default Address | rw | 0xC8 | = 0x10 at POR |
| LTA_W_CHAN | LTA Write Channel | w | 0xC9 | |
| LTA_W_H | LTA Write Value | w | 0XCA | |
| LTA_W_L | | w | 0XCB | |

# 8 Memory Map Description

## 8.1 PROD_NR (0x00)

**Table 8.1 PROD_NR (0x00)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

The device identification register. This register contains the device identifier, which is 0x0C for the IQS222.

## 8.2 FW_VER (0x01)

**Table 8.2 FW_VER (0x01)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Firmware Version Number | | | | | | | |

The firmware version number. This register contains the firmware version number for the IQS222. The latest firmware version is 0x03.

## 8.3 WHEEL_DATA_H (0x10) and WHEEL_DATA_L (0x11)

**Table 8.3 WHEEL_DATA_H (0x10)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Noise Detection | Wheel Coordinate High Byte | | | | | | |

**Table 8.4 WHEEL_DATA_L (0x11)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Wheel Coordinate Low Byte | | | | | | | |

The current coordinate value of the wheel or slider. The MSB of the High register is used to indicate if noise is detected. If 7 bit resolution is selected the current wheel coordinate will be placed in the Wheel Data High Register. The Wheel Data Low Register will be cleared in 7 bit mode.

## 8.4 PROX_STATE (0x31)

**Table 8.5 PROX_STATE (0x31)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Prox 7 | Prox 6 | Prox 5 | Prox 4 | Prox 3 | Prox 2 | Prox 1 | Prox 0 |

The prox states for the channels.

## 8.5 TOUCH_STATE (0x35)

**Table 8.6 TOUCH_STATE (0x35)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Touch 7 | Touch 6 | Touch 5 | Touch 4 | Touch 3 | Touch 2 | Touch 1 | Touch 0 |

The touch states for the channels.

## 8.6 HALT_STATE (0x39)

**Table 8.7 HALT_STATE (0x39)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Halt 7 | Halt 6 | Halt 5 | Halt 4 | Halt 3 | Halt 2 | Halt 1 | Halt 0 |

The halt states for the channels. Indicates if the averaging filter for a particular channel is currently halted.

## 8.7 ACTIVE_CHAN (0x3D)

**Table 8.8 ACTIVE_CHAN (0x3D)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Active 7 | Active 6 | Active 5 | Active 4 | Active 3 | Active 2 | Active 1 | Active 0 |

Indicates which channels are active for the current conversion cycle. This is used to determine which channels' count values and long term average values are currently available.

## 8.8 CSA_H (0x42) and CSA_L (0x43)

**Table 8.9 CSA_H (0x42)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Count Value A High Byte | | | | | | | |

**Table 8.10 CSA_L (0x43)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Count Value A Low Byte | | | | | | | |

The count value for the channel in position A. The ACTIVE_CHAN register is used to determine which channel's count value is present. The channels that are stored here are 0, 3, and 6.

## 8.9 CSB_H (0x44) and CSB_L (0x45)

**Table 8.11 CSB_H (0x44)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Count Value B High Byte | | | | | | | |

**Table 8.12 CSB_L (0x45)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Count Value B Low Byte | | | | | | | |

The count value for the channel in position B. The ACTIVE_CHAN register is used to determine which channel's count value is present. The channels that are stored here are 1, 4, and 7.

## 8.10 CSC_H (0x46) and CSC_L (0x47)

**Table 8.13 CSC_H (0x46)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Count Value C High Byte | | | | | | | |

Table 8.14 CSC_L (0x47)

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Count Value C Low Byte | | | | | | | |

The count value for the channel in position C. The ACTIVE_CHAN register is used to determine which channel's count value is present. The channels that are stored here are 2 and 5.

## 8.11 LTA_H (0x83) and LTA_L (0x84)

Table 8.15 LTA_H (0x83)

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Long Term Average A High Byte | | | | | | | |

Table 8.16 LTA_L (0x84)

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Long Term Average A Low Byte | | | | | | | |

The Long Term Average value for the channel in position A. The ACTIVE_CHAN register is used to determine which channel's Long Term Average value is present. The channels that are stored here are 0, 3, and 6.

## 8.12 LTB_H (0x85) and LTB_L (0x86)

Table 8.17 LTB_H (0x85)

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Long Term Average B High Byte | | | | | | | |

Table 8.18 LTB_L (0x86)

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Long Term Average B Low Byte | | | | | | | |

The Long Term Average value for the channel in position A. The ACTIVE_CHAN register is used to determine which channel's Long Term Average value is present. The channels that are stored here are 1, 4, and 7.

## 8.13 LTC_H (0x87) and LTC_L (0x88)

**Table 8.19 LTC_H (0x87)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Long Term Average C High Byte | | | | | | | |

**Table 8.20 LTC_L (0x88)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Long Term Average C Low Byte | | | | | | | |

The Long Term Average value for the channel in position A. The ACTIVE_CHAN register is used to determine which channel's Long Term Average value is present. The channels that are stored here are 2 and 5.

## 8.14 POWER_CFG (0xC4)

**Table 8.21 POWER_CFG (0xC4)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Sleep | Reseed | Zoom | XLP | Fast Charge | Charge Period | | Power Mode |

Table 8.22 Power Settings Description

| | |
|---|---|
| Sleep | Device enters sleep mode when a ‘1’ is written into this bit position Refer to Section 5.4. |
| Reseed | All channels are reseeded when a ‘1’ is written into this bit position. |
| Zoom | Device zooms into normal power mode when a proximity condition is detected. Refer to Section 4.4.<br>‘0’: Device enters zoom on proximity detection<br>‘1’: Zoom is disabled |
| XLP | Device periodically switches off all channels except channel 7 (refer to Section 4.5)<br>‘0’: Disabled<br>‘1’: Enabled |
| Fast Charge | Controls the charging time<br>‘0’: 50 Hz<br>‘1’:65 Hz |
| Charge Period | Controls the charge cycle time when in low power mode<br>‘00’: 74 ms<br>‘01’: 133 ms<br>‘10’: 192 ms<br>‘11’: 250 ms |
| Power Mode | Controls the power mode of the device<br>‘0’: Normal power mode<br>‘1’: Low power mode |

## 8.15 THRESH_CFG_1 (0xC5)

Table 8.23 THRESH_CFG_1

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| P06 | T36_2 | T36_1 | T36_0 | CX_VSS | T02_2 | T02_1 | T02_0 |

### Table 8.24 Threshold Settings 1 Description

| | |
|---|---|
| P06 | Proximity threshold selection for channels 0 to 6<br>(Refer toTable 8.25) |
| T36_2<br>T36_1<br>T36_0 | Touch threshold selection for channels 3 to 6<br>(Refer to Table 8.26) |
| CX_VSS | '0 ' : Ground Cx Channels between conversions<br>'1' : Float Cx Channels between conversions |
| T02_2<br>T02_1<br>T02_0 | Touch threshold selection for channels 0 to 2<br>(Refer to Table 8.27) |

### Table 8.25 Channels 0 to 6 Proximity Threshold

| Prox Range | P06 | Proximity Threshold |
|---|---|---|
| 0 | 0 | 6 |
| 0 | 1 | 2 |
| 1 | 0 | 12 |
| 1 | 1 | Disabled |

### Table 8.26 Channels 3 to 6 Touch Threshold

| T36_2 | T36_1 | T36_0 | Touch Threshold |
|---|---|---|---|
| 0 | 0 | 0 | 1/32 |
| 0 | 0 | 1 | 2/32 |
| 0 | 1 | 0 | 3/32 |
| 0 | 1 | 1 | 4/32 |
| 1 | 0 | 0 | 5/32 |
| 1 | 0 | 1 | 6/32 |
| 1 | 1 | 0 | 7/32 |
| 1 | 1 | 1 | 8/32 |

Table 8.27 Channels 0 to 2 Touch Threshold

| T02_2 | T02_1 | T02_0 | Touch Threshold |
|---|---|---|---|
| 0 | 0 | 0 | 1/32 |
| 0 | 0 | 1 | 2/32 |
| 0 | 1 | 0 | 3/32 |
| 0 | 1 | 1 | 4/32 |
| 1 | 0 | 0 | 5/32 |
| 1 | 0 | 1 | 6/32 |
| 1 | 1 | 0 | 7/32 |
| 1 | 1 | 1 | 8/32 |

## 8.16 THRESH_CFG_2 (0xC6)

Table 8.28 THRESH_CFG_2

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Prox Range | Force Halt | P7_1 | P7_0 | $\overline{\text{RDY}}$ Timeout Enable | T7_2 | T7_1 | T7_0 |

### Table 8.29 Threshold Settings 2 Description

| | |
|---|---|
| Prox Range | Controls which range of proximity threshold selections are available<br>'0': Default proximity threshold range<br>'1': Alternative proximity threshold range |
| Force Halt | Forces the Long Term Average to stop being calculated<br>'0': LTA updates normally<br>'1': LTA is halted |
| P7_1<br>P7_0 | Proximity threshold selection for channel 7<br>(Refer to Table 8.30) |
| $\overline{\text{RDY}}$ Timeout Enable | Enable the $\overline{\text{RDY}}$ timeout<br>'0': $\overline{\text{RDY}}$ timeout disabled<br>'1': $\overline{\text{RDY}}$ timeout enabled |
| T7_2<br>T7_1<br>T7_0 | Touch threshold selection for channel 7<br>(Refer to Table 8.31) |

### Table 8.30 Channel 7 Proximity Threshold

| Prox Range | P7_1 | P7_0 | Proximity Threshold |
|---|---|---|---|
| 0 | 0 | 0 | 6 |
| 0 | 0 | 1 | 12 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 32 |
| 1 | 1 | 1 | Disabled |

Table 8.31 Channel 7 Touch Threshold

| T7_2 | T7_1 | T7_0 | Touch Threshold |
|---|---|---|---|
| 0 | 0 | 0 | 1/32 |
| 0 | 0 | 1 | 2/32 |
| 0 | 1 | 0 | 3/32 |
| 0 | 1 | 1 | 4/32 |
| 1 | 0 | 0 | 5/32 |
| 1 | 0 | 1 | 6/32 |
| 1 | 1 | 0 | 7/32 |
| 1 | 1 | 1 | 8/32 |

## 8.17 FILTER_CFG (0xC7)

Table 8.32 FILTER_CFG

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Stop Transmit | Noise Detect Disable | Wheel Resolution | LTN Disable | Wheel Disable | Wheel Filter Disable | Halt_1 | Halt_0 |

### Table 8.33 Filter Settings Description

| | |
|---|---|
| Stop Transmit | Device stops serial communication when a '1' is written into this bit position (refer to Section 5.23). |
| Noise Detect Disable | Disables Noise Detection (refer to Section 5.2)<br>'0': Enabled<br>'1': Disabled |
| Wheel Resolution | Sets the resolution of the wheel output<br>'0': 11 bit<br>'1': 7 bit |
| LTN Disable | Disables the LTN filter (refer to Section 5.1)<br>'0': Enabled<br>'1': Disabled |
| Wheel Disable | Disables the wheel output<br>'0': Enabled<br>'1': Disabled |
| Wheel Filter Disable | Disables the wheel filter<br>'0': Enabled<br>'1': Disabled |
| Halt_0<br>Halt_1 | Time before a recalibrate takes place, (Refer to Table 8.34) |

### Table 8.34 Halt Time

| Halt 1 | Halt 0 | Halt Time |
|---|---|---|
| 0 | 0 | 45 seconds |
| 0 | 1 | 90 seconds |
| 1 | 0 | Never Halt |
| 1 | 1 | Permanent Halt |

## 8.18 DEFAULT_ADDR (0xC8)

**Table 8.35 DEFAULT_ADDR (0xC8)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Default Address (0x10 at POR) | | | | | | | |

## 8.19 LTA_W_CHAN (0xC9), LTA_W_H (0xCA) and LTA_W_L(0xCB)

**Table 8.36 LTA_W_CHAN (0XC9)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Channel Number | | | | | | | |

**Table 8.37 LTA_W_H (0XCA)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LTA Write MSB | | | | | | | |

**Table 8.38 LTA LTA_W_L (0XCB)**

| Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LTA Write LSB | | | | | | | |

# 9 Reference Design

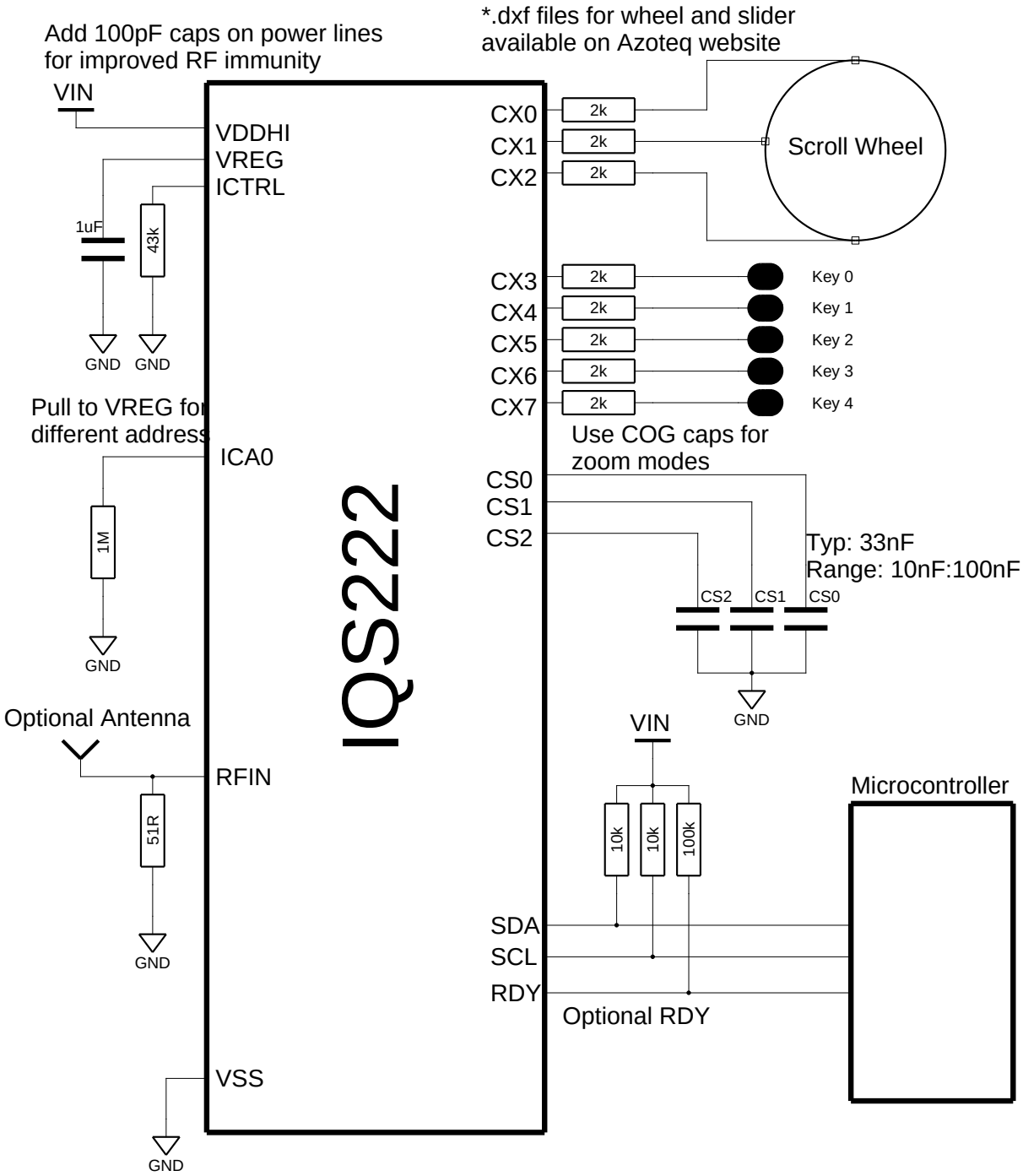



**Figure 9.1 Reference Design.**

# 10 Electrical Specifications

## 10.1 Absolute Maximum Specifications

*Exceeding these maximum specifications may cause damage to the device.*

| | |
|---|---|
| Operating Temperature | -40°C to 85°C |
| Storage Temperature | -55°C to 125°C |
| Maximum Pin Voltage (VDDHI, VREG, VSS) | 5.5V |
| Pin voltage (Cs, Cx) | 2.5V |
| Minimum Pin Voltage | -0.5V |
| Minimum Turn On Slope | 1V/s |
| Maximum Turn Off Slope (VREG) | TBD |
| ESD Protection (All Pads) | 2kV |

## 10.2 System Resources

**Table 10.1 System Resources.**

| | |
|---|---|
| Controller Operating frequency | 2MHz |
| Charge transfer frequency | 250kHz / 125kHz (@ 2MHz Controller) |

## 10.3 Operating Conditions (Measured at 25°C)

**Table 10.2 Operating Conditions.**

| DESCRIPTION | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Internal Regulator Output | VREG | 2.2 | 2.5 | 2.8 | V |
| Supply Voltage Input | $V_{DDHI}$ | 2[1] | 3.3 | 5.5 | V |
| Normal Operating Current[2] | $I_{IQS222\_NORMAL\_STREAMING}$ | 126 | 164 | | µA |
| | $I_{IQS222\_NORMAL\_NO\_STREAMING}$ | 119 | 152 | | µA |

[1] For supply voltages below 2.8V, the allowed ripple on the input voltage is lower as described in Application Note AZD031.

[2] Charge Cycle duration < 10ms.

## Table 10.2 Operating Conditions.

| DESCRIPTION | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Low Power Operating Current | $I_{IQS222\_LP1\_STREAMING}$ | 42 | 54 | | µA |
| | $I_{IQS222\_LP1\_NO\_STREAMING}$ | 34 | 42 | | uA |
| | $I_{IQS222\_LP2\_STREAMING}$ | 30 | 38 | | µA |
| | $I_{IQS222\_LP2\_NO\_STREAMING}$ | 24 | 29 | | uA |
| | $I_{IQS222\_LP3\_STREAMING}$ | 23 | 30 | | uA |
| | $I_{IQS222\_LP3\_NO\_STREAMING}$ | 19 | 23 | | uA |
| | $I_{IQS222\_LP4\_STREAMING}$ | 20 | 27 | | uA |
| | $I_{IQS222\_LP4\_NO\_STREAMING}$ | 17 | 21 | | uA |
| XLP $Current_{STREAMING}$ | $I_{IQS222\_LP4\_XLP}$ | 19 | 22 | | uA |
| Sleep Current | $I_{IQS222\_Sleep}$ | | 8 | | uA |
| Cs trip voltage | $V_{TRIP}$ | 600 | 730 | 785 | mV |
| Input Low Voltage on Cx pins | $V_{IL-CX}$ | | 0.1*VREG | | V |
| Input High Voltage on Cx pins | $V_{IH-CX}$ | | 0.9*VREG | | V |

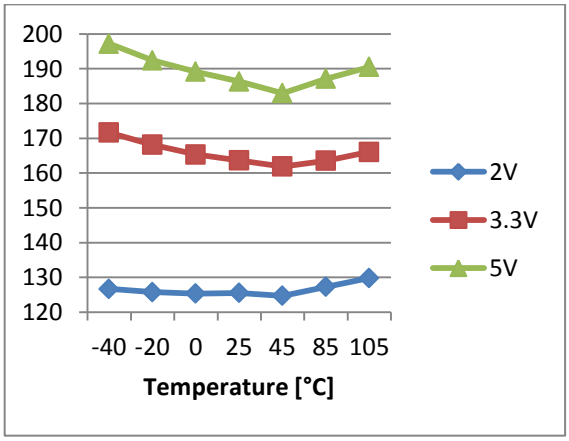



Figure 10.1 Current Consumption [uA] in NP mode while streaming.

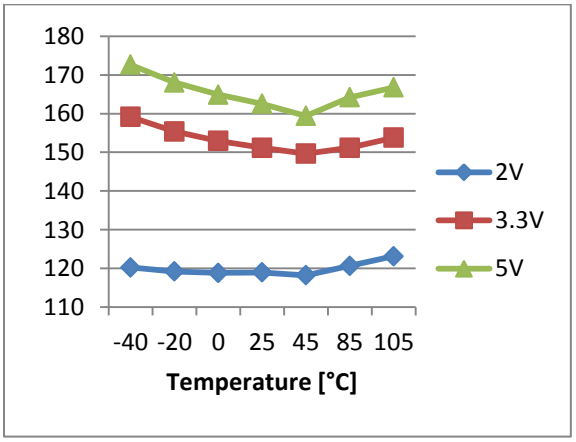



Figure 10.2 NP current consumption [uA], no streaming.

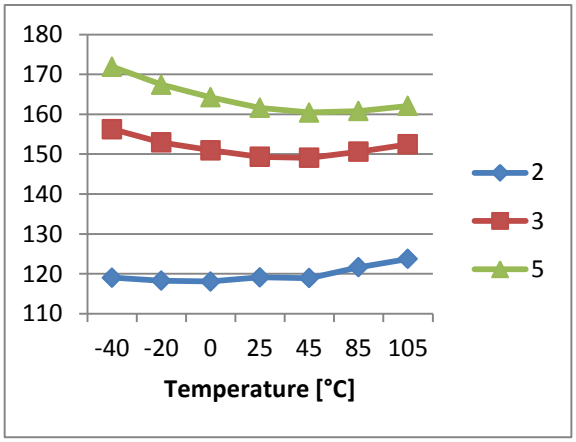



Figure 10.3 NP current consumption [uA], in XLP mode, no streaming.

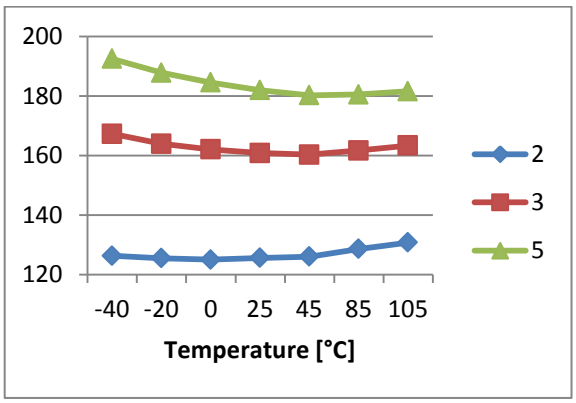



Figure 10.4 Current Consumption [uA] in NP (XLP) mode while streaming.

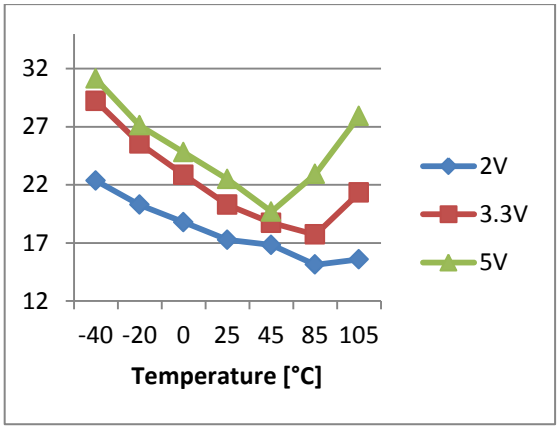



Figure 10.5 LP4 current consumption [uA], no streaming.

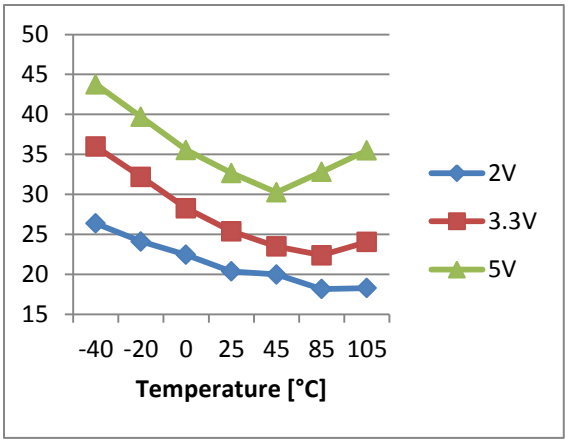



Figure 10.6 Current consumption [uA] in LP4 while streaming.

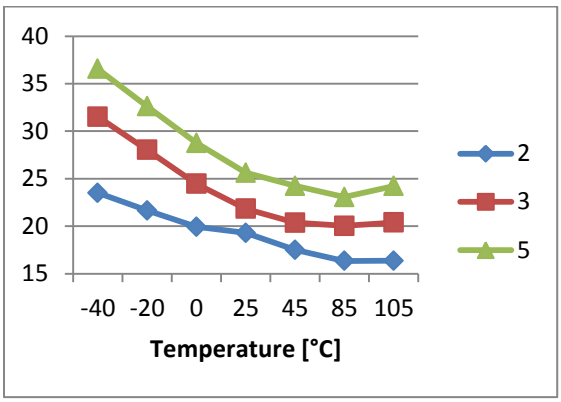



Figure 10.7 Current consumption [uA] in LP4 (XLP) mode while streaming.

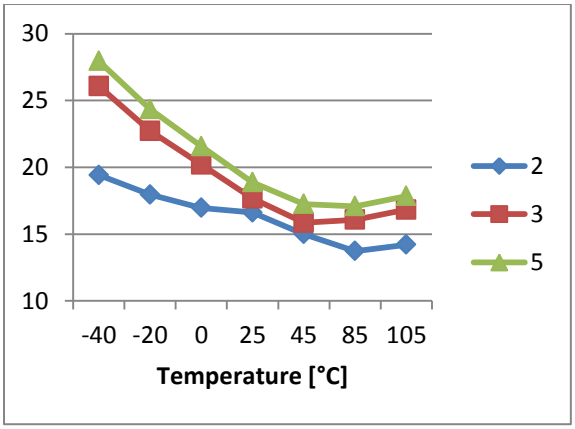



Figure 10.8 LP4 current consumption [uA], in XLP mode, no streaming.

## 10.4 Timing Characteristics

### Table 10-3 Timing Characteristics.

| DESCRIPTION | SYMBOL | IQS222 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| Report Rate (All 8 channels) | | | 15[1] | | Hz |
| Report Rate (One group – 3 channels only) | | | 45[1] | | Hz |
| Time before switching back to LP Mode | $T_{LOW\_POWER}$ | | 3.3 | | s |
| Cx charging Oscillator | $F_{Cx}$ | 213 | 250 | 287 | kHz |
| Touch Response Time | $T_{DEBOUNCE.Touch}$ | 50[2] | 142[3] | | ms |
| Proximity Response Time | $T_{DEBOUNCE.Prox}$ | 90[2] | 260[3] | | ms |

[1] Count Value = 25ms in NP mode

[2] Count Value = 12ms and only 1 Group active – 3 channels. Fast charge selected in NP mode.

[3] Count Value = 12ms and all channels active. Fast charge selected in NP mode.

# 11 Packaging Information

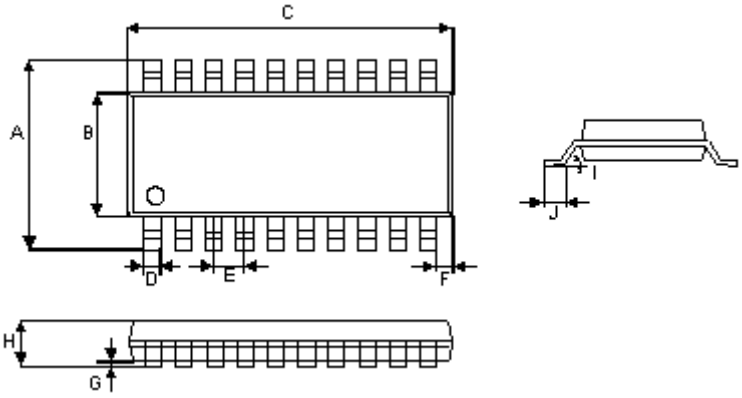



**Figure 11.1 1 SO-20 Package**

**Table 11.1 SO-20 Dimensions**

| Dimension | Min | Max |
|---|---|---|
| A | 7.40 mm | 8.20 mm |
| B | 5.00 mm | 5.60 mm |
| C | 12.30 mm | 12.90 mm |
| D | 0.35 mm | 0.51 mm |
| E | 1.27 mm Typ | |
| F | 0.29 mm Typ | |
| G | 0.05 mm | 0.20 mm |
| H | | 2.00 mm |
| I | 5° Typ | |
| J | 0.55 mm | 1.05 mm |

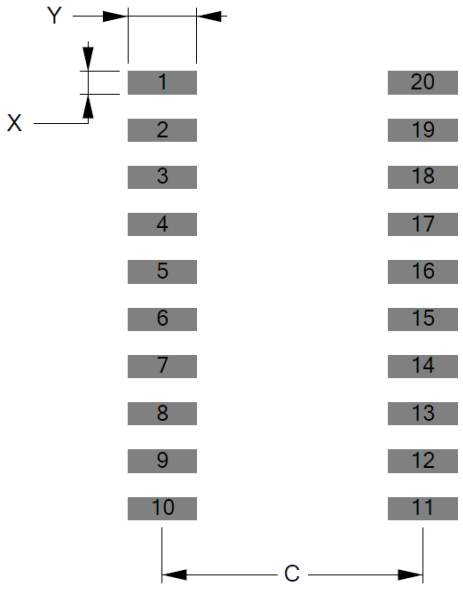



**Figure 11.2 SO-20 Footprint**

**Table 11.3 SO-20 Dimensions from Figure 11.2.**

| Dimension | [mm] |
|---|---|
| Pitch | 1.27 |
| C | 7.00 |
| Y | 1.85 |
| X | 0.60 |

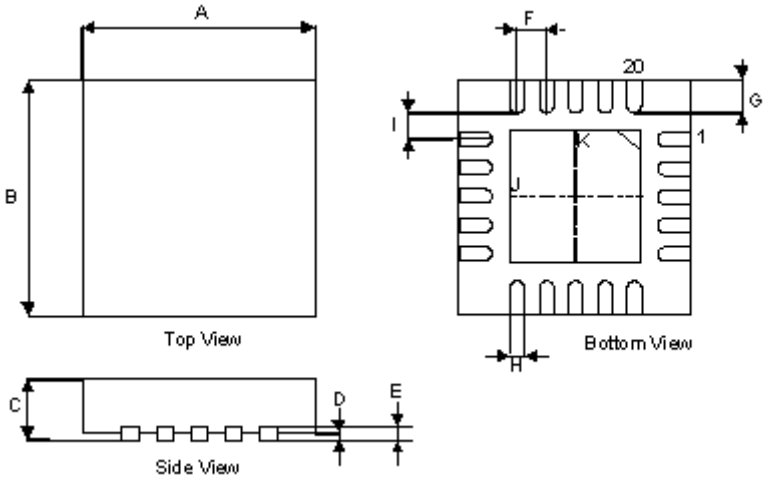



**Figure 11.3 QFN (4x4) -20 Package**

**Table 11.4 QFN (4x4)-20 Dimensions from Figure 11.3**

| Dimension | Min | Max |
|---|---|---|
| A,B | 3.85 mm | 4.15 mm |
| C | 0.70 mm | 1.00 mm |
| D | 0.00 mm | 0.05 mm |
| E | 0.203 mm Ref. | |
| F | 0.5 mm Typ | |
| G | 0.30mm | 0.50 mm |
| H | 0.18 mm | 0.30 mm |
| I | 0.2 mm Min. | |
| J,K | | 2.25mm |

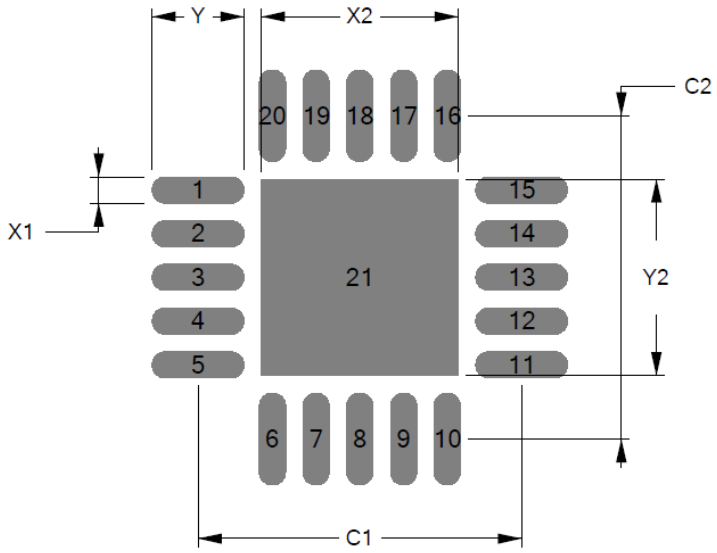


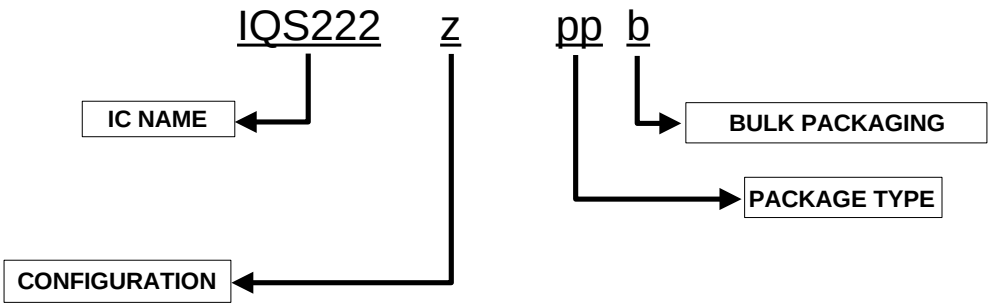

**Figure 11.4 QFN (4x4) - 20 Footprint.**

**Table 11.5 QFN (4x4) – 20 Dimensions from Figure 11.4**

| Dimension | [mm] |
|---|---|
| Pitch | 0.50 |
| C1 | 3.70 |
| Y1 | 1.05 |
| X1 | 0.30 |
| C2 | 3.70 |
| Y2 | 2.25 |
| X2 | 2.25 |

# 12 Ordering and Part-number Information

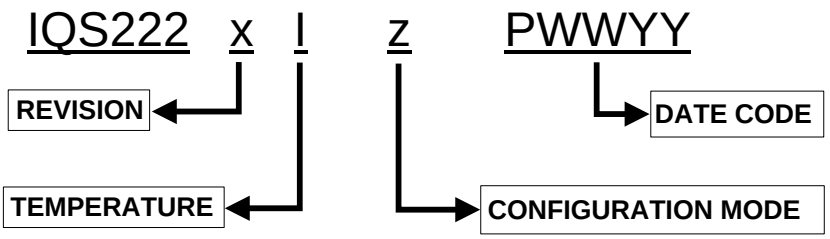
## 12.1 Ordering Information




Please check stock availability with your local distributor.

| | | | | |
|---|---|---|---|---|
| **CONFIGURATION** | | z | = | 0 : ICA1 = 0 |
| | | | | 1 : ICA1 = 1 |
| **PACKAGE TYPE** | | QN | = | QFN(4x4)-20 |
| | | SO | = | SO-20 |
| **BULK PACKAGING** | QFN(4x4)-20 | R | = | Reel: 3000pcs/reel |
| | | T | = | Tube: 92/pcs/tube |
| | SO-20 | T | = | Tube: 40/pcs/tube |

## 12.2 Device Numbering Convention




| | | | |
|---|---|---|---|
| **REVISION** | x | = | IC Revision Number |
| **TEMPERATURE RANGE** | I | = | -40°C to 85°C (Industrial) |
| **IC CONFIGURATION** | z | = | 0 : ICA1 = 0 |
| | | | 1 : ICA1 = 1 |
| **DATE CODE** | P | = | Package House |
| | WW | = | Week |
| | YY | = | Year |

**Example:** IQS222 2C 0 12308 = Revision 2; Commercial Temperature Range; ICA1=0; Packaged at facility 1 the 23RD week of 2008

# 13 Device Limitations

The limitations for specific revision numbers (refer to Section 12.2) are described below:

| Revision | Device ID[1] | Package Markings | Limitations |
|---|---|---|---|
| 0 | 0C01 | IQS222 ENG<br>24109 | • Multiple slave devices on I²C bus not supported<br>• Sleep functionality not supported<br>• Channel disable not supported<br>• Custom LTA write not supported<br>• I²C address 0xC6 to 0xCB not supported, FILTER_CFG at address 0xC6<br>• Only 2 touch threshold groupings are supported, a touch group for channels 0-6 and a group for channel 7<br>• RDY is active high<br>• I²C communication only has timeout option (timeout is approx. 800µs)<br>• Address 0x04 |
| 1 | 0C02 | IQS222 1C0<br>10110 | • Sleep functionality is not supported on an I²C bus with multiple slave devices<br>• Device sub-address selection using ICA0 is not supported<br>• RDY is active high<br>• I²C communication only has timeout option (timeout is approx. 800µs)<br>• Address 0x04 |
| 2 | 0C03 | IQS222 2IO<br>QFN 11410<br>SO20 21410 | • Address change:<br>0x70<br>0x71<br>0x72 &0x73 (Special order)<br>• RDY active Low |
| 3 | 1801 | IQS222 2IO<br>QFN x2410 (or later)<br>SO20 x2410 (or later) | • Production IC<br>• No change from 0C03 |

[1] Refers to product number and firmware version (See Sections 8.1 and 8.2)

# 14 Datasheet Revision History

Version 1.00 – Official Release

Version 1.03

- Changed RDY to $\overline{\text{RDY}}$
- Changed device addresses (refer to Section 6.5.2)
- Changed Section 6.1
- Added "$\overline{\text{RDY}}$ Timeout Enable" (refer to Section 8.16)

Version 1.04

- Updated Section 13

Version 1.05

- Include Engineering version IC address
- Include Reference Design Section 9

Version 1.06

- Add MP version characterisation data
- Change datasheet format

Version 1.07

- Reference for supply voltage below 2.8V

Version 1.08

- Updated Package dimensions to IPC7351A standard
- Included PCB footprint from IPC standard

Version 1.09

- Added Communication Timeout (refer to Section 6.2)

# 15 Contact Information

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