Application Note: AZD013

IQ Switch® - ProxSense® Series

ProxSense® ESD performance overview

Contents

Introduction

Many ESD standards such as the Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM), and IEC 61000-4-2 have been developed to test for robustness and ensure ESD protection. These standards are often misunderstood and sometimes used interchangeably, which can result in tested, “protected” systems that later fail in the consumer’s hands. To ensure better product reliability, it is critical that today’s design engineer understand the significant differences between the manufacturing environment and system end user environment ESD testing. The purpose of traditional ESD testing of integrated circuits in the manufacturing environment is very different than system level testing. HBM, MM and CDM tests are intended to ensure that integrated circuits survive the manufacturing process. Processes such as packaging, final testing, shipment to a board assembly facility, placement on the circuit board, and the soldering process should be performed in controlled ESD environments that limit the level of ESD stress to which the device is exposed.

Integrated Circuits (ICs) are inherently susceptible to ESD damage. This damage can occur during the process of assembling the ICs into boards and finished systems, packaging or in the field. There are several current methods for rating ICs for ESD in the manufacturing environment. The most common include:

- **HBM** - this standard is intended to simulate a person becoming charged and discharging from a bare finger to ground through the circuit under test.
- **MM** - intended to simulate a charged manufacturing machine, discharging through the device to ground.
- **CDM** - simulates an integrated circuit becoming charged and discharging to a grounded metal surface.

The HBM is usually sufficient for the controlled ESD environment of the factory floor, but it is completely inadequate for system level testing. The levels of ESD strikes, both the voltages and the currents, can be much greater in the end user environment. For this reason, the industry uses a different testing standard for system level ESD testing. This standard is known as the IEC61000-4-2.

While most designers are familiar with the classic device level manufacturing tests that are applied to integrated circuits, the most common misunderstanding occurs between the HBM and IEC61000-4-2 standards. These two very different standards are designed for very different purposes.

1 Human Body Model (HBM)

The Human Body Model simulates the ESD phenomenon wherein a charged body directly transfers its accumulated electrostatic charge to the ESD-sensitive (ESDS) device. A common example of this phenomenon, and from which the name of this model was derived, is when a person accumulates static charge by walking across a carpet and then transferring all of the charge to an ESDS device by touching it. Of course, other 'non-human' materials that accumulate and transfer charge in a similar manner are also covered by the HBM. HBM ensures the immunity levels for ESD discharge in controlled manufacturing environment, which is very different from the real system operating environment. The HBM only guarantees that Integrated Circuits (ICs) can survive in the manufacturing process and be assembled to the system safely.

Table 1: Human Body Model Classification Criteria:

Class	Voltage Range
Class 0	<250 Volts
Class 1A	250 Volts to < 500 Volts
Class 1B	500 Volts to < 1000 Volts
Class 1C	1000 Volts to < 2000 Volts
Class 2	2000 Volts to < 4000 Volts
Class 3A	4000 Volts to < 8000 Volts
Class 3B	>= 8000 Volts

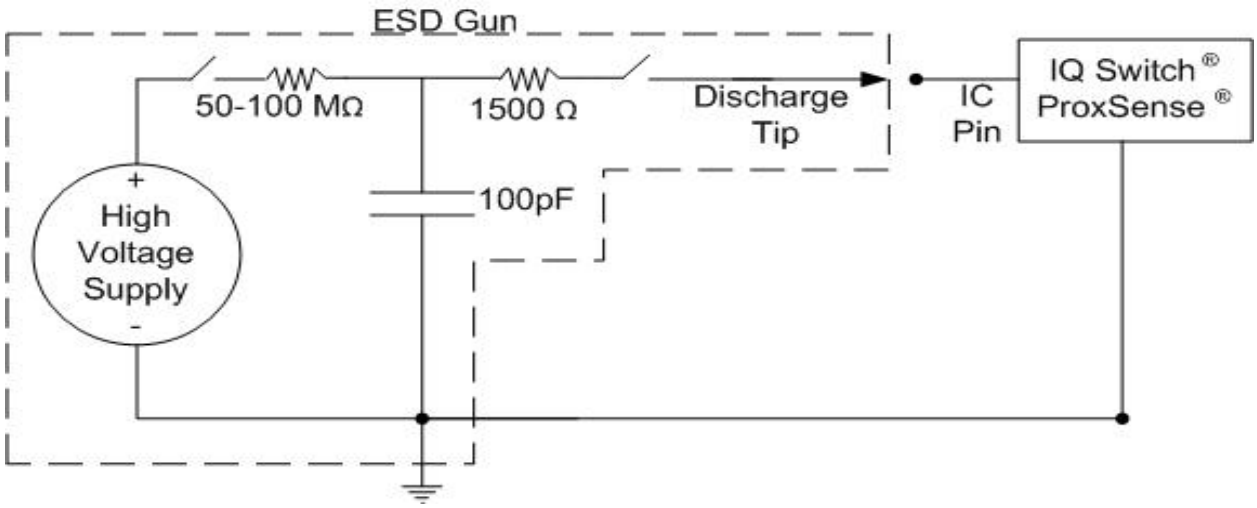

Figure 1: Example of the HBM ESD test setup.

2 IEC61000-4-2: ESD Standard for System Level Testing

The IEC standard is a system level test that replicates a charged person discharging to a system in a system end user environment. The purpose of the system level test is to ensure that finished products can survive normal operation and it is generally assumed that the user of the product will not take any ESD precautions to lower ESD stress to the product.

The IEC 61000-4-2 standard defines four standard levels of ESD protection, using two different testing methodologies: Contact Discharge and Air Discharge.

- Contact discharge involves discharging an ESD pulse directly from the ESD test gun that is touching the device under test. This is the preferred method of testing.
- In Air Discharge testing the rounded tip of the ESD tester should approach the Equipment under test (EUT) until a spark gap discharge takes place before actually touching the test point of the EUT. In general the reproducibility of the air discharge method is influenced by, for example, the speed of approach of the discharge tip, humidity, and construction of the ESD generator, leading to variations in pulse rise time and magnitude of the discharge current.

Table 2: IEC61000-4-2 Test Levels:

Contact Discharge		Air Discharge	
Level	**Test Voltage (kV)**	**Level**	**Test Voltage (kV)**
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X (See Notes))	Special	X (See Notes)	Special

Notes: *"X" is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those are specified, special test equipment may be required.*

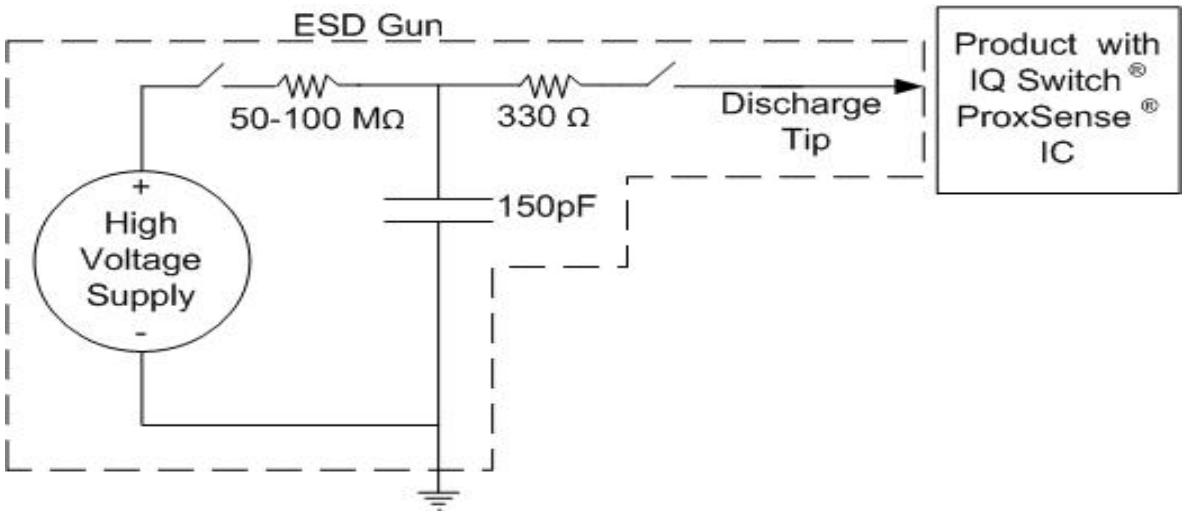

Figure 2: Example of the IEC61000-4-2 ESD test setup.

3 HBM versus IEC61000-4-2

There are several differences between the HBM and IEC61000-4-2 standard that are immediately obvious. The most important differences are:

- The amount of current and I^2R power released during a voltage strike
- The rise time of the voltage strike
- The number of voltage strikes repeated in the tests

The Amount of Current and I^2R Power Released During a Voltage Strike

A key difference between these two standards is the peak current level associated with a strike. As shown in Table 3, the peak current discharged during an 10KV HBM strike is less than the peak current discharged during a 2KV IEC61000-4-2 strike.

Table 3: Peak current of HBM vs. IEC 61000-4-2 ESD Standards

Applied Voltage (kV)	Peak Current (A) Human Body Model	Peak Current (A) IEC 61000-4-2
2	1.33	7.5
4	2.67	15
6	4	22.5
8	5.33	30
10	6.67	37.5

The difference in current is critical to whether the DUT will survive the ESD strike. Because high current levels can cause junction failures and metallization traces to melt. It is possible that a chip protected to 8KV HBM can be destroyed by a 2KV IEC61000-4-2 strike. For this reason, it is crucial that system design engineers do not rely on HBM ratings alone to determine whether a system will survive an ESD strike after it is shipped to end customers.

Rise Time of the Voltage Strike

Another key difference between these standards is the rise time of the voltage strike. The HBM model specifies a rise time of 25nS. An IEC pulse has a rise time of less than 1 nS and dissipates most of its energy in the first 30nS. If it takes 25nS to respond, the device rated using the HBM specification can be destroyed before its protection circuits are even activated

The Number of Voltage Strikes Repeated

Another difference between the HBM and IEC standards is the number of strikes used during testing. The HBM standard requires 3 positive and 3 negative strikes to be discharged on each pin specified in the test, whereas the IEC61000-4-2 test requires 10 positive strikes and 10 negative strikes. It is possible for a device to survive the first strike, but fail on subsequent strikes due to damage sustained during the initial strike.

4 ESD Protection Methods

4.1 Series Rx for improved ESD performance

The Sense Electrode is usually exposed and placing a series resistor (R_X) between the ProxSense®IC pin and sense electrode (C_X) can improve the system ESD protection capabilities of the device. This resistance limits peak currents and helps dissipate some of the power in a transient. As with capacitor protection, precautions should be taken to ensure that circuit operation is not affected adversely by this increased impedance.

From the IEC 61000-4-2 ESD test, the required series resistance can be given by

$$R_X = \left(\frac{V_{ESD} - V_{MAX^{pad}}}{I_{ESD}}\right) - 330 \qquad (\Omega)$$

- V_{ESD} is the required ESD threshold according to the IEC61000-4-2 standard.
- $V_{MAX^{pad}}$ is the maximum pin voltage. In most of Azoteq's ICs that value is 7.5V.
- I_{ESD} is the peak input current that the specific IC pin can handle during the HBM test. To determine the $I_{ESD:}$ Divide the ICs HBM Voltage Rating by the value of the discharge resistor of the ESD model (1500Ω) Ex: A 2KV rated IC: 2000 V / 1500 Ω = 1.33A.

➢ **Table 4: Example of I_{ESD} and HBM ESD Rating**

HBM ESD Rating (KV)	HBM Peak Current (A) I_{ESD}
2	1.33
3	2
4	2.67
5	3.33
6	4
7	4.67

Thus to obtain an IEC 4kV ESD rating of a specific product that uses an IC with a HBM Rating of 2KV:

$$R_X = \left(\frac{4000 - 7.5}{1.33}\right) - 330 \qquad (\Omega)$$

$$R_X = 2672 \qquad (\Omega)$$

Thus the value of Rx has to be at least 2.7KΩ.

Taking physical component parameters and the breakdown-voltage of air into consideration, it is advised to not use type 0603 surface mount resistors for ESD requirements above V_{ESD} = 4.6kV. For higher ESD requirements, it is recommended that multiple 0603 or 1206 components are used.

An increase in R_X may reduce the sensitivity of a ProxSense® device when used for proximity detection.

4.2 Overlay Specification

An overlay is a non-conductive material used to isolate the touch pad from the user. Overlays are generally used to increase the robustness of a design, enabling the design to withstand higher levels of ESD.

Typical overlay materials include Perspex/Plexi-glass, standard window glass and other plastic / non-conductive materials. Table 5 gives a summary of certain commonly used overlay materials and their properties.

Table 5: Overlay material properties

Material	Permittivity (ε_r)	Breakdown voltage (V/mm) (approx.)
Air	1	1180
Glass (standard)	7.6 – 8.0	7800
Plexi-glass	2.8	17,700
Mylar	3	295,200
FR4	5.2	27,500
Nylon	3.2	16,000

In order for the ESD to punch through this layer, it would have to have a voltage higher than the material's dielectric strength, measured in volts (V) per unit thickness. If the insulating material is 2 mm thick and has a dielectric strength of 8 kV per mm, then the point at which ESD breakdown could occur would be equal to 2×8 = 16 kV. If the user decides to use Plexi-glass with a thickness of 2mm; then the ESD will have to be at least 35KV to break through to the Touch Pad.

*Please refer to **Application Note AZD008** for further design guidelines on overlays.*

4.3 TVS diodes

TVS diodes have been successfully integrated into projects assisted by Azoteq. TVS diodes are however, only required if ESD strikes are able to directly penetrate the Cx/SHLD pins on the ProxSense® IC device. This can occur if sense antennas or shield wires are exposed or if the ESD strike bends around an overlay or if there are defects in the overlay.

Implementing TVS diodes may influence the sensitivity of the design, as this establishes a parasitic capacitance on the Cx pin. The influence on sensitivity by a known capacitance will however, differ in every design, as it depends on (1) The initial parasitic capacitance of the design, (2) The Cs capacitor and (3) The ATI compensation required to achieve target counts. This has not been formally quantified, as these parameters have only been tested in individual cases.

It is recommended that when using TVS diodes, selecting a component with the lowest possible capacitance value is necessary, if sensible proximity detection is required. Furthermore, the effects of TVS diodes on the sensitivity of touch events are negligible when using low capacitance components.

It is also theoretically possible for the TVS diode to decrease the RF immunity of a design, because clamp diodes can act as RF detectors. It is thus recommended (when possible) to use an overlay for a design and placing an R_X resistor as close as possible to the IC, when designing a system which require high levels of ESD protection.

Examples of TVS Diodes that have been used in Azoteq Applications:

- NXP-PESD5V0X1BL: Ultra low capacitance bidirectional ESD protection diode
- MURATA-LXES2SBAA4-016: 4 Channel ESD protection diode

4.4 Spark gap implementation

The inclusion of "spark gaps" in the PCB layout of a design may be sufficient for improved ESD protection.

Spark gaps are generally implemented by routing an I/O line (i.e. the Cx line) so that its pad (furthest from the IC pin) is a small distance from a ground plane. The spark gap will then dissipate the current produced by an ESD strike when it sparks over. Figure 3 illustrates an example of this concept.

However, the spark gap area needs to be free from solder masks and other coatings to be able to function correctly as a spark gap. A build-up of carbon due the spark between the two points also influences the efficiency of the spark gap.

In addition, the spark gap may reduce the proximity sensitivity of ProxSense® devices, as ground traces effectively shunt capacitive field lines, but this has no notable effects on the touch performance of the devices.

The breakdown voltage of spark gaps on a PCB can be varied by changing the distance between the IC and ground traces. The shape of the electrodes also affects the breakdown voltage. Most people use simplistic rules of thumb to estimate spark gap breakdown voltages. Maybe the simplest and one is 1 kV/mm for air at normal atmospheric pressure. This is only an estimate and each specific spark gap layout and distance between the gap would determine the breakdown voltage.

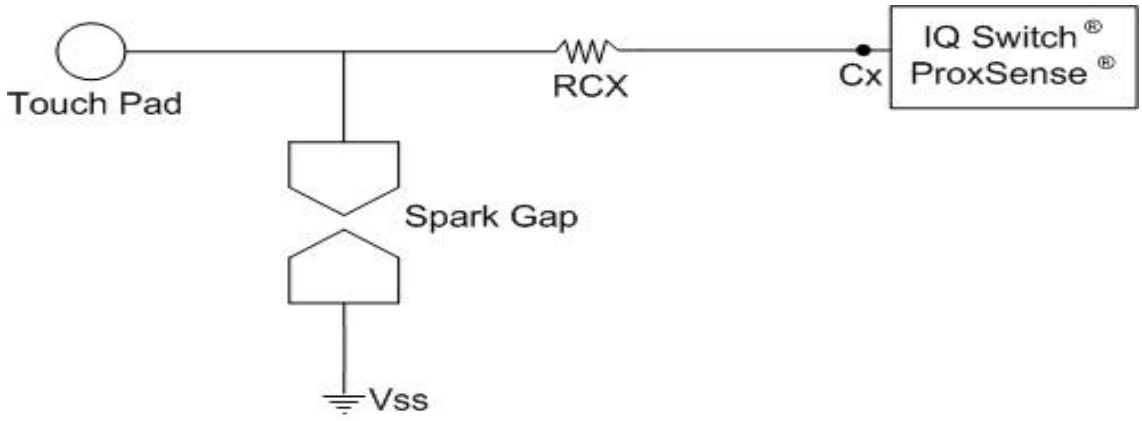

Figure 3: Example of a "spark gap" in a PCB layout.

4.5 ESD protection with BJT configuration

Bipolar junction transistors (BJTs) can be implemented to dissipate current spikes produced by ESD strikes. The configuration in Figure 4 shows a setup for advanced ESD protection using an NPN BJT.

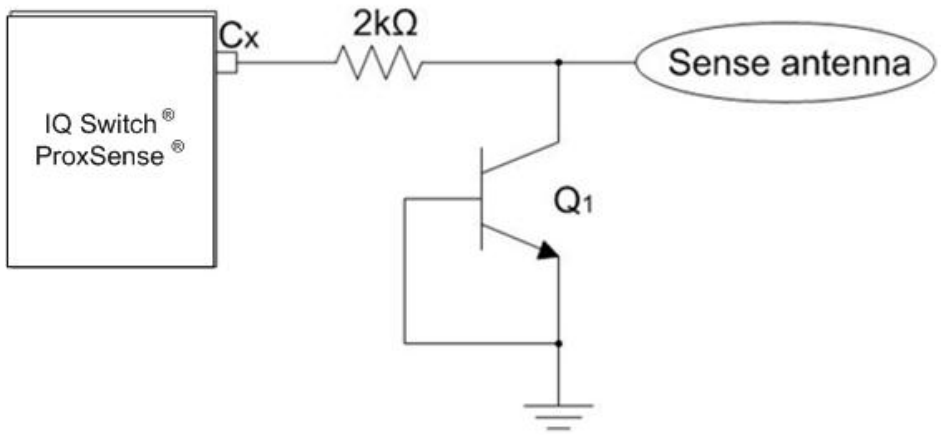

Figure 4: ESD protection with BJT network

The BJT network illustrated in Figure 4 forms an active ESD discharging circuit. Its functioning can be described by the avalanche breakdown effect of the BC-junction of the NPN transistor. The BC-junction enters a temporary breakdown state when the reverse junction voltage (V_{BC}) is increased above its threshold (V_{BCO}), which typically occurs during ESD events.

When the transistor's BC-junction enters the avalanche breakdown mode, the transistor is switched on and dissipates the current produced by the ESD strike.

Parasitic capacitances between the base-collector (C_{BC}) and base-emitter (C_{BE}) of the NPN BJT (Figure 5) may influence the performance of the design. The full effects of the parasitic capacitance introduced on the Cx line, by adding the BJT network, has not been formally characterised by Azoteq as these parameters will vary with different components and different designs

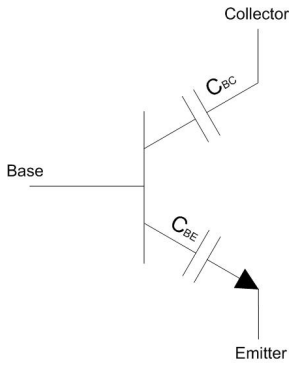

Figure 5: NPN BJT parasitic junction capacitance

It was however noticed that the sensitivity achieved for proximity detection, might be slightly influenced when adding an external BJT network for enhanced ESD protection, whereas the touch sensitivity seems to be unchanged. It is thus recommended to select a stable component with minimal parasitic capacitance and low noise characteristics in a design to achieve the desired ESD performance, whist maintaining maximum sensitivity.

4.6 Capacitor Protection

This method is common in high-volume consumer and automotive equipment. It protects the input pins with a simple shunt capacitor from input to ground. The idea is that a capacitor of sufficient value will absorb an ESD discharge without exceeding the ESD rating of the attached IC pin. In most ProxSense® IC applications an external capacitor can greatly affect the operation of the IC and this is not the most ideal protection method.

5 Conclusion

System designers need to be familiar with the differences between various ESD test standards. The ratings that are used for protecting ICs in the manufacturing environment such as HBM and CDM are not equivalent to system level ESD tests such as the IEC61000-4-2. Each standard has a legitimate purpose, but misapplying these standards can result in design delays and/or product returns. For system level ESD ratings, always use the IEC61000-4-2 standard. Most ESD ratings found on the Datasheets of Azoteq's ProxSense® and IQ Switch® ICs are HBM ratings and most ICs are rated at 2KV-4kKV HBM. Most of the newer generation Azoteq ICs are all rated at at least 4KV which puts them in the second highest HBM ESD rating: Class 3A.

The following The following patents relate to the device or usage of the device:

US 6,249,089 B1, US 6,621,225 B2, US 6,650,066 B2, US 6,952,084 B2, US 6,984,900 B1, US 7,084,526 B2, US 7,084,531 B2, US 7,119,459 B2, US 7,265,494 B2, US 7,291,940 B2, US 7,329,970 B2, US 7,336,037 B2, US 7,443,101 B2, US 7,466,040 B2, US 7,498,749 B2, US 7,528,508 B2, US 7,755,219 B2, US 7,772,781, US 7,781,980 B2, US 7,915,765 B2, EP 1 120 018 B1, EP 1 206 168 B1, EP 1 308 913 B1, EP 1 530 178 B1, ZL 99 8 14357.X, AUS 761094

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